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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2294hbd144-551

- 16 kB on-chip static RAM and 256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high-speed 60 MHz operation.
- In-System Programming/In-Application Programming (ISP/IAP) via on-chip bootloader software. Single flash sector or full chip erase in 400 ms and programming of 256 B in 1 ms.
- EmbeddedICE-RT and Embedded Trace interfaces offer real-time debugging with the on-chip RealMonitor software as well as high-speed real-time tracing of instruction execution.
- Two/four (LPC2292/2294) interconnected CAN interfaces with advanced acceptance filters. Additional serial interfaces include two UARTs (16C550), Fast I^2C-bus (400 kbit/s) and two SPIs.
- Eight channel 10-bit ADC with conversion time as low as 2.44 μs.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC), and watchdog.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Configurable external memory interface with up to four banks, each up to 16 MB and 8/16/32-bit data width.
- Up to 112 general purpose I/O pins (5 V tolerant). Up to nine edge/level sensitive external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- The on-chip crystal oscillator should have an operating range of 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
  - CPU operating voltage range of 1.65 V to 1.95 V (1.8 V ± 0.15 V).
  - I/O power supply range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2292FBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2292FET144/00	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/01	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2
LPC2292FET144/G	TFBGA144	plastic thin fine-pitch ball grid array package; 144 balls; body 12 × 12 × 0.8 mm	SOT569-2

Table 1. Ordering information *…continued*

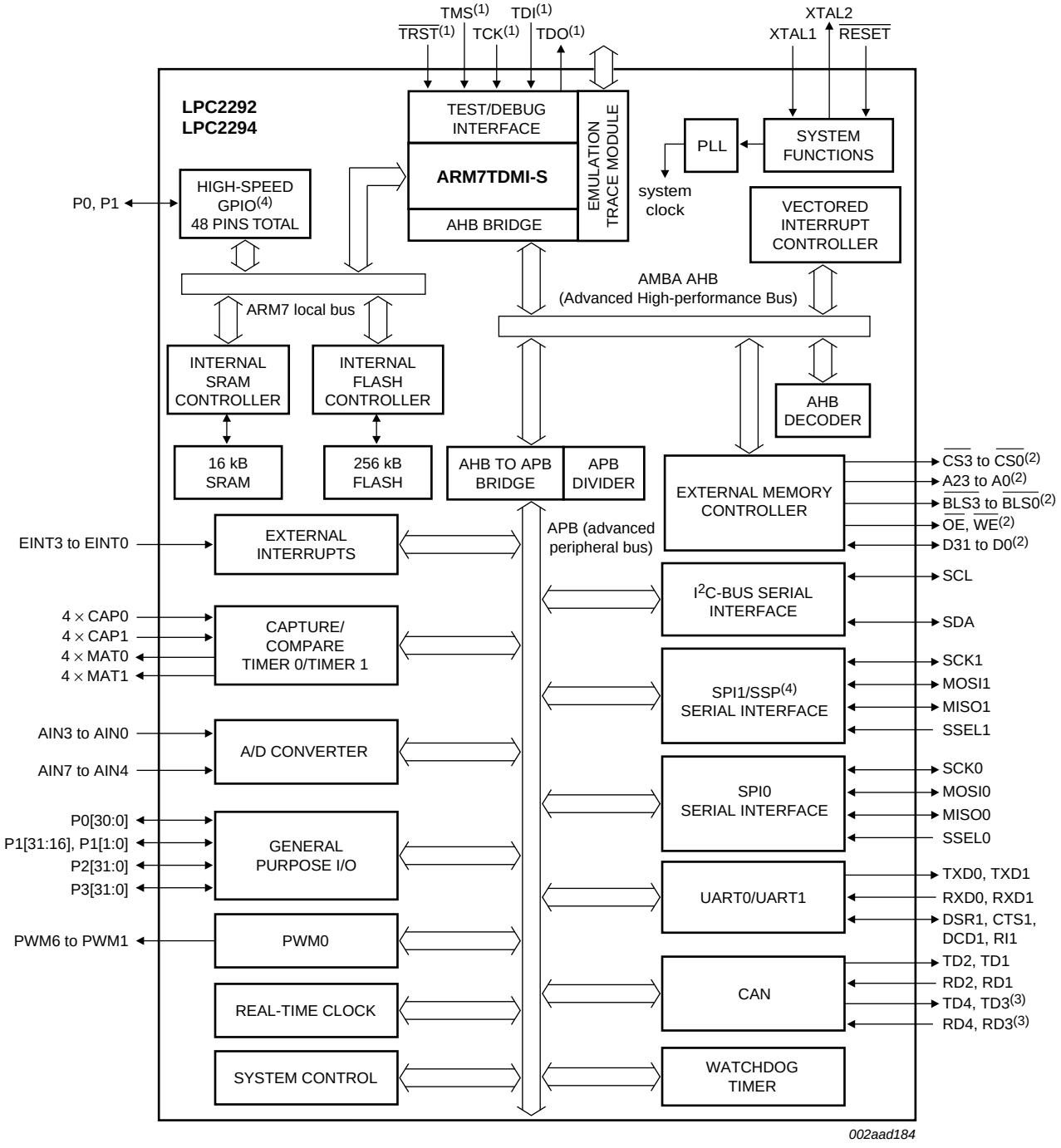
Type number	Package		
	Name	Description	Version
LPC2294HBD144	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/00	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1
LPC2294HBD144/01	LQFP144	plastic low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm	SOT486-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	CAN	Fast GPIO/ SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2292FBD144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/00	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2292FET144/01	256 kB	16 kB	2 channels	yes	−40 °C to +85 °C
LPC2292FET144/G	256 kB	16 kB	2 channels	no	−40 °C to +85 °C
LPC2294HBD144	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/00	256 kB	16 kB	4 channels	no	−40 °C to +125 °C
LPC2294HBD144/01	256 kB	16 kB	4 channels	yes	−40 °C to +125 °C

4. Block diagram



(1) When test/debug interface is used, GPIO/other functions sharing these pins are not available.

(2) Pins shared with GPIO.

(3) Available in LPC2294 only.

(4) SSP interface and high-speed GPIO are available on LPC2292/2294/01 only.

Fig 1. Block diagram

Table 3. Ball allocation

Row	Column 1	2	3	4	5	6	7	8	9	10	11	12	13
A	P2[22]/ D22	$V_{DDA(1V8)}$	P1[28]/ TDI	P2[21]/ D21	P2[18]/ D18	P2[14]/ D14	P1[29]/ TCK	P2[11]/ D11	P2[10]/ D10	P2[7]/D7	$V_{DD(3V3)}$	$V_{DD(1V8)}$	P2[4]/D4
B	$V_{DD(3V3)}$	P1[27]/ TDO	XTAL2	$V_{SSA(PLL)}$	P2[19]/ D19	P2[15]/ D15	P2[12]/ D12	P0[20]/ MAT1[3]/ SSEL1/ EINT3	$V_{DD(3V3)}$	P2[6]/D6	V_{SS}	P2[3]/D3	V_{SS}
C	P0[21]/ PWM5/ CAP1[3]	V_{SS}	XTAL1	V_{SSA}	RESET	P2[16]/ D16	P2[13]/ D13	P0[19]/ MAT1[2]/ MOSI1/ CAP1[2]	P2[9]/D9	P2[5]/D5	P2[2]/D2	P2[1]/D1	$V_{DD(3V3)}$
D	P0[24]/ TD2	P1[19]/ TRACE PKT3	P0[23]/ RD2	P0[22]/ CAP0[0]/ MAT0[0]	P2[20]/ D20	P2[17]/ D17	V_{SS}	P0[18]/ CAP1[3]/ MISO1/ MAT1[3]	P2[8]/D8	P1[30]/ TMS	V_{SS}	P1[20]/ TRACE SYNC	P0[17]/ CAP1[2]/ SCK1/ MAT1[2]
E	P2[25]/ D25	P2[24]/ D24	P2[23]	V_{SS}						P0[16]/ EINT0/ MAT0[2]/ CAP0[2]	P0[15]/ RI1/ EINT2	P2[0]/D0	P3[30]/ BLS1
F	P2[27]/ D27/ BOOT1	P1[18]/ TRACE PKT2	$V_{DDA(3V3)}$	P2[26]/ D26/ BOOT0						P3[31]/ BLS0	P1[21]/ PIPE STAT0	$V_{DD(3V3)}$	V_{SS}
G	P2[29]/ D29	P2[28]/ D28	P2[30]/ D30/AIN4	P2[31]/ D31/AIN5						P0[14]/ DCD1/ EINT1	P1[0]/CS0	P3[0]/A0	P1[1]/OE
H	P0[25]/ RD1	TD1	P0[27]/ AIN0/ CAP0[1]/ MAT0[1]	P1[17]/ TRACE PKT1						P0[13]/ DTR1/ MAT1[1]	P1[22]/ PIPE STAT1	P3[2]/A2	P3[1]/A1
J	P0[28]/ AIN1/ CAP0[2]/ MAT0[2]	V_{SS}	P3[29]/ BLS2/ AIN6	P3[28]/ BLS3/ AIN7						P3[3]/A3	P1[23]/ PIPE STAT2	P0[11]/ CTS1/ CAP1[1]	P0[12]/ DSR1/ MAT1[0]
K	P3[27]/ WE	P3[26]/ CS1	$V_{DD(3V3)}$	P3[22]/ A22	P3[20]/ A20	P0[1]/ RXD0/ PWM3/ EINT0	P3[14]/ A14	P1[25]/ EXTIN0	P3[11]/ A11	$V_{DD(3V3)}$	P0[10]/ RTS1/ CAP1[0]	V_{SS}	P3[4]/A4

Table 3. Ball allocation *…continued*

Row	Column												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
L	P0[29]/ AIN2/ CAP0[3]/ MAT0[3]	P0[30]/ AIN3/ EINT3/ CAP0[0]	P1[16]/ TRACE PKT0	P0[0]/ TXD0/ PWM1	P3[19]/ A19	P0[2]/ SCL/ CAP0[0]	P3[15]/ A15	P0[4]/ SCK0/ CAP0[1]	P3[12]/ A12	V_{SS}	P1[24]/ TRACE CLK	P0[8]/ TXD1/ PWM4	P0[9]/ RXD1/ PWM6/ EINT3
M	P3[25]/ $\overline{CS2}$	P3[24]/ $\overline{CS3}$	$V_{DD(3V3)}$	P1[31]/ $\overline{TRST}$	P3[18]/ A18	$V_{DD(3V3)}$	P3[16]/ A16	P0[3]/ SDA/ MAT0[0]/ EINT1	P3[13]/ A13	P3[9]/A9	P0[7]/ SSEL0/ PWM2/ EINT2	P3[7]/A7	P3[5]/A5
N	$V_{DD(1V8)}$	V_{SS}	P3[23]/ A23/ XCLK	P3[21]/ A21	P3[17]/ A17	P1[26]/ RTCK	V_{SS}	$V_{DD(3V3)}$	P0[5]/ MISO0/ MAT0[1]	P3[10]/ A10	P0[6]/ MOSI0/ CAP0[2]	P3[8]/A8	P3[6]/A6

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	42[2]	L4[2]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49[4]	K6[4]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50[5]	L6[5]	I/O	**SCL —** I^2C-bus clock input/output. Open-drain output (for I^2C-bus compliance).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58[5]	M8[5]	I/O	**SDA —** I^2C-bus data input/output. Open-drain output (for I^2C-bus compliance).
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59[2]	L8[2]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61[2]	N9[2]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68[2]	N11[2]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69[4]	M11[4]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	75[2]	L12[2]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76[4]	L13[4]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78[2]	K11[2]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83[2]	J12[2]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84[2]	J13[2]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			I	**RD4 —** CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85[2]	H10[2]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**TD4 —** CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92[4]	G10[4]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99[4]	E11[4]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100[4]	E10[4]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101[2]	D13[2]	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121[2]	D8[2]	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave.
			O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122[2]	C8[2]	O	**MAT1[2] —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave.
			I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123[4]	B8[4]	O	**MAT1[3] —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave.
			I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4[2]	C1[2]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**RD3 —** CAN3 receiver input (LPC2294 only).
			I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5[2]	D4[2]	O	**TD3 —** CAN3 transmitter output (LPC2294 only).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	6[2]	D3[2]	I	**RD2 —** CAN2 receiver input.
P0[24]/TD2	8[2]	D1[2]	O	**TD2 —** CAN2 transmitter output.
P0[25]/RD1	21[2]	H1[2]	I	**RD1 —** CAN1 receiver input.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[27]/AIN0/ CAP0[1]/ MAT0[1]	23[6]	H3[6]	I	**AIN0 —** ADC, input 0. This analog input is always connected to its pin.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[28]/AIN1/ CAP0[2]/ MAT0[2]	25[6]	J1[6]	I	**AIN1 —** ADC, input 1. This analog input is always connected to its pin.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
P0[29]/AIN2/ CAP0[3]/ MAT0[3]	32[6]	L1[6]	I	**AIN2 —** ADC, input 2. This analog input is always connected to its pin.
			I	**CAP0[3] —** Capture input for Timer 0, Channel 3.
			O	**MAT0[3] —** Match output for Timer 0, channel 3.
P0[30]/AIN3/ EINT3/CAP0[0]	33[6]	L2[6]	I	**AIN3 —** ADC, input 3. This analog input is always connected to its pin.
			I	**EINT3 —** External interrupt 3 input.
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P1[0] to P1[31]			I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the Pin Connect Block. Pins 2 through 15 of port 1 are not available.
P1[0]/$\overline{\text{CS0}}$	91[7]	G11[7]	O	**$\overline{\text{CS0}}$ —** LOW-active Chip Select 0 signal. (Bank 0 addresses range 0x8000 0000 to 0x80FF FFFF)
P1[1]/$\overline{\text{OE}}$	90[7]	G13[7]	O	**$\overline{\text{OE}}$ —** LOW-active Output Enable signal.
P1[16]/ TRACEPKT0	34[7]	L3[7]	O	**TRACEPKT0 —** Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	24[7]	H4[7]	O	**TRACEPKT1 —** Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	15[7]	F2[7]	O	**TRACEPKT2 —** Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	7[7]	D2[7]	O	**TRACEPKT3 —** Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	102[7]	D12[7]	O	**TRACESYNC —** Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	95[7]	F11[7]	O	**PIPESTAT0 —** Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	86[7]	H11[7]	O	**PIPESTAT1 —** Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	82[7]	J11[7]	O	**PIPESTAT2 —** Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	70[7]	L11[7]	O	**TRACECLK —** Trace Clock. Standard I/O port with internal pull-up.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P3[17]/A17	48[7]	N5[7]	O	**A17 —** External memory address line 17.
P3[18]/A18	47[7]	M5[7]	O	**A18 —** External memory address line 18.
P3[19]/A19	46[7]	L5[7]	O	**A19 —** External memory address line 19.
P3[20]/A20	45[7]	K5[7]	O	**A20 —** External memory address line 20.
P3[21]/A21	44[7]	N4[7]	O	**A21 —** External memory address line 21.
P3[22]/A22	41[7]	K4[7]	O	**A22 —** External memory address line 22.
P3[23]/A23/ XCLK	40[7]	N3[7]	I/O	**A23 —** External memory address line 23.
			O	**XCLK —** Clock output.
P3[24]/$\overline{CS3}$	36[7]	M2[7]	O	**$\overline{CS3}$ —** LOW-active Chip Select 3 signal. (Bank 3 addresses range 0x8300 0000 to 0x83FF FFFF)
P3[25]/$\overline{CS2}$	35[7]	M1[7]	O	**$\overline{CS2}$ —** LOW-active Chip Select 2 signal. (Bank 2 addresses range 0x8200 0000 to 0x82FF FFFF)
P3[26]/$\overline{CS1}$	30[7]	K2[7]	O	**$\overline{CS1}$ —** LOW-active Chip Select 1 signal. (Bank 1 addresses range 0x8100 0000 to 0x81FF FFFF)
P3[27]/$\overline{WE}$	29[7]	K1[7]	O	**$\overline{WE}$ —** LOW-active Write enable signal.
P3[28]/$\overline{BLS3}$/ AIN7	28[6]	J4[6]	O	**$\overline{BLS3}$ —** LOW-active Byte Lane Select signal (Bank 3).
			I	**AIN7 —** ADC, input 7. This analog input is always connected to its pin.
P3[29]/$\overline{BLS2}$/ AIN6	27[6]	J3[6]	O	**$\overline{BLS2}$ —** LOW-active Byte Lane Select signal (Bank 2).
			I	**AIN6 —** ADC, input 6. This analog input is always connected to its pin.
P3[30]/$\overline{BLS1}$	97[7]	E13[7]	O	**$\overline{BLS1}$ —** LOW-active Byte Lane Select signal (Bank 1).
P3[31]/$\overline{BLS0}$	96[7]	F10[7]	O	**$\overline{BLS0}$ —** LOW-active Byte Lane Select signal (Bank 0).
TD1	22[7]	H2[7]	O	**TD1:** CAN1 transmitter output.
$\overline{RESET}$	135[8]	C5[8]	I	**External Reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	142[9]	C3[9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	141[9]	B3[9]	O	Output from the oscillator amplifier.
V_{SS}	3, 9, 26, 38, 54, 67, 79, 93, 103, 107, 111, 128	C2, E4, J2, N2, N7, L10, K12, F13, D11, B13, B11, D7	I	**Ground:** 0 V reference.
V_{SSA}	139	C4	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{SSA(PLL)}$	138	B4	I	**PLL analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	37, 110	N1, A12	I	**1.8 V core power supply:** This is the power supply voltage for internal circuitry.

6.8 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.8.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8.2 Features added with the Fast GPIO set of registers available on LPC2292/2294/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.9 10-bit ADC

The LPC2292/2294 each contain a single 10-bit successive approximation ADC with four multiplexed channels.

6.9.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.

6.9.2 ADC features available in LPC2292/2294/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2292/2294 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2292/2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.13.2 Features available in LPC2292/2294/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

6.18 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2292/2294. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $1/6$ of the CPU clock (CCLK) for the JTAG interface to operate.

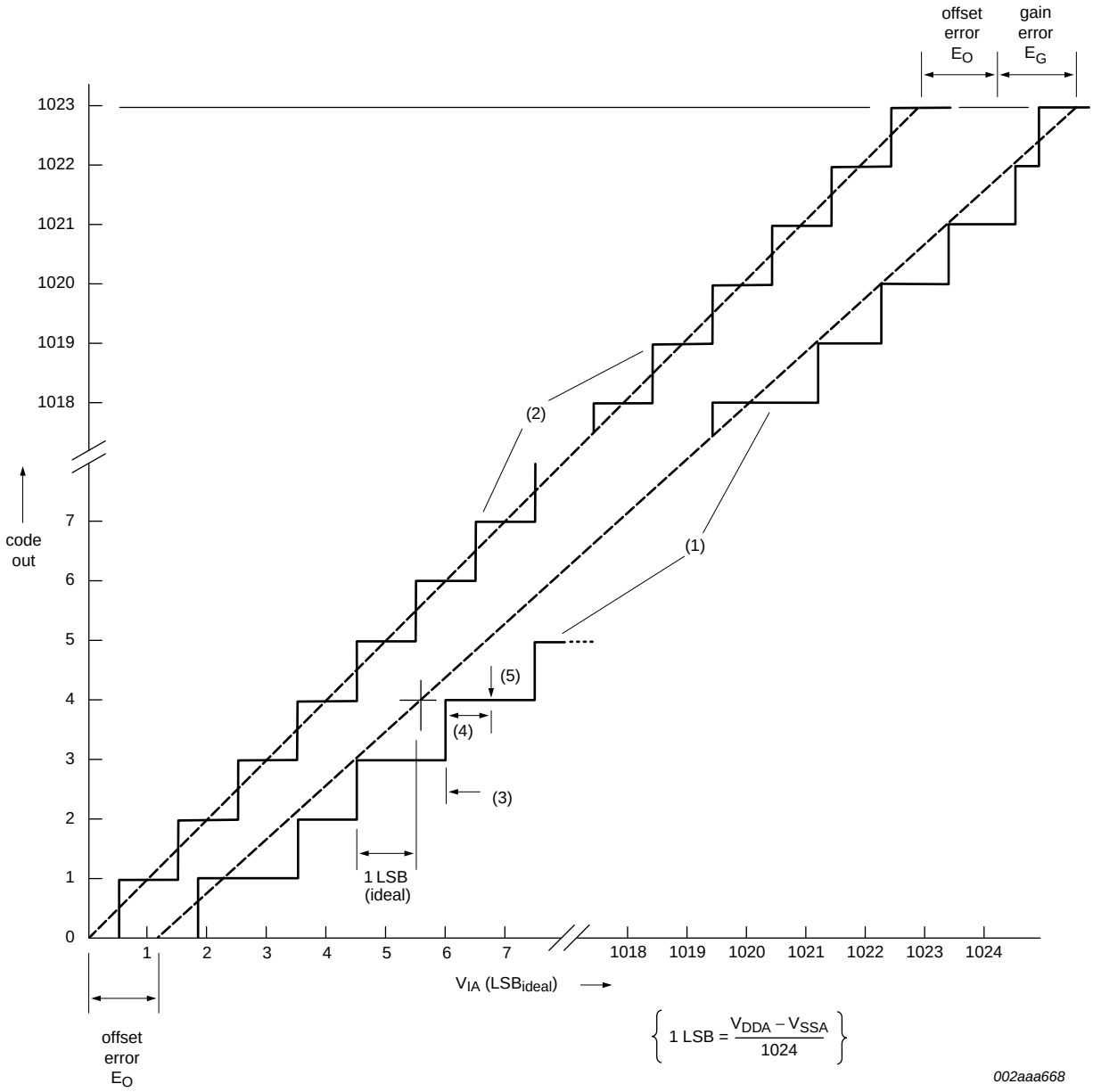
6.20.2 Embedded trace

Since the LPC2292/2294 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.20.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the Debug Communications Channel (DCC), which is present in the EmbeddedICE logic. The LPC2292/2294 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

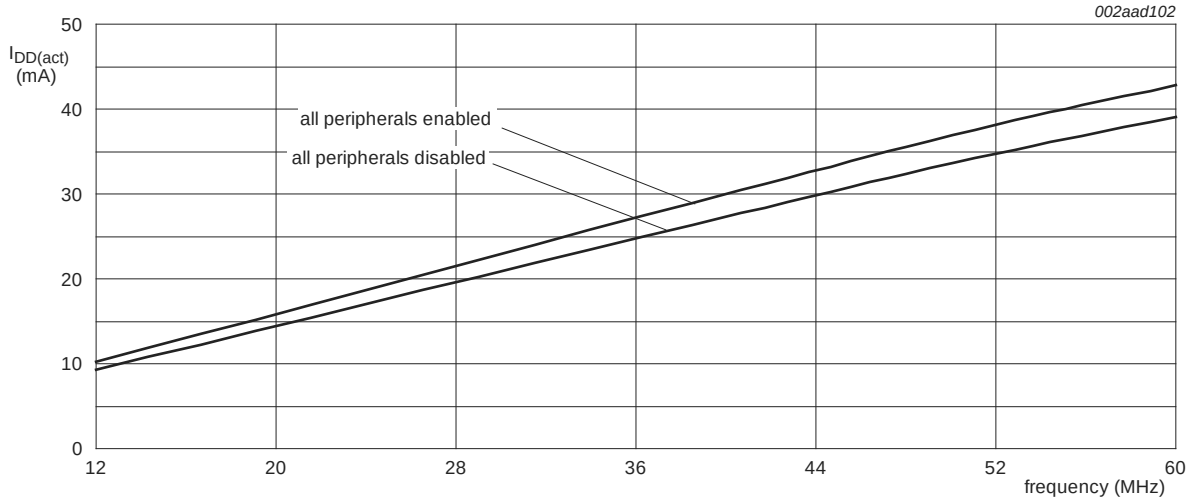
(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 5. ADC characteristics

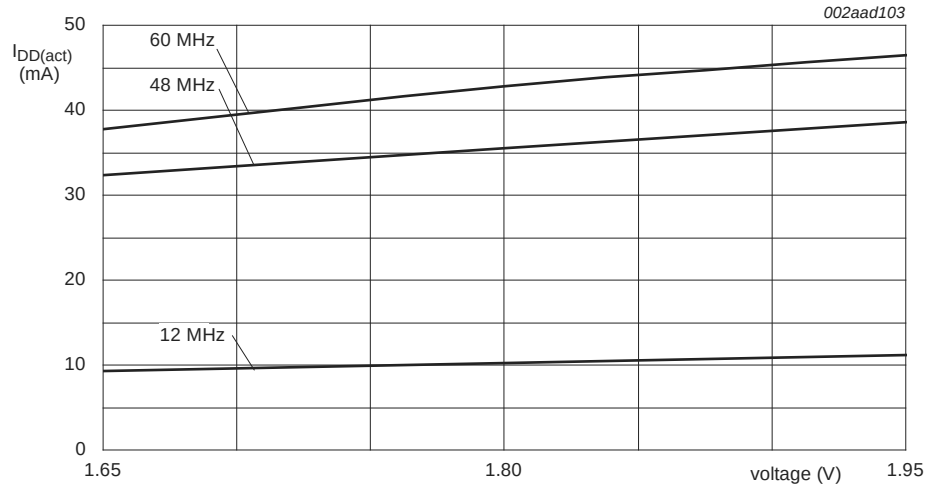
8.1 Power consumption measurements for LPC2292/01 and LPC2294/01

The power consumption measurements represent typical values for the given conditions. The peripherals were enabled through the PCONP register, but for these measurements, the peripherals were not configured to run. Peripherals were disabled through the PCONP register. For a description of the PCONP register bits, refer to the *LPC2119/2129/2194/2292/2294 User Manual*.



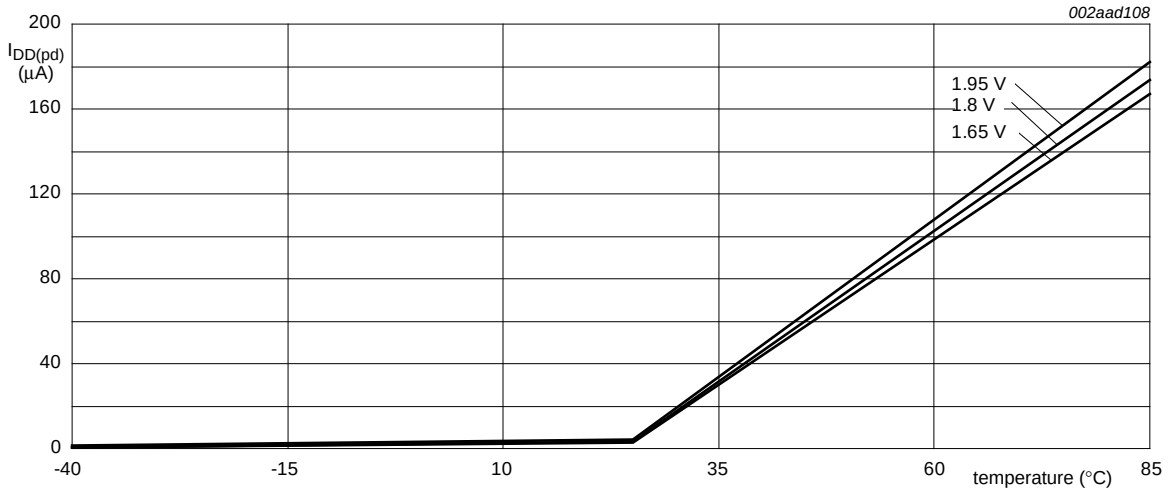
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; core voltage 1.8 V.

Fig 6. Typical LPC2292/01 $I_{DD(act)}$ measured at different frequencies



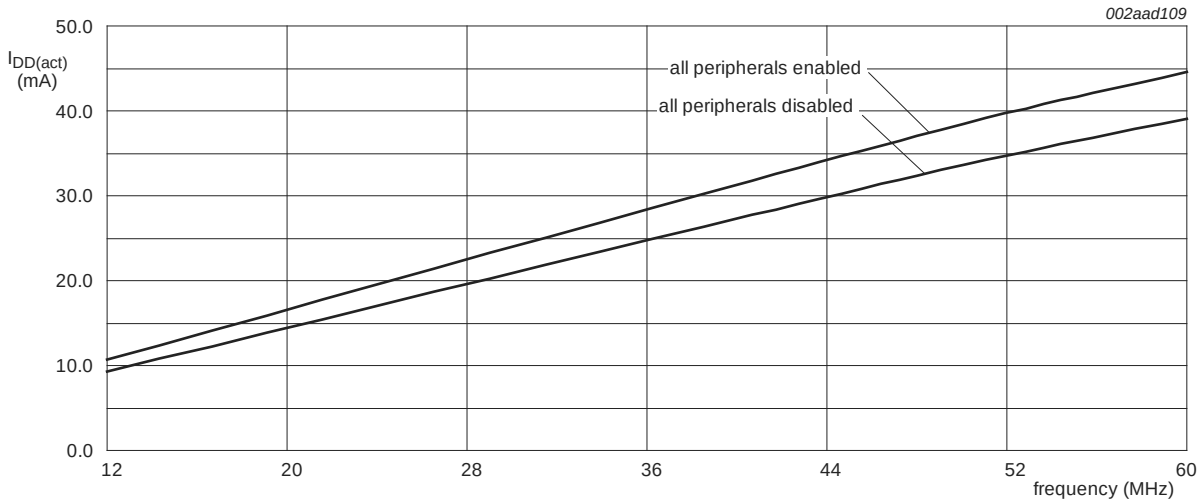
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 7. Typical LPC2292/01 $I_{DD(act)}$ measured at different core voltages



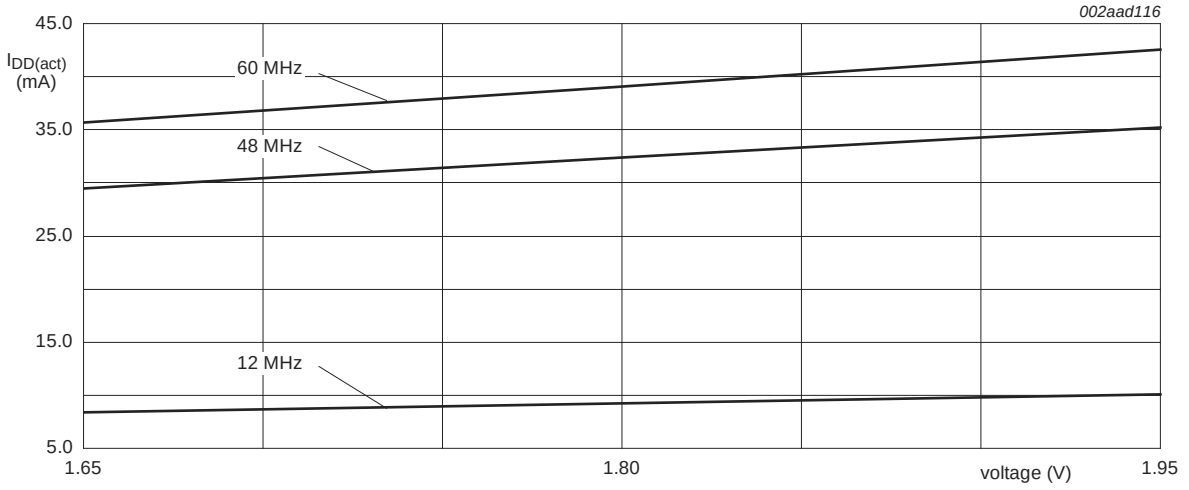
Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 12. Typical LPC2292/01 core power-down current $I_{DD(pd)}$ measured at different temperatures



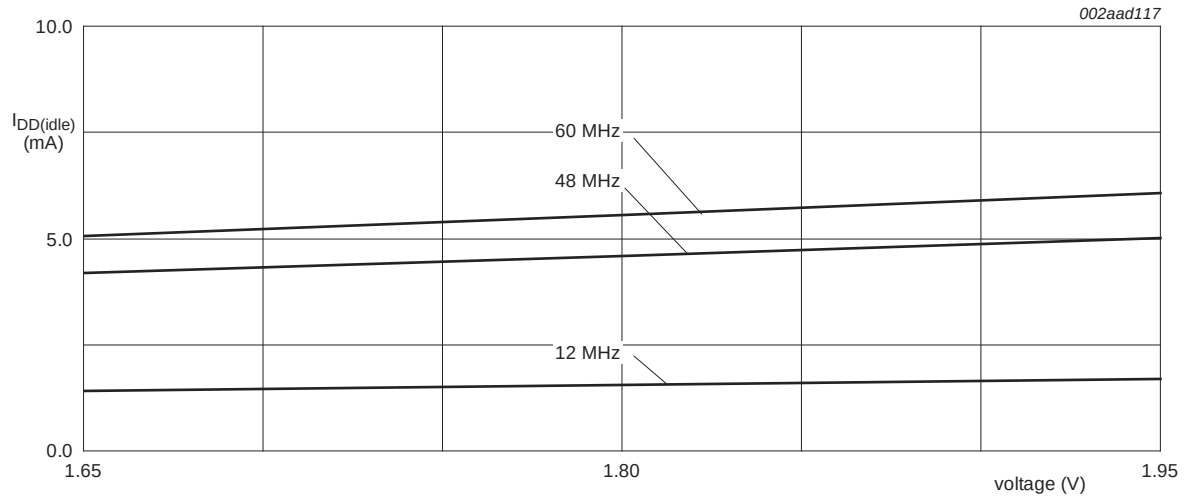
Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; core voltage 1.8 V.

Fig 13. Typical LPC2294/01 $I_{DD(act)}$ measured at different frequencies



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 20. Typical LPC2292/01 and LPC2294/01 $I_{DD(act)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals disabled.

Fig 21. Typical LPC2292/01 and LPC2294/01 $I_{DD(idle)}$ measured at different core voltages

Table 9. Typical LPC2292/01 peripheral power consumption in active mode

Core voltage 1.8 V; T_{amb} = 25 °C; all measurements in µA; PCLK = $^{CCLK}/_{4}$; all peripherals enabled.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421

Table 11. Dynamic characteristics *...continued*
T_{amb} = −40 °C to +125 °C; $V_{DD(1V8)}$, $V_{DD(3V3)}$ over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0[2] and P0[3])						
t_r	rise time		-	10	-	ns
t_f	fall time		-	10	-	ns
I^2C-bus pins (P0[2] and P0[3])						
t_f	fall time	V_{IH} to V_{IL}	[2] $20 + 0.1 \times C_b$	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Bus capacitance C_b in pF, from 10 pF to 400 pF.

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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