NXP USA Inc. - LPC2294JBD144,551 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	112
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2294jbd144-551

Table 3. **Ball allocation** *…continued*

Row	Column												
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**
L	P0[29]/ AIN2/ CAP0[3]/ MAT0[3]	P0[30]/ AIN3/ EINT3/ CAP0[0]	P1[16]/ TRACE PKT0	P0[0]/ TXD0/ PWM1	P3[19]/ A19	P0[2]/ SCL/ CAP0[0]	P3[15]/ A15	P0[4]/ SCK0/ CAP0[1]	P3[12]/ A12	V_{SS}	P1[24]/ TRACE CLK	P0[8]/ TXD1/ PWM4	P0[9]/ RXD1/ PWM6/ EINT3
M	P3[25]/ $\overline{\text{CS2}}$	P3[24]/ $\overline{\text{CS3}}$	$V_{DD(3V3)}$	P1[31]/ $\overline{\text{TRST}}$	P3[18]/ A18	$V_{DD(3V3)}$	P3[16]/ A16	P0[3]/ SDA/ MAT0[0]/ EINT1	P3[13]/ A13	P3[9]/A9	P0[7]/ SSEL0/ PWM2/ EINT2	P3[7]/A7	P3[5]/A5
N	$V_{DD(1V8)}$	V_{SS}	P3[23]/ A23/ XCLK	P3[21]/ A21	P3[17]/ A17	P1[26]/ RTCK	V_{SS}	$V_{DD(3V3)}$	P0[5]/ MISO0/ MAT0[1]	P3[10]/ A10	P0[6]/ MOSI0/ CAP0[2]	P3[8]/A8	P3[6]/A6

5.2 Pin description

Table 4. Pin description

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[0] to P0[31]			I/O	**Port 0:** Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	42[2]	L4[2]	O	**TXD0 —** Transmitter output for UART0.
			O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	49[4]	K6[4]	I	**RXD0 —** Receiver input for UART0.
			O	**PWM3 —** Pulse Width Modulator output 3.
			I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/ CAP0[0]	50[5]	L6[5]	I/O	**SCL —** I^{2}C-bus clock input/output. Open-drain output (for I^{2}C-bus compliance).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	58[5]	M8[5]	I/O	**SDA —** I^{2}C-bus data input/output. Open-drain output (for I^{2}C-bus compliance).
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
			I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	59[2]	L8[2]	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
			I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	61[2]	N9[2]	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
			O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	68[2]	N11[2]	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	69[4]	M11[4]	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
			O	**PWM2 —** Pulse Width Modulator output 2.
			I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/ PWM4	75[2]	L12[2]	O	**TXD1 —** Transmitter output for UART1.
			O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	76[4]	L13[4]	I	**RXD1 —** Receiver input for UART1.
			O	**PWM6 —** Pulse Width Modulator output 6.
			I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	78[2]	K11[2]	O	**RTS1 —** Request to Send output for UART1.
			I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	83[2]	J12[2]	I	**CTS1 —** Clear to Send input for UART1.
			I	**CAP1[1] —** Capture input for Timer 1, channel 1.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P0[12]/DSR1/ MAT1[0]/RD4	84[2]	J13[2]	I	**DSR1 —** Data Set Ready input for UART1.
			O	**MAT1[0] —** Match output for Timer 1, channel 0.
			I	**RD4 —** CAN4 receiver input (LPC2294 only).
P0[13]/DTR1/ MAT1[1]/TD4	85[2]	H10[2]	O	**DTR1 —** Data Terminal Ready output for UART1.
			O	**MAT1[1] —** Match output for Timer 1, channel 1.
			O	**TD4 —** CAN4 transmitter output (LPC2294 only).
P0[14]/DCD1/ EINT1	92[4]	G10[4]	I	**DCD1 —** Data Carrier Detect input for UART1.
			I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take over control of the part after reset.
P0[15]/RI1/ EINT2	99[4]	E11[4]	I	**RI1 —** Ring Indicator input for UART1.
			I	**EINT2 —** External interrupt 2 input.
P0[16]/EINT0/ MAT0[2]/ CAP0[2]	100[4]	E10[4]	I	**EINT0 —** External interrupt 0 input.
			O	**MAT0[2] —** Match output for Timer 0, channel 2.
			I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[17]/CAP1[2]/ SCK1/MAT1[2]	101[2]	D13[2]	I	**CAP1[2] —** Capture input for Timer 1, channel 2.
			I/O	**SCK1 —** Serial Clock for SPI1/SSP[3]. SPI clock output from master or input to slave.
			O	**MAT1[2] —** Match output for Timer 1, channel 2.
P0[18]/CAP1[3]/ MISO1/MAT1[3]	121[2]	D8[2]	I	**CAP1[3] —** Capture input for Timer 1, channel 3.
			I/O	**MISO1 —** Master In Slave Out for SPI1/SSP[3]. Data input to SPI master or data output from SPI slave.
			O	**MAT1[3] —** Match output for Timer 1, channel 3.
P0[19]/MAT1[2]/ MOSI1/CAP1[2]	122[2]	C8[2]	O	**MAT1[2] —** Match output for Timer 1, channel 2.
			I/O	**MOSI1 —** Master Out Slave In for SPI1/SSP[3]. Data output from SPI master or data input to SPI slave.
			I	**CAP1[2] —** Capture input for Timer 1, channel 2.
P0[20]/MAT1[3]/ SSEL1/EINT3	123[4]	B8[4]	O	**MAT1[3] —** Match output for Timer 1, channel 3.
			I	**SSEL1 —** Slave Select for SPI1/SSP[3]. Selects the SPI interface as a slave.
			I	**EINT3 —** External interrupt 3 input.
P0[21]/PWM5/ RD3/CAP1[3]	4[2]	C1[2]	O	**PWM5 —** Pulse Width Modulator output 5.
			I	**RD3 —** CAN3 receiver input (LPC2294 only).
			I	**CAP1[3] —** Capture input for Timer 1, channel 3.
P0[22]/TD3/ CAP0[0]/ MAT0[0]	5[2]	D4[2]	O	**TD3 —** CAN3 transmitter output (LPC2294 only).
			I	**CAP0[0] —** Capture input for Timer 0, channel 0.
			O	**MAT0[0] —** Match output for Timer 0, channel 0.
P0[23]/RD2	6[2]	D3[2]	I	**RD2 —** CAN2 receiver input.
P0[24]/TD2	8[2]	D1[2]	O	**TD2 —** CAN2 transmitter output.
P0[25]/RD1	21[2]	H1[2]	I	**RD1 —** CAN1 receiver input.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P1[25]/EXTIN0	60[7]	K8[7]	I	**EXTIN0 —** External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	52[7]	N6[7]	I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\mathrm{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	144[7]	B2[7]	O	**TDO —** Test Data out for JTAG interface.
P1[28]/TDI	140[7]	A3[7]	I	**TDI —** Test Data in for JTAG interface.
P1[29]/TCK	126[7]	A7[7]	I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	113[7]	D10[7]	I	**TMS —** Test Mode Select for JTAG interface.
P1[31]/$\overline{\mathrm{TRST}}$	43[7]	M4[7]	I	**$\overline{\mathrm{TRST}}$ —** Test Reset for JTAG interface.
P2[0] to P2[31]			I/O	**Port 2 —** Port 2 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 2 pins depends upon the pin function selected via the Pin Connect Block.
P2[0]/D0	98[7]	E12[7]	I/O	**D0 —** External memory data line 0.
P2[1]/D1	105[7]	C12[7]	I/O	**D1 —** External memory data line 1.
P2[2]/D2	106[7]	C11[7]	I/O	**D2 —** External memory data line 2.
P2[3]/D3	108[7]	B12[7]	I/O	**D3 —** External memory data line 3.
P2[4]/D4	109[7]	A13[7]	I/O	**D4 —** External memory data line 4.
P2[5]/D5	114[7]	C10[7]	I/O	**D5 —** External memory data line 5.
P2[6]/D6	115[7]	B10[7]	I/O	**D6 —** External memory data line 6.
P2[7]/D7	116[7]	A10[7]	I/O	**D7 —** External memory data line 7.
P2[8]/D8	117[7]	D9[7]	I/O	**D8 —** External memory data line 8.
P2[9]/D9	118[7]	C9[7]	I/O	**D9 —** External memory data line 9.
P2[10]/D10	120[7]	A9[7]	I/O	**D10 —** External memory data line 10.
P2[11]/D11	124[7]	A8[7]	I/O	**D11 —** External memory data line 11.
P2[12]/D12	125[7]	B7[7]	I/O	**D12 —** External memory data line 12.
P2[13]/D13	127[7]	C7[7]	I/O	**D13 —** External memory data line 13.
P2[14]/D14	129[7]	A6[7]	I/O	**D14 —** External memory data line 14.
P2[15]/D15	130[7]	B6[7]	I/O	**D15 —** External memory data line 15.
P2[16]/D16	131[7]	C6[7]	I/O	**D16 —** External memory data line 16.
P2[17]/D17	132[7]	D6[7]	I/O	**D17 —** External memory data line 17.
P2[18]/D18	133[7]	A5[7]	I/O	**D18 —** External memory data line 18.
P2[19]/D19	134[7]	B5[7]	I/O	**D19 —** External memory data line 19.
P2[20]/D20	136[7]	D5[7]	I/O	**D20 —** External memory data line 20.
P2[21]/D21	137[7]	A4[7]	I/O	**D21 —** External memory data line 21.
P2[22]/D22	1[7]	A1[7]	I/O	**D22 —** External memory data line 22.
P2[23]/D23	10[7]	E3[7]	I/O	**D23 —** External memory data line 23.

Table 4. Pin description *…continued*

Symbol	Pin (LQFP)	Pin (TFBGA)[1]	Type	Description
P2[24]/D24	11[7]	E2[7]	I/O	**D24 —** External memory data line 24.
P2[25]/D25	12[7]	E1[7]	I/O	**D25 —** External memory data line 25.
P2[26]/D26/ BOOT0	13[7]	F4[7]	I/O	**D26 —** External memory data line 26.
			I	**BOOT0 —** While $\overline{\text{RESET}}$ is low, together with BOOT1 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected.
P2[27]/D27/ BOOT1	16[7]	F1[7]	I/O	**D27 —** External memory data line 27.
			I	**BOOT1 —** While $\overline{\text{RESET}}$ is low, together with BOOT0 controls booting and internal operation. Internal pull-up ensures high state if pin is left unconnected. BOOT1:0 = 00 selects 8-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 01 selects 16-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 10 selects 32-bit memory on $\overline{\text{CS0}}$ for boot. BOOT1:0 = 11 selects internal flash memory.
P2[28]/D28	17[7]	G2[7]	I/O	**D28 —** External memory data line 28.
P2[29]/D29	18[7]	G1[7]	I/O	**D29 —** External memory data line 29.
P2[30]/D30/ AIN4	19[6]	G3[6]	I/O	**D30 —** External memory data line 30.
			I	**AIN4 —** ADC, input 4. This analog input is always connected to its pin.
P2[31]/D31/ AIN5	20[6]	G4[6]	I/O	**D31 —** External memory data line 31.
			I	**AIN5 —** ADC, input 5. This analog input is always connected to its pin.
P3[0] to P3[31]			I/O	**Port 3 —** Port 3 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 3 pins depends upon the pin function selected via the Pin Connect Block.
P3[0]/A0	89[7]	G12[7]	O	**A0 —** External memory address line 0.
P3[1]/A1	88[7]	H13[7]	O	**A1 —** External memory address line 1.
P3[2]/A2	87[7]	H12[7]	O	**A2 —** External memory address line 2.
P3[3]/A3	81[7]	J10[7]	O	**A3 —** External memory address line 3.
P3[4]/A4	80[7]	K13[7]	O	**A4 —** External memory address line 4.
P3[5]/A5	74[7]	M13[7]	O	**A5 —** External memory address line 5.
P3[6]/A6	73[7]	N13[7]	O	**A6 —** External memory address line 6.
P3[7]/A7	72[7]	M12[7]	O	**A7 —** External memory address line 7.
P3[8]/A8	71[7]	N12[7]	O	**A8 —** External memory address line 8.
P3[9]/A9	66[7]	M10[7]	O	**A9 —** External memory address line 9.
P3[10]/A10	65[7]	N10[7]	O	**A10 —** External memory address line 10.
P3[11]/A11	64[7]	K9[7]	O	**A11 —** External memory address line 11.
P3[12]/A12	63[7]	L9[7]	O	**A12 —** External memory address line 12.
P3[13]/A13	62[7]	M9[7]	O	**A13 —** External memory address line 13.
P3[14]/A14	56[7]	K7[7]	O	**A14 —** External memory address line 14.
P3[15]/A15	55[7]	L7[7]	O	**A15 —** External memory address line 15.
P3[16]/A16	53[7]	M7[7]	O	**A16 —** External memory address line 16.

6.5 Interrupt controller

The VIC accepts all of the interrupt request inputs and categorizes them as Fast Interrupt Request (FIQ), vectored Interrupt Request (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are requesting, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Table 5 lists the interrupt sources for each peripheral function. Each peripheral device has one interrupt line connected to the VIC, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Table 5. Interrupt sources

Block	Flag(s)	VIC channel #
WDT	Watchdog Interrupt (WDINT)	0
-	Reserved for software interrupts only	1
ARM Core	EmbeddedICE, DbgCommRx	2
ARM Core	EmbeddedICE, DbgCommTx	3
Timer 0	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	4
Timer 1	Match 0 to 3 (MR0, MR1, MR2, MR3) Capture 0 to 3 (CR0, CR1, CR2, CR3)	5
UART0	RX Line Status (RLS) Transmit Holding Register Empty (THRE) RX Data Available (RDA) Character Time-out Indicator (CTI) Auto-baud time-out (ABTO)[1]End of auto-baud (ABEO)[1]	6

receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2292/2294 supports bit rate up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus may be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2292/2294 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.13.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.13.2 Features available in LPC2292/2294/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit prescaler.

6.19 System control

6.19.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 25 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.19.2 “PLL” for additional information.

6.19.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle.The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.19.3 Reset and wake-up timer

Reset has two sources on the LPC2292/2294: the $\overline{\text{RESET}}$ pin and watchdog reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal reset is removed, the processor begins executing at address 0, which is the reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The Wake-up Timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power-on, all types of reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.20.2 Embedded trace

Since the LPC2292/2294 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The Embedded Trace Macrocell (ETM) provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code cannot be traced because of this restriction.

6.20.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real-time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the Debug Communications Channel (DCC), which is present in the EmbeddedICE logic. The LPC2292/2294 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			–0.5	+4.6	V
V_{IA}	analog input voltage			–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][6]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		–2000	+2000	V

[1] The following applies to Table 6:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. Static characteristics

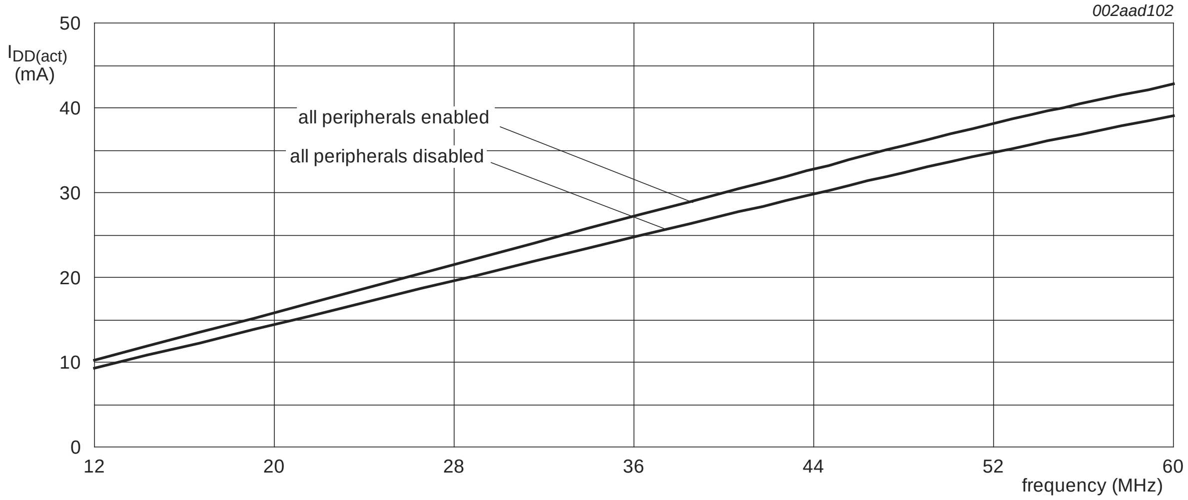
Table 7. Static characteristics

T_{amb} = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK						
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up	-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(3V3)}$; no pull-down	-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V, $V_O = V_{DD(3V3)}$; no pull-up/down	-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C	100	-	-	mA
V_I	input voltage	[4][5][6]	0	-	5.5	V
V_O	output voltage	output active	0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA [7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA [7]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V [7]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V [7]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V [8]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD(3V3)}$ [8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V [10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I <$ 5 V [9]	0	0	0	μA

8.1 Power consumption measurements for LPC2292/01 and LPC2294/01

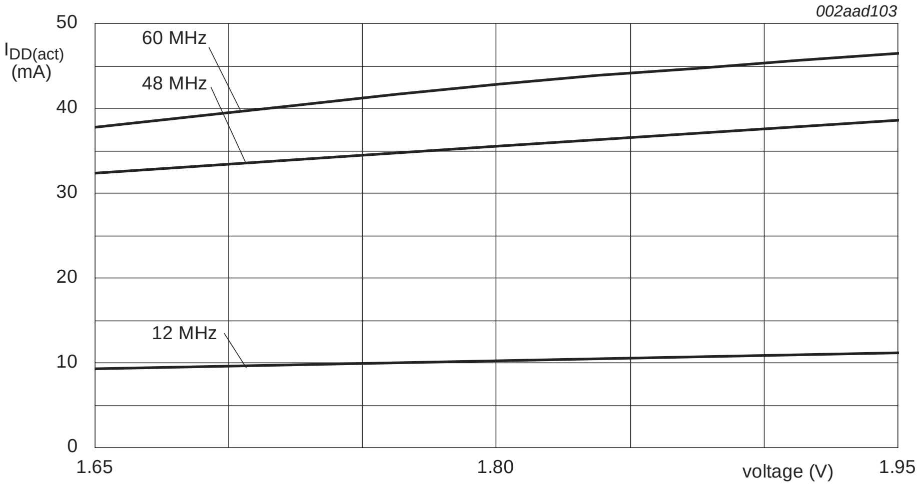
The power consumption measurements represent typical values for the given conditions. The peripherals were enabled through the PCONP register, but for these measurements, the peripherals were not configured to run. Peripherals were disabled through the PCONP register. For a description of the PCONP register bits, refer to the *LPC2119/2129/2194/2292/2294 User Manual*.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;

T_{amb} = 25 °C; core voltage 1.8 V.

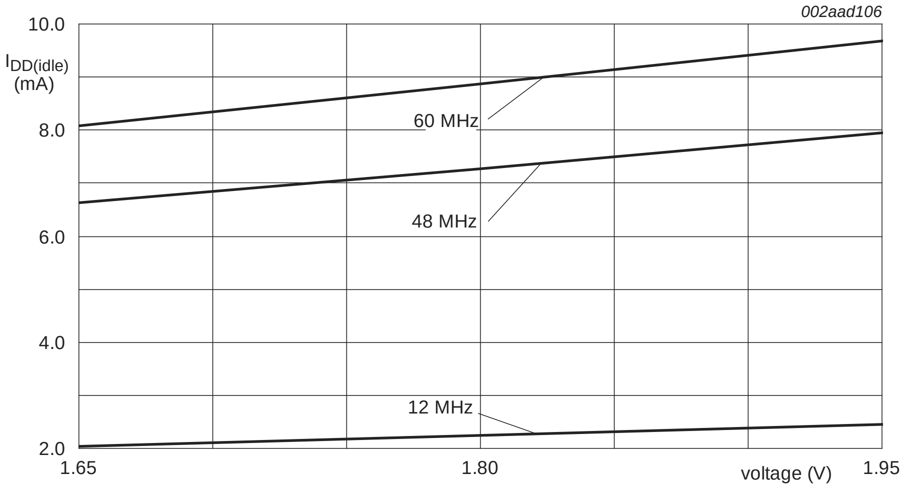
Fig 6. Typical LPC2292/01 $I_{DD(act)}$ measured at different frequencies



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;

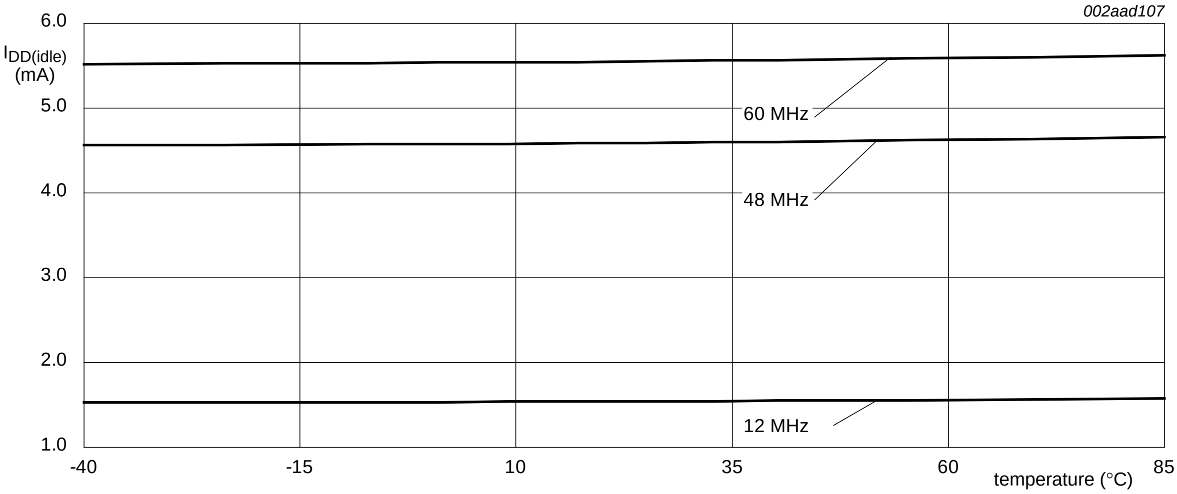
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 7. Typical LPC2292/01 $I_{DD(act)}$ measured at different core voltages



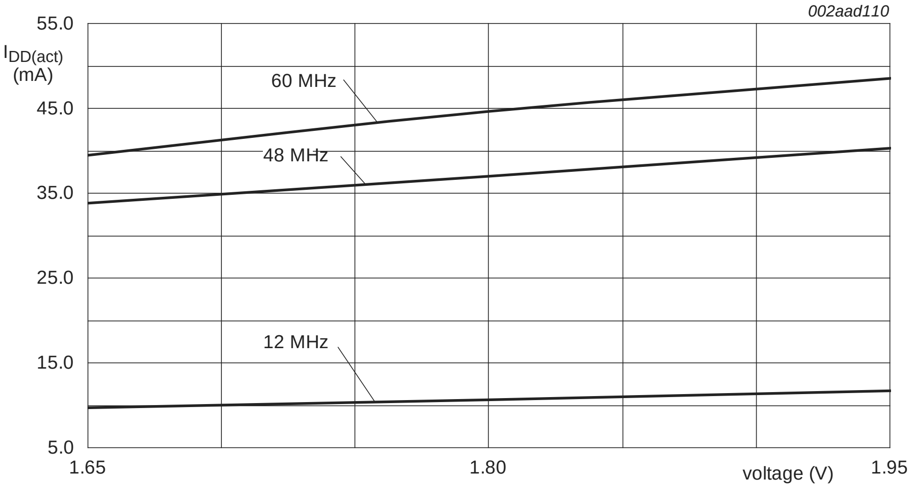
Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 10. Typical LPC2292/01 $I_{DD(idle)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$;
Core voltage 1.8 V; all peripherals disabled.

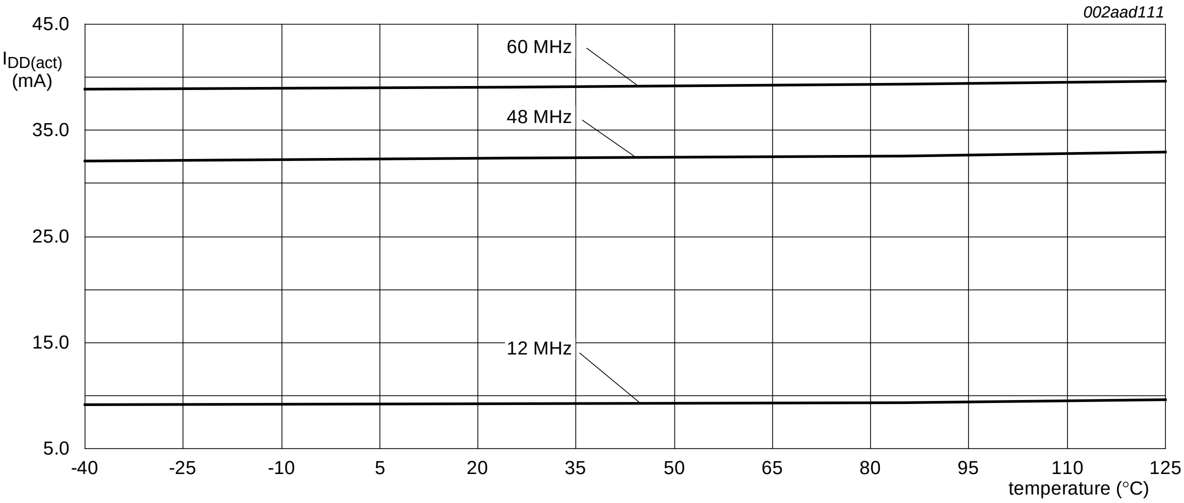
Fig 11. Typical LPC2292/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_4$;

T_{amb} = 25 °C; all peripherals enabled but not active.

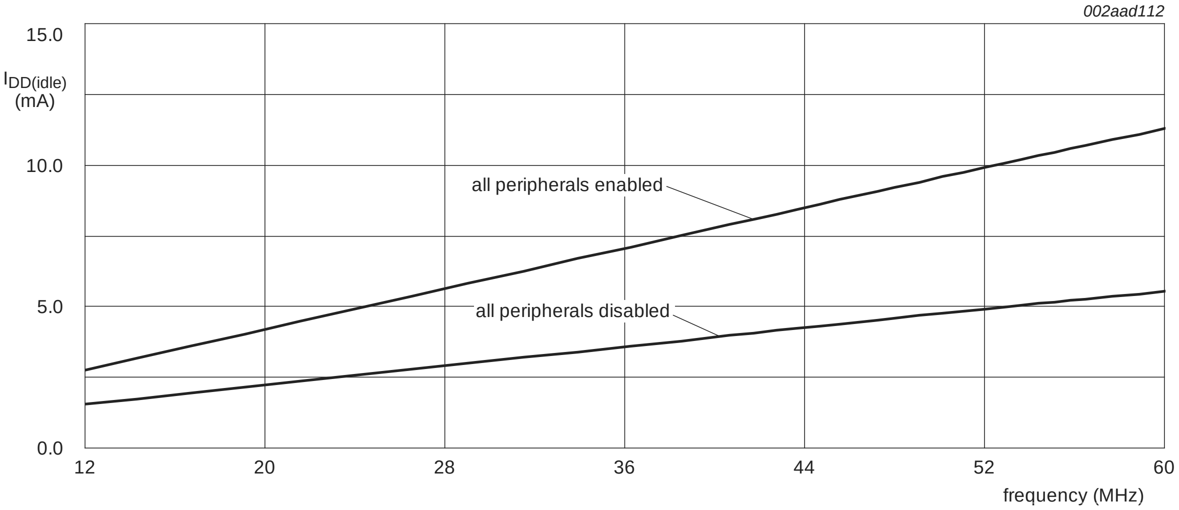
Fig 14. Typical LPC2294/01 $I_{DD(act)}$ measured at different core voltages



Test conditions: Active mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_4$;

core voltage 1.8 V; all peripherals disabled.

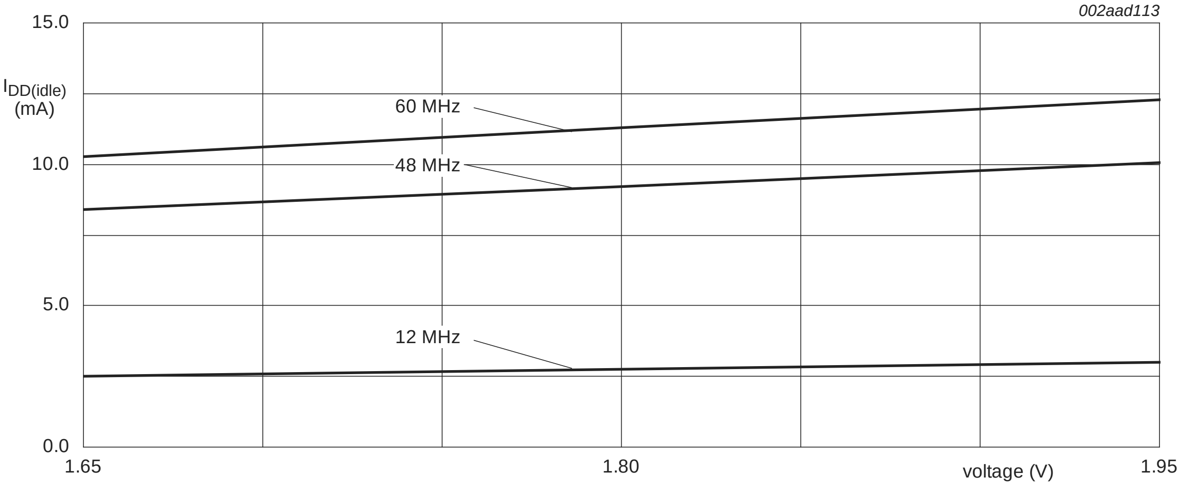
Fig 15. Typical LPC2294/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}\!/_4$;

T_{amb} = 25 °C; core voltage 1.8 V.

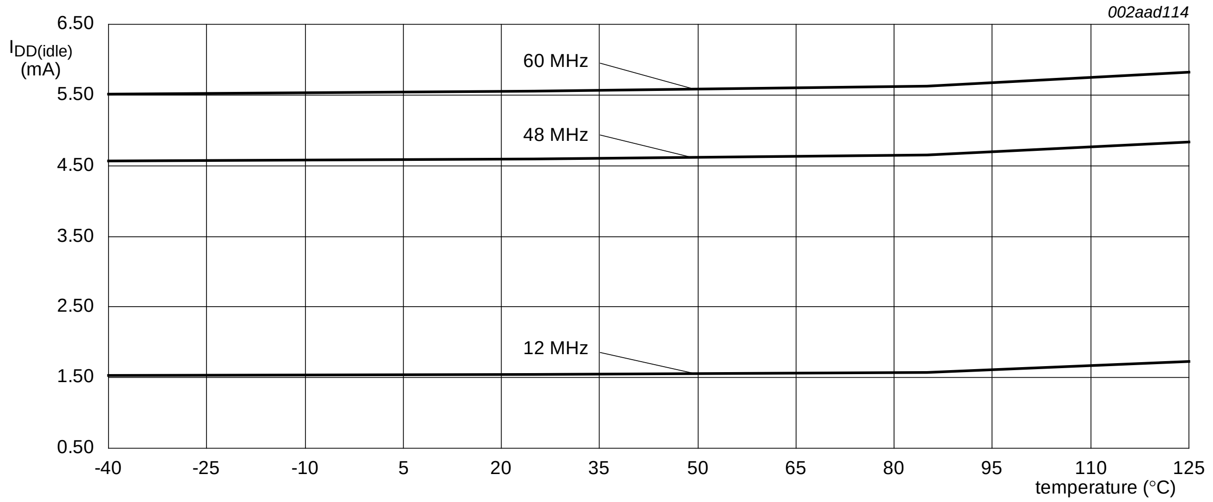
Fig 16. Typical LPC2294/01 $I_{DD(idle)}$ measured at different frequencies



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}\!/_4$;

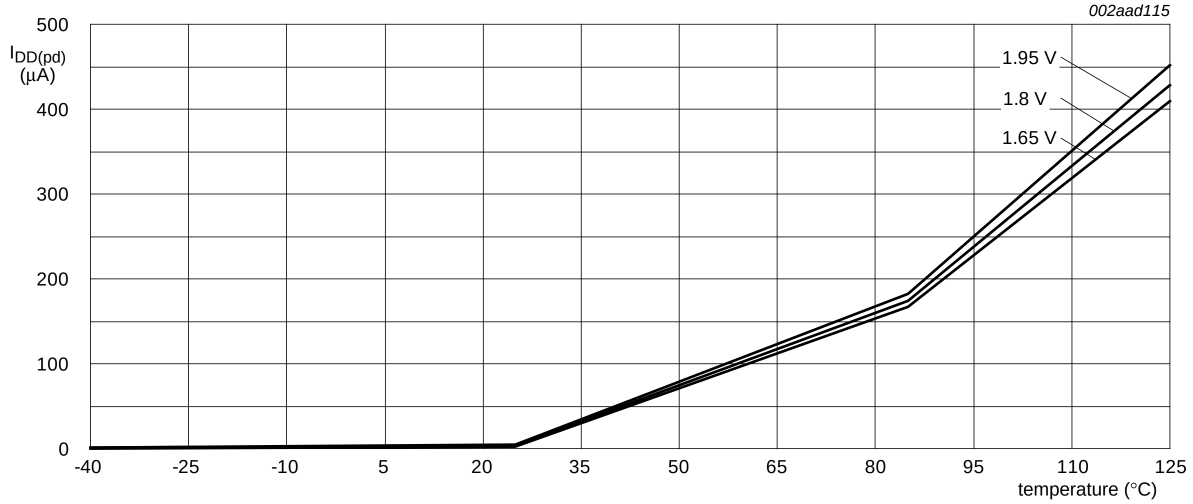
T_{amb} = 25 °C; all peripherals enabled but not active.

Fig 17. Typical LPC2294/01 $I_{DD(idle)}$ measured at different core voltages



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = $^{CCLK}/_{4}$; core voltage 1.8 V; all peripherals disabled.

Fig 18. Typical LPC2294/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 19. Typical LPC2294/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 12. External memory interface dynamic characteristics
C_L = 25 pF, T_{amb} = 40 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CHAV}	XCLK HIGH to address valid time		-	-	10	ns
t_{CHCSL}	XCLK HIGH to $\overline{\text{CS}}$ LOW time		-	-	10	ns
t_{CHCSH}	XCLK HIGH to $\overline{\text{CS}}$ HIGH time		-	-	10	ns
t_{CHANV}	XCLK HIGH to address invalid time		-	-	10	ns
Read cycle parameters						
t_{CSLAV}	$\overline{\text{CS}}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{OELAV}	$\overline{\text{OE}}$ LOW to address valid time	[1]	–5	-	+10	ns
t_{CSLOEL}	$\overline{\text{CS}}$ LOW to $\overline{\text{OE}}$ LOW time		–5	-	+5	ns
t_{am}	memory access time	[2][3]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(ibr)}$	memory access time (initial burst-ROM)	[2][3]	$(T_{cy(CCLK)} \times (2 + WST1)) + (-20)$	-	-	ns
$t_{am(sbr)}$	memory access time (subsequent burst-ROM)	[2][4]	$T_{cy(CCLK)} + (-20)$	-	-	ns
$t_{h(D)}$	data input hold time	[5]	0	-	-	ns
t_{CSHOEH}	$\overline{\text{CS}}$ HIGH to $\overline{\text{OE}}$ HIGH time		–5	-	+5	ns
t_{OEHANV}	$\overline{\text{OE}}$ HIGH to address invalid time		–5	-	+5	ns
t_{CHOEL}	XCLK HIGH to $\overline{\text{OE}}$ LOW time		–5	-	+5	ns
t_{CHOEH}	XCLK HIGH to $\overline{\text{OE}}$ HIGH time		–5	-	+5	ns
Write cycle parameters						
t_{AVCSL}	address valid to $\overline{\text{CS}}$ LOW time	[1]	$T_{cy(CCLK)} - 10$	-	-	ns
t_{CSLDV}	$\overline{\text{CS}}$ LOW to data valid time		–5	-	+5	ns
t_{CSLWEL}	$\overline{\text{CS}}$ LOW to $\overline{\text{WE}}$ LOW time		–5	-	+5	ns
$t_{CSLBLSL}$	$\overline{\text{CS}}$ LOW to $\overline{\text{BLS}}$ LOW time		–5	-	+5	ns
t_{WELDV}	$\overline{\text{WE}}$ LOW to data valid time		–5	-	+5	ns
t_{CSLDV}	$\overline{\text{CS}}$ LOW to data valid time		–5	-	+5	ns
t_{WELWEH}	$\overline{\text{WE}}$ LOW to $\overline{\text{WE}}$ HIGH time	[2]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
$t_{BLSLBLSH}$	$\overline{\text{BLS}}$ LOW to $\overline{\text{BLS}}$ HIGH time	[2]	$T_{cy(CCLK)} \times (1 + WST2) - 5$	-	$T_{cy(CCLK)} \times (1 + WST2) + 5$	ns
t_{WEHANV}	$\overline{\text{WE}}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns
t_{WEHDNV}	$\overline{\text{WE}}$ HIGH to data invalid time	[2]	$(2 \times T_{cy(CCLK)}) - 5$	-	$(2 \times T_{cy(CCLK)}) + 5$	ns
$t_{BLSHANV}$	$\overline{\text{BLS}}$ HIGH to address invalid time	[2]	$T_{cy(CCLK)} - 5$	-	$T_{cy(CCLK)} + 5$	ns

9.1 Timing

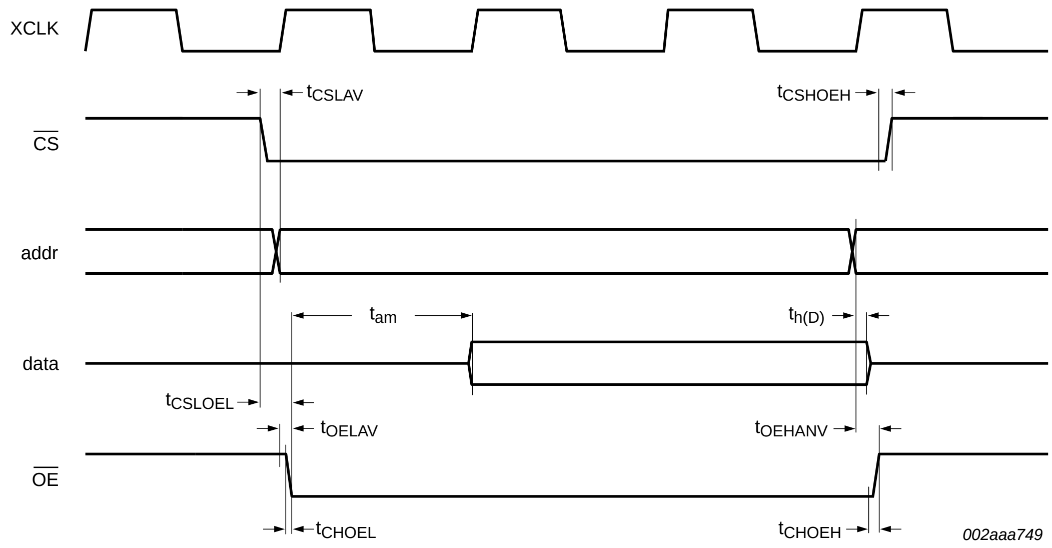


Fig 22. External memory read access

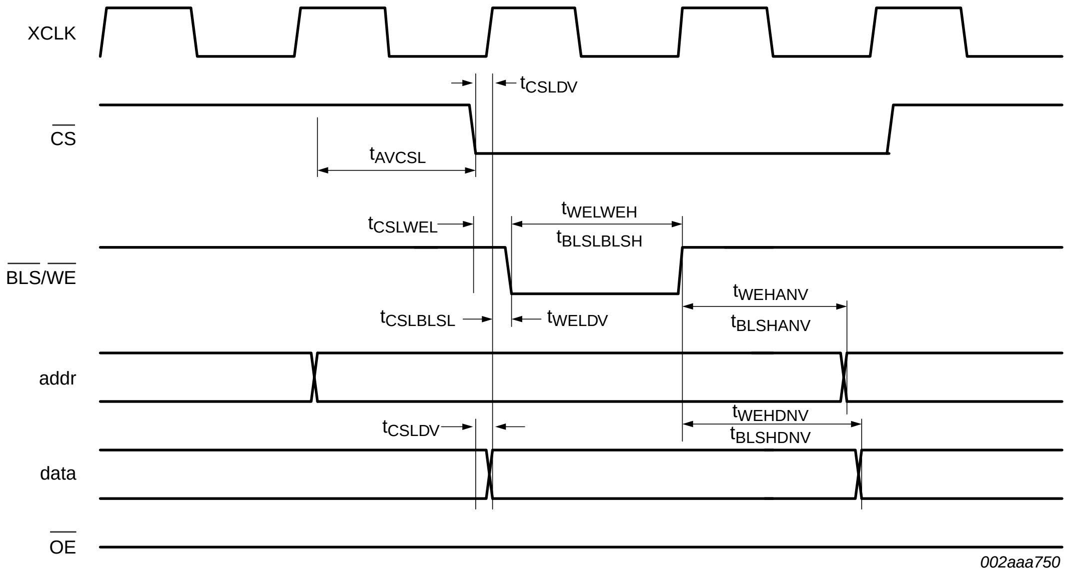


Fig 23. External memory write access

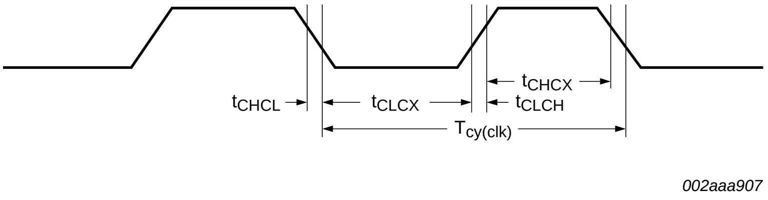
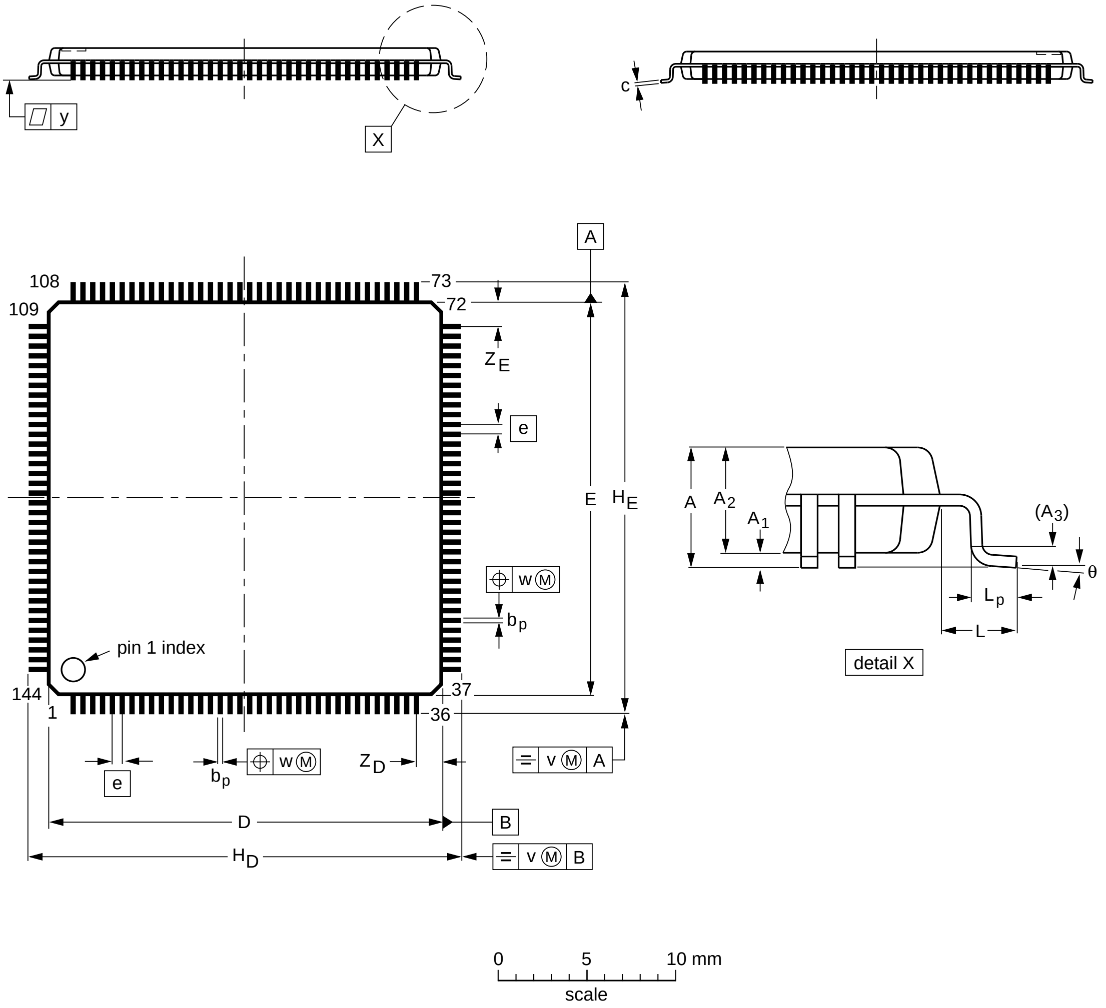


Fig 24. **External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)**

10. Package outline

LQFP144: plastic low profile quad flat package; 144 leads; body 20 x 20 x 1.4 mm **SOT486-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.15 0.05	1.45 1.35	0.25	0.27 0.17	0.20 0.09	20.1 19.9	20.1 19.9	0.5	22.15 21.85	22.15 21.85	1	0.75 0.45	0.2	0.08	0.08	1.4 1.1	1.4 1.1	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

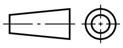
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT486-1	136E23	MS-026				~~00-03-14~~ 03-02-20

Fig 25. Package outline SOT486-1 (LQFP144)