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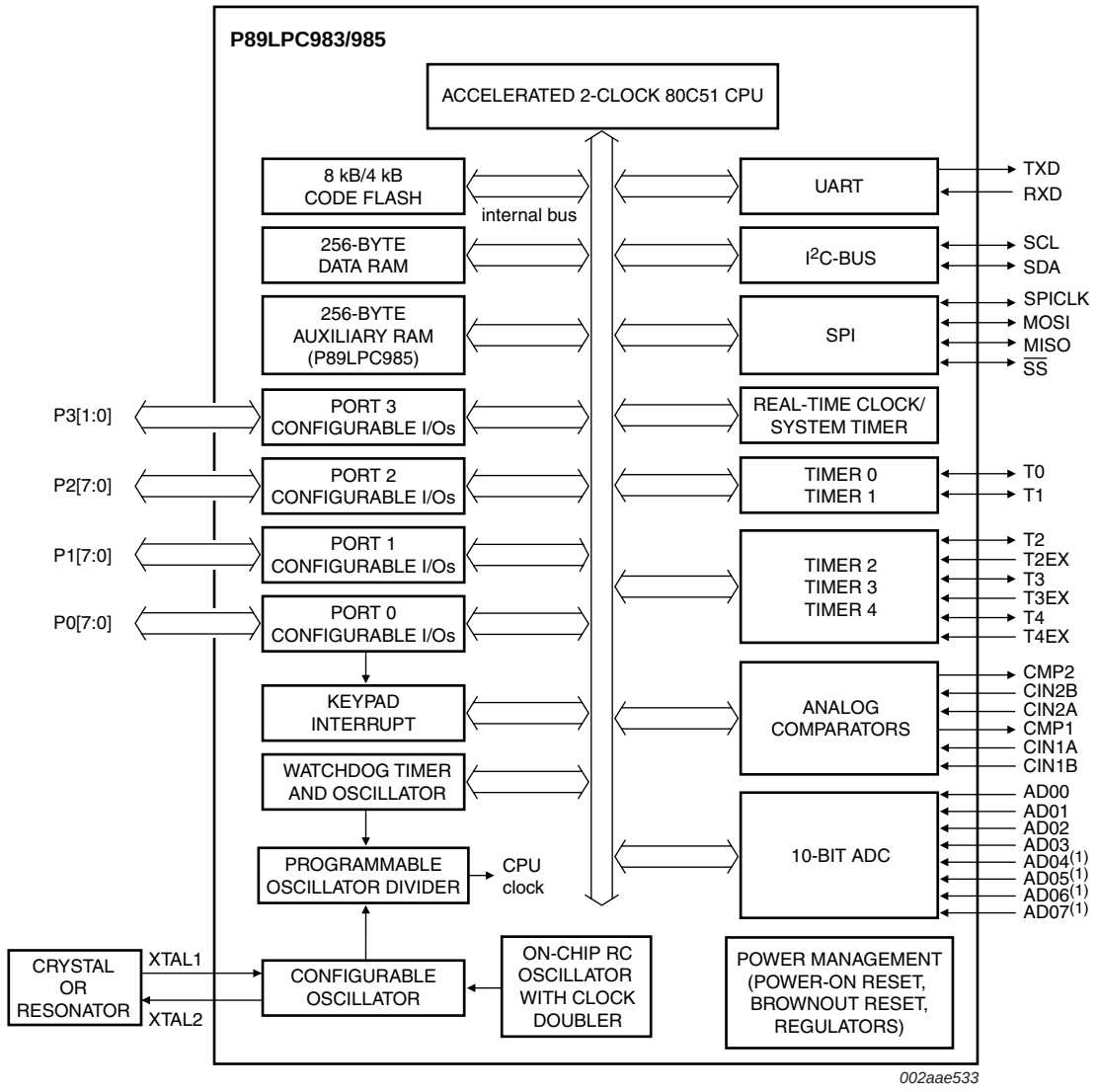
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc983fdh-529



(1) Only on the P89LPC985.

Fig 2. P89LPC983/985 block diagram

6. Pinning information

6.1 Pinning

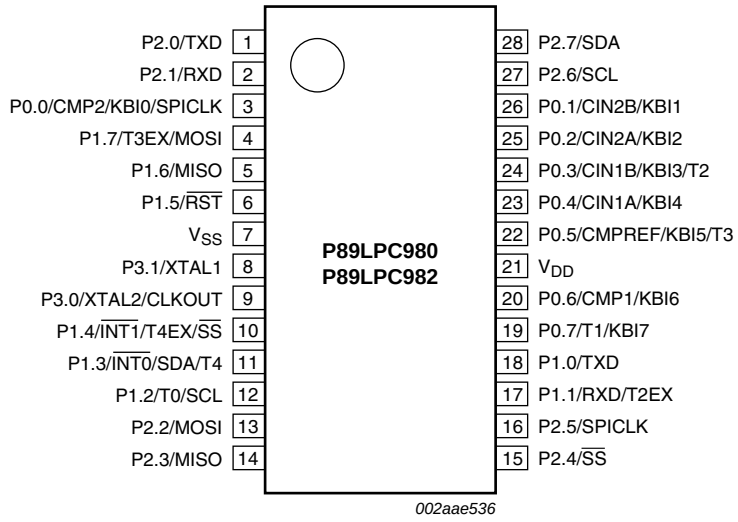


Fig 5. P89LPC980/982 TSSOP28 pin configuration

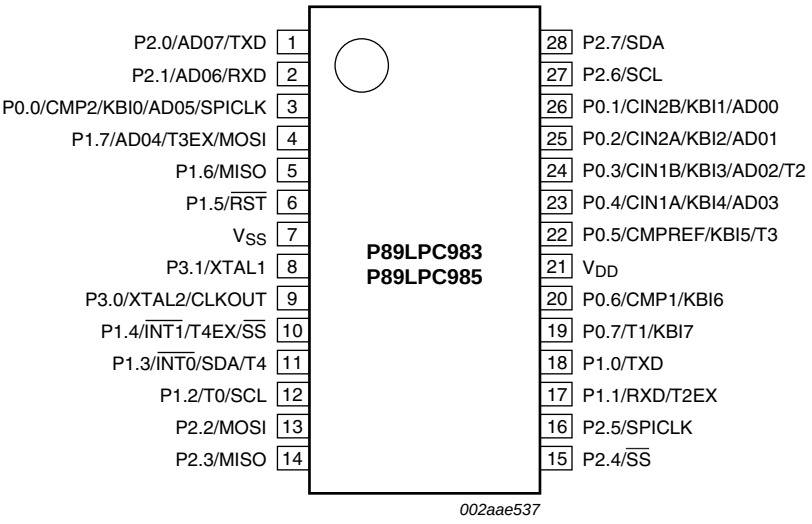


Fig 6. P89LPC983/985 TSSOP28 pin configuration

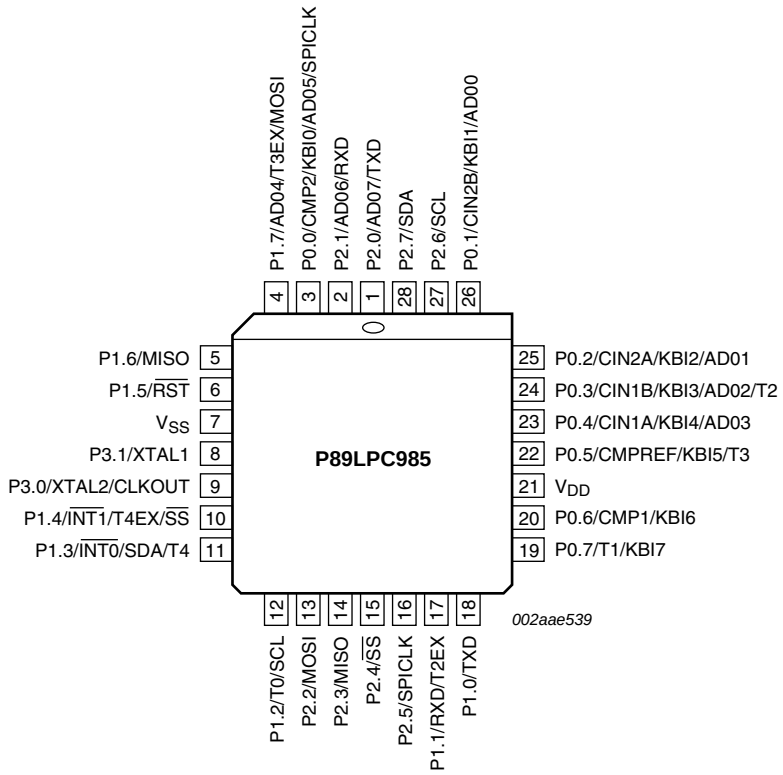


Fig 8. P89LPC985 PLCC28 pin configuration

Table 4. Special function registers - P89LPC980/982 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
IP1H	Interrupt priority 1 high	F7H	-	PSTH	-	PXTIMH	PSPIH	PCH	PKBIH	PI2CH	00[2]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[2]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register	93H									FF	1111 1111
	Bit address		**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7	CMP1 /KB6	CMPREF /KB5/T3	CIN1A /KB4	CIN1B /KB3/T2	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[2]	
	Bit address		**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	T3EX	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$/T4EX	$\overline{\text{INT0}}$/SDA/T4	T0/SCL	RXD/T2EX	TXD	[2]	
	Bit address		**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**		
P2*	Port 2	A0H	-	-	SPICLK	$\overline{\text{SS}}$	MISO	MOSI	-	-	[2]	
	Bit address		**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P3*	Port 3	B0H	-	-	-	-	-	-	XTAL1	XTAL2	[2]	
P0M1	Port 0 output mode 1	84H	(P0M1.7)	(P0M1.6)	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[2]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	(P0M2.6)	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[2]	0000 0000
P1M1	Port 1 output mode 1	91H	(P1M1.7)	(P1M1.6)	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[2]	11x1 xx11
P1M2	Port 1 output mode 2	92H	(P1M2.7)	(P1M2.6)	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[2]	00x0 xx00
P2M1	Port 2 output mode 1	A4H	(P2M1.7)	(P2M1.6)	(P2M1.5)	(P2M1.4)	(P2M1.3)	(P2M1.2)	(P2M1.1)	(P2M1.0)	FF[2]	1111 1111
P2M2	Port 2 output mode 2	A5H	(P2M2.7)	(P2M2.6)	(P2M2.5)	(P2M2.4)	(P2M2.3)	(P2M2.2)	(P2M2.1)	(P2M2.0)	00[2]	0000 0000

Table 4. Special function registers - P89LPC980/982 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	SPPD	SPD	-	00[2]	0000 0000
PINCON	Pin remap control register	CFH	-	-	-	-	-	UART	SPI	I2C	00[2]	0000 0000
PMUCON	Power Management Unit control register	FAH	LPMOD	-	-	-	-	-	-	HCOK		0xxx xxx1
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
PWMD2H	PWM Free Cycle Register 2 High Byte	AEH									00	0000 0000
PWMD2L	PWM Free Cycle Register 2 Low Byte	AFH									00	0000 0000
PWMD3H	PWM Free Cycle Register 3 High Byte	E9H									00	0000 0000
PWMD3L	PWM Free Cycle Register 3 Low Byte	EAH									00	0000 0000
PWMD4H	PWM Free Cycle Register 4 High Byte	AAH									00	0000 0000

Table 4. Special function registers - P89LPC980/982 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
T2CON	Timer/Counter 2 Control	FFH	PSEL2	ENT2	TIEN2	PWM2	EXEN2	TR2	C/NT2	CP/NRL2	00	0000 0000
TH2	Timer/Counter 2 High Byte	FEH									00	0000 0000
TL2	Timer/Counter 2 Low Byte	FDH									00	0000 0000
T3CON	Timer/Counter 3 Control	EFH	PSEL3	ENT3	TIEN3	PWM3	EXEN3	TR3	C/NT3	CP/NRL3	00	0000 0000
TH3	Timer/Counter 3 High Byte	EEH									00	0000 0000
TL3	Timer/Counter 3 Low Byte	EDH									00	0000 0000
T4CON	Timer/Counter 2 Control	CDH	PSEL4	ENT4	TIEN4	PWM4	EXEN4	TR4	C/NT4	CP/NRL4	00	0000 0000
TH4	Timer/Counter 4 High Byte	CCH									00	0000 0000

Table 6. Special function registers - P89LPC983/985 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C-bus slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C-bus control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C-bus data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C-bus status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	EXTIM	ESPI	EC	EKBI	EI2C	00[2]	00x0 0000

Table 7. Extended special function registers - P89LPC983/985[1]

Name	Description	SFR addr.	Bit functions and addresses		Reset value	
			MSB	LSB	Hex	Binary
AD0DAT0L	ADC0 data register 0, left (MSB)	FFFFH	AD0DAT0 [9:2]		00	0000 0000
AD0DAT0R	ADC0 data register 0, right (LSB)	FFFEH	AD0DAT0 [7:0]		00	0000 0000
AD0DAT1L	ADC0 data register 1, left (MSB)	FFFDH	AD0DAT1 [9:2]		00	0000 0000
AD0DAT1R	ADC0 data register 1, right (LSB)	FFFCH	AD0DAT1 [7:0]		00	0000 0000
AD0DAT2L	ADC0 data register 2, left (MSB)	FFFBH	AD0DAT2 [9:2]		00	0000 0000
AD0DAT2R	ADC0 data register 2, right (LSB)	FFFAH	AD0DAT2 [7:0]		00	0000 0000
AD0DAT3L	ADC0 data register 3, left (MSB)	FFF9H	AD0DAT3 [9:2]		00	0000 0000
AD0DAT3R	ADC0 data register 3, right (LSB)	FFF8H	AD0DAT3 [7:0]		00	0000 0000
AD0DAT4L	ADC0 data register 4, left (MSB)	FFF7H	AD0DAT4 [9:2]		00	0000 0000
AD0DAT4R	ADC0 data register 4, right (LSB)	FFF6H	AD0DAT4 [7:0]		00	0000 0000
AD0DAT5L	ADC0 data register 5, left (MSB)	FFF5H	AD0DAT5 [9:2]		00	0000 0000
AD0DAT5R	ADC0 data register 5, right (LSB)	FFF4H	AD0DAT5 [7:0]		00	0000 0000

7.5 Clock output

The P89LPC980/982/983/985 supports a user-selectable clock output function on the P3.0/XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC980/982/983/985. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC980/982/983/985 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz $\pm$ 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

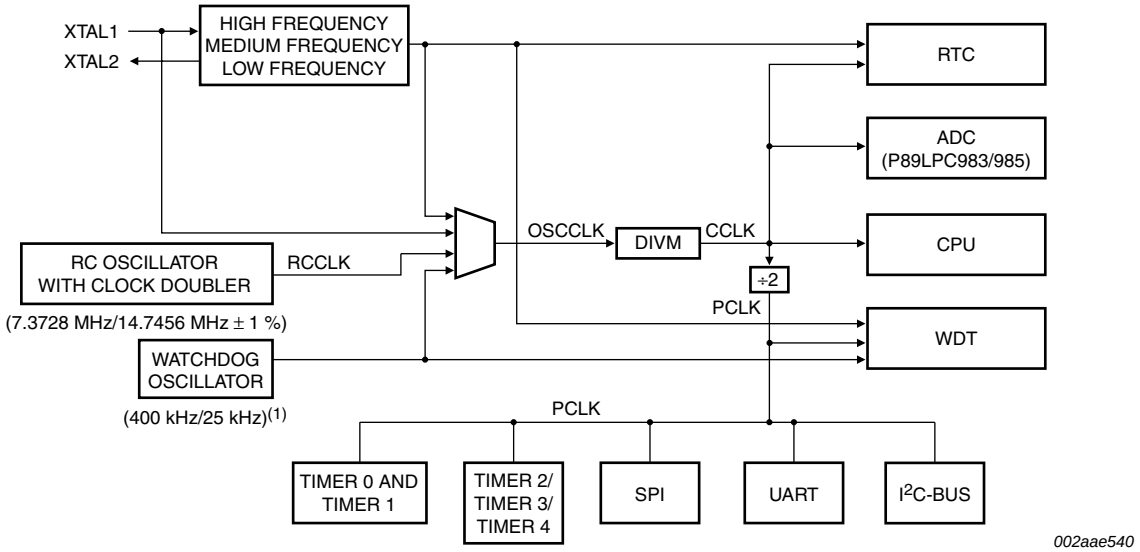
The watchdog has a separate oscillator which provides two options: 400 kHz and 25 kHz. It is calibrated to $\pm$10 % at 400 kHz. The oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2/CLKOUT pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock source switching on the fly

P89LPC980/982/983/985 can implement clock switching on any sources of watchdog oscillator, 7 MHz/14 MHz internal RC oscillator, crystal oscillator and external clock input during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is ‘0’, writing to CLKCON register is not allowed.



(1) ±10 % at 400 kHz.

Fig 9. Block diagram of oscillator control

7.10 CCLK wake-up delay

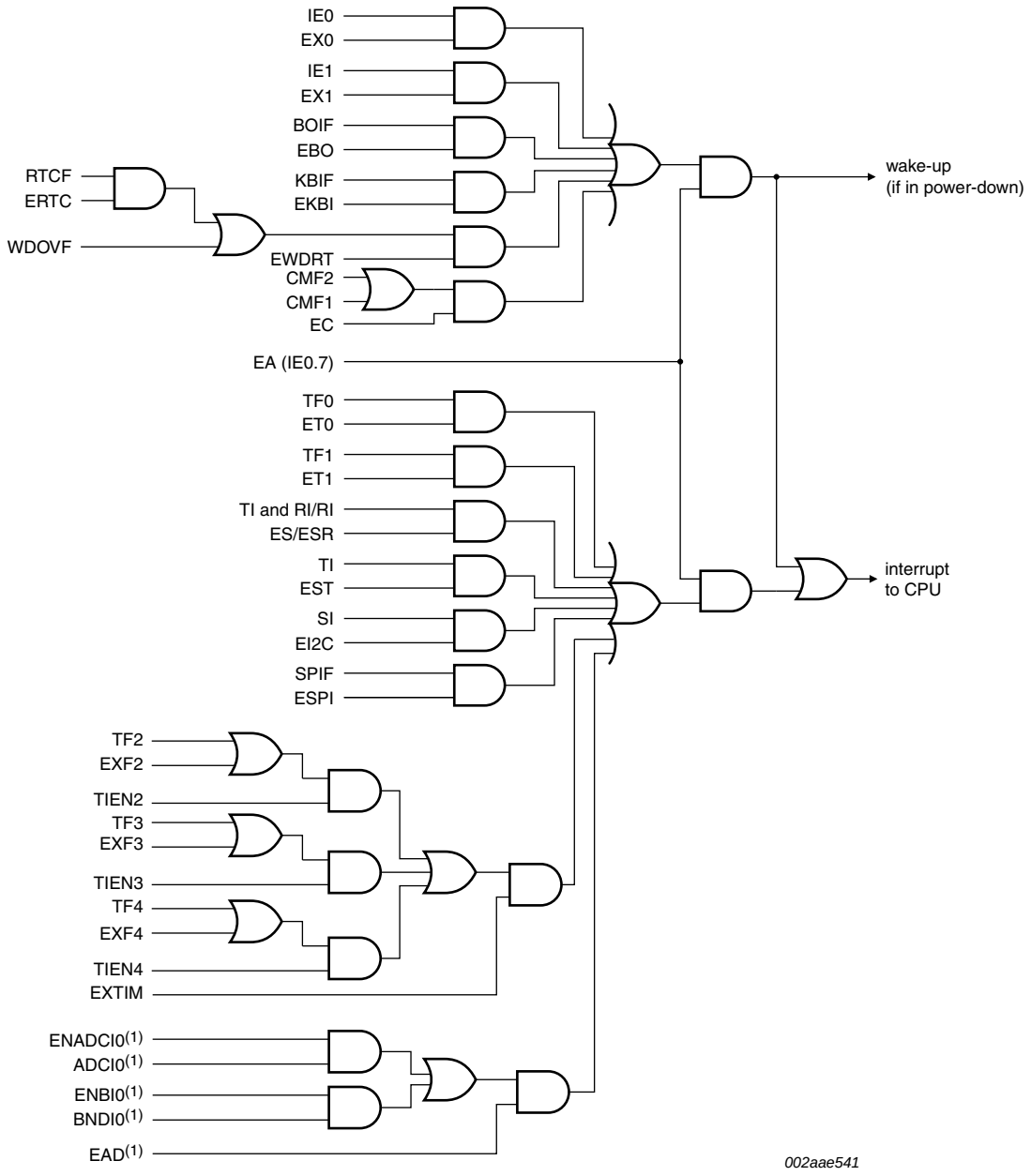
The P89LPC980/982/983/985 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μs to 100 μs. If the clock source is the internal RC oscillator, the delay is 200 μs to 300 μs. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.11 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.12 Low power select

The P89LPC980/982/983/985 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.



(1) P89LPC983/985.

Fig 10. Interrupt sources, interrupt enables, and power-down wake-up sources

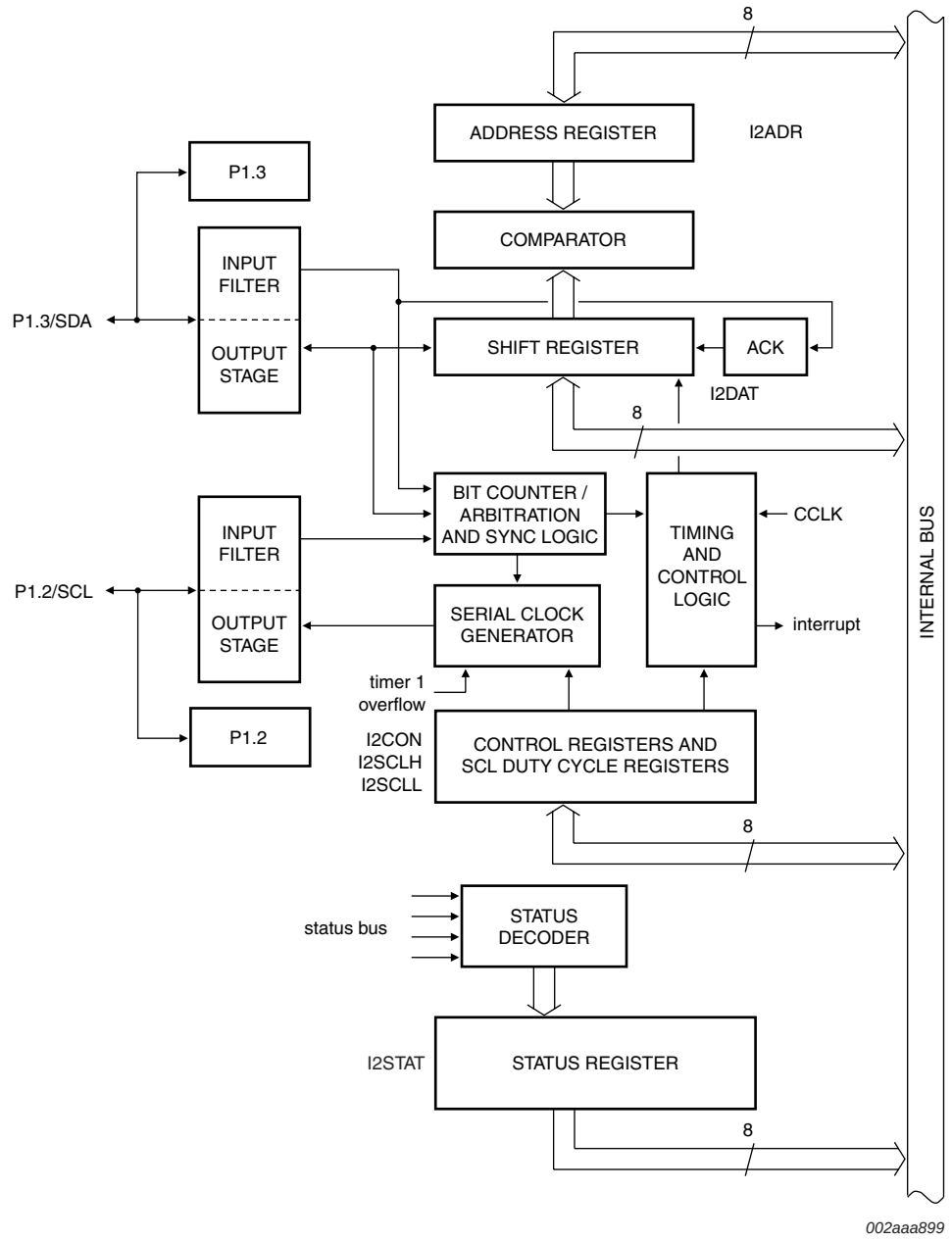


Fig 13. I²C-bus serial interface block diagram

7.26 KBI

The Keypad Interrupt function (KBI) is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The port can be configured via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in P87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.27 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler can be the PCLK, the nominal 400 kHz/25 kHz watchdog oscillator or low speed crystal oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 19 shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the *P89LPC980/982/983/985 User manual* for more details.

8.6 Boundary limits interrupt

The ADC has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt criteria, the boundary limits will again be compared after all 8 MSBs have been converted. A boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.7 Clock divider

The ADC requires that its internal clock source be in the range of 500 kHz to 6.6 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.8 Power-down and Idle mode

In Idle mode the ADC, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the ADC does not function. If the ADC is enabled, they will consume power. Power can be reduced by disabling the ADC.

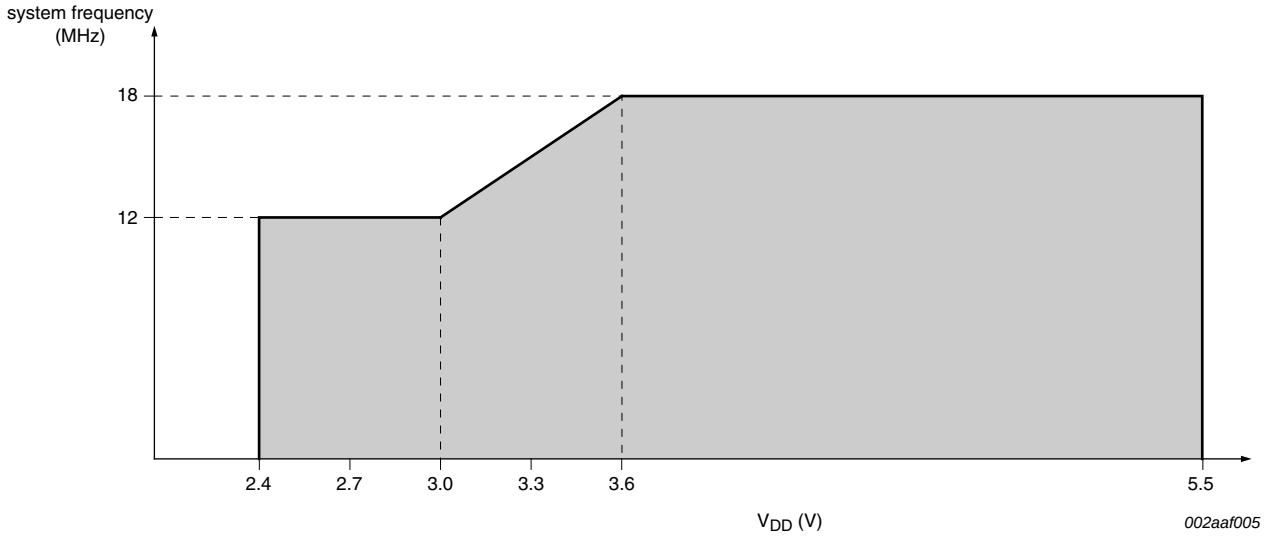


Fig 21. Frequency vs. supply voltage

10. Static characteristics

Table 13. Static characteristics

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	5	6	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	9	10	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	7	8	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	10	11	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	8	9	mA
		f_{osc} = 18 MHz, high speed mode of regulators	[2]	-	11	12	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	3.5	4.5	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	3	4	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	5	6	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	4	5	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	4	5	mA
		f_{osc} = 18 MHz, high speed mode of regulators	[2]	-	6.5	7.5	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 2.4 V; voltage comparators powered down	[3]	-	28	35	μA
		V_{DD} = 3.3 V; voltage comparators powered down	[3]	-	32	40	μA
		V_{DD} = 5.5 V; voltage comparators powered down	[3]	-	38	45	μA

Table 14. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
T_{SPICYC}	SPI cycle time	see Figure 24, 25, 26, 27					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 26, 27					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 26, 27					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 24, 25, 26, 27	100	-	100	-	ns
	master or slave						
t_{SPIDH}	SPI data hold time	see Figure 24, 25, 26, 27	100	-	100	-	ns
	master or slave						
t_{SPIA}	SPI access time	see Figure 26, 27					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 26, 27					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

14. Abbreviations

Table 19. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
BOD	BrownOut Detect
CPU	Central Processing Unit
CCU	Capture/Compare Unit
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
GPIO	General Purpose Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
WDT	WatchDog Timer

15. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC980_982_983_985 v.4	20100615	Product data sheet	-	P89LPC980_982_983_985_3
Modifications:	• Section 7.4 “Crystal oscillator option” on page 33: Updated text. • Section 7.27 “Watchdog timer” on page 54: Updated text.			
P89LPC980_982_983_985_3	20100518	Product data sheet	-	P89LPC980_982_983_985_2
Modifications:	• Changed data sheet status to ‘Product data sheet’. • Table 13 “Static characteristics”: Updated Min/Typ/Max values for BOD interrupt and BOD reset. • Table 13 “Static characteristics”: Updated conditions and Min/Max/Unit values for $(dV/dt)_r$.			
P89LPC980_982_983_985_2	20100208	Preliminary data sheet	-	P89LPC980_982_1
Modifications:	• Added P89LPC983 and P89LPC985 devices. • Table 12 “Limiting values”: Updated V_{ESD} min/max. • Table 13 “Static characteristics”: Updated $I_{DD(oper)}$ and $I_{DD(idle)}$.			
P89LPC980_982_1	20091113	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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