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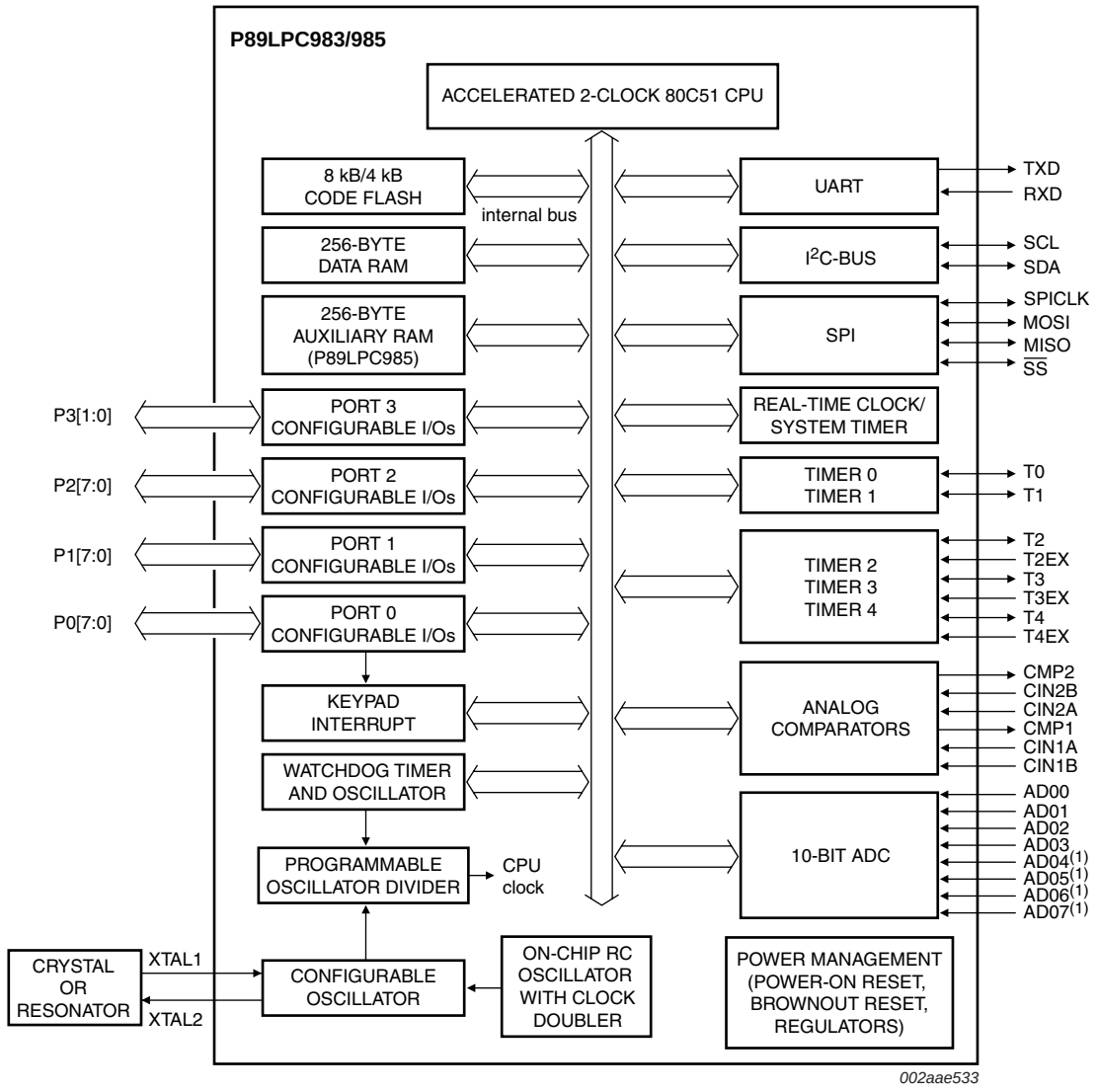
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-LCC (J-Lead)
Supplier Device Package	28-PLCC (11.48x11.48)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc985fa-529



(1) Only on the P89LPC985.

Fig 2. P89LPC983/985 block diagram

7. Functional description

Remark: Please refer to the P89LPC980/982/983/985 *User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers - P89LPC980/982

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[1]	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1[1]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[1]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[2]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[2]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000

Table 4. Special function registers - P89LPC980/982 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
P3M1	Port 3 output mode 1	B1H	-	-	-	-	-	-	(P3M1.1)	(P3M1.0)	03[2]	xxxx xx11
P3M2	Port 3 output mode 2	B2H	-	-	-	-	-	-	(P3M2.1)	(P3M2.0)	00[2]	xxxx xx00
PCON	Power control register	87H	SMOD1	SMOD0	-	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	-	I2PD	SPPD	SPD	-	00[2]	0000 0000
PINCON	Pin remap control register	CFH	-	-	-	-	-	UART	SPI	I2C	00[2]	0000 0000
PMUCON	Power Management Unit control register	FAH	LPMOD	-	-	-	-	-	-	HCOK		0xxx xxx1
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
PWMD2H	PWM Free Cycle Register 2 High Byte	AEH									00	0000 0000
PWMD2L	PWM Free Cycle Register 2 Low Byte	AFH									00	0000 0000
PWMD3H	PWM Free Cycle Register 3 High Byte	E9H									00	0000 0000
PWMD3L	PWM Free Cycle Register 3 Low Byte	EAH									00	0000 0000
PWMD4H	PWM Free Cycle Register 4 High Byte	AAH									00	0000 0000

Table 6. Special function registers - P89LPC983/985 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
PWMD3L	PWM Free Cycle Register 3 Low Byte	EAH									00	0000 0000
PWMD4H	PWM Free Cycle Register 4 High Byte	AAH									00	0000 0000
PWMD4L	PWM Free Cycle Register 4 Low Byte	ABH									00	0000 0000
RCAP2H	Capture Register 2 High Byte	FCH									00	0000 0000
RCAP2L	Capture Register 2 Low Byte	FBH									00	0000 0000
RCAP3H	Capture Register 3 High Byte	ECH									00	0000 0000
RCAP3L	Capture Register 3 Low Byte	EBH									00	0000 0000
RCAP4H	Capture Register 4 High Byte	CAH									00	0000 0000
RCAP4L	Capture Register 4 Low Byte	C9H									00	0000 0000
RSTSRC	Reset source register	DFH	-	BOIF	BORF	POF	R_KB	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][4]	011x xx00
RTCH	RTC register high	D2H									00[4]	0000 0000
RTCL	RTC register low	D3H									00[4]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000

Table 7. Extended special function registers - P89LPC983/985[1] *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3H	AD0DAT6 [9:2]								00	0000 0000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2H	AD0DAT6 [7:0]								00	0000 0000
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7 [9:2]								00	0000 0000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0H	AD0DAT7 [7:0]								00	0000 0000
ADC0HBND	ADC0 high boundary register	FFEFH									FF	1111 1111
ADC0LBND	ADC0 Low boundary register	FFEEH									00	0000 0000
BNDSTA0	ADC0 boundary status register	FFEDH	BST07	BST06	BST05	BST04	BST03	BST02	BST01	BST00		
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	BOICFG2	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	WDMOD	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	1000 xxxx

7.2 Enhanced CPU

The P89LPC980/982/983/985 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC980/982/983/985 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see Figure 9) and can also be optionally divided to a slower frequency (see Section 7.11 “CCLK modification: DIVM register”).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

7.3.2 CPU clock (OSCCLK)

The P89LPC980/982/983/985 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 Crystal oscillator option

The crystal oscillator option can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK and RTC. The low speed oscillator option can be the clock source of the WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.5 Clock output

The P89LPC980/982/983/985 supports a user-selectable clock output function on the P3.0/XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC980/982/983/985. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC980/982/983/985 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to 7.373 MHz $\pm$ 1 % at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG2.7 = 1), the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

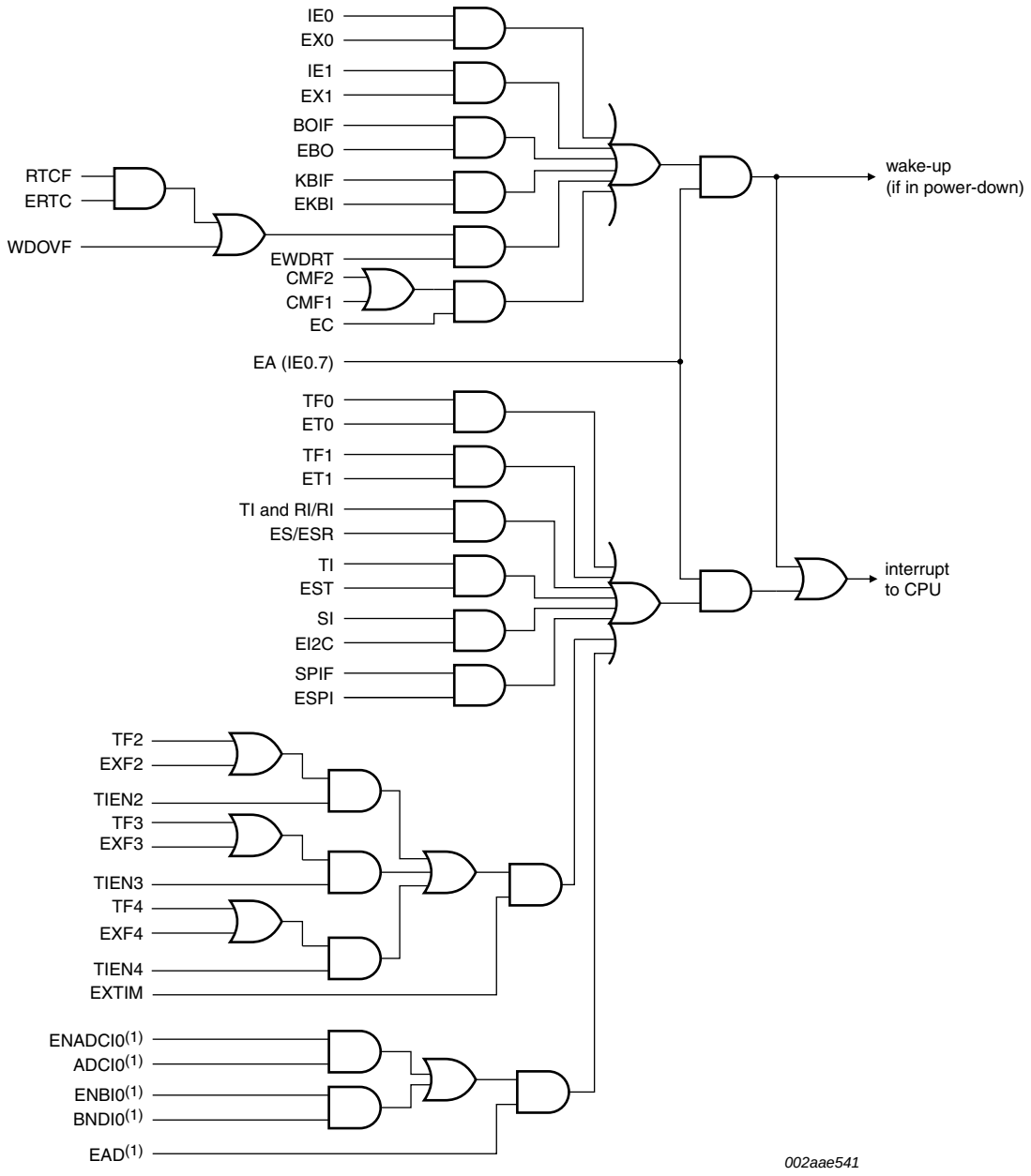
The watchdog has a separate oscillator which provides two options: 400 kHz and 25 kHz. It is calibrated to $\pm$10 % at 400 kHz. The oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2/CLKOUT pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE0 to BOE2 bits (UCFG1[3:5]) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock source switching on the fly

P89LPC980/982/983/985 can implement clock switching on any sources of watchdog oscillator, 7 MHz/14 MHz internal RC oscillator, crystal oscillator and external clock input during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is ‘0’, writing to CLKCON register is not allowed.



(1) P89LPC983/985.

Fig 10. Interrupt sources, interrupt enables, and power-down wake-up sources

Please refer to P89LPC980/982/983/985 User manual for detail configurations.

Table 10. SPI/I2C/UART pin remap

Peripherals	Function	Primary pin out	Alternative pin out
SPI	SPICLK	P2.5	P0.0
	MOSI	P2.2	P1.7
	MISO	P2.3	P1.6
	$\overline{SS}$	P2.4	P1.4
I2C	SDA	P1.3	P2.7
	SCL	P1.2	P2.6
UART	TXD	P1.0	P2.0
	RXD	P1.1	P2.1

7.17 Power management

The P89LPC980/982/983/985 support a variety of power management features.

Power-on detect and brownout detect are designed to prevent incorrect operation during initial power-up and power loss or reduction during operation.

The P89LPC980/982/983/985 support three different power reduction modes: Idle mode, Power-down mode, and total Power-down mode. In addition, individual on-chip peripherals can be disabled to eliminate unnecessary dynamic power use in any peripherals that are not required for the application.

Integrated PMU automatically adjusts internal regulators to minimize power consumption during Idle mode, Power-down mode and total Power-down mode. In addition, the power consumption can be further reduced in Normal or Idle mode through configuring regulators mode according to the applications.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD flash.

These three functions are disabled in Power-down mode and Total Power-down mode. In Normal or Idle mode, BOD reset and BOD flash are always on and can not be disabled in software. BOD interrupt may be enabled or disabled in software.

BOD reset and BOD interrupt, each has 6 levels. BOE0 to BOE2 (UCFG1[3:5]) are used as trip point configuration bits of BOD reset. BOICFG0 to BOICFG2 in register BODCFG are used as trip point configuration bits of BOD interrupt.

BOD reset voltage should be lower than BOD interrupt trip point. BOD flash is used for flash programming/erase protection and has only 1 trip point at 2.4 V. Please refer to *P89LPC980/982/983/985 User manual* for detail configurations.

If brownout detection works, the brownout condition occurs when V_{DD} falls below the brownout falling trip voltage and is negated when V_{DD} rises above the brownout rising trip voltage.

7.24 SPI

The P89LPC980/982/983/985 provides another high-speed serial communication interface: the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master mode or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

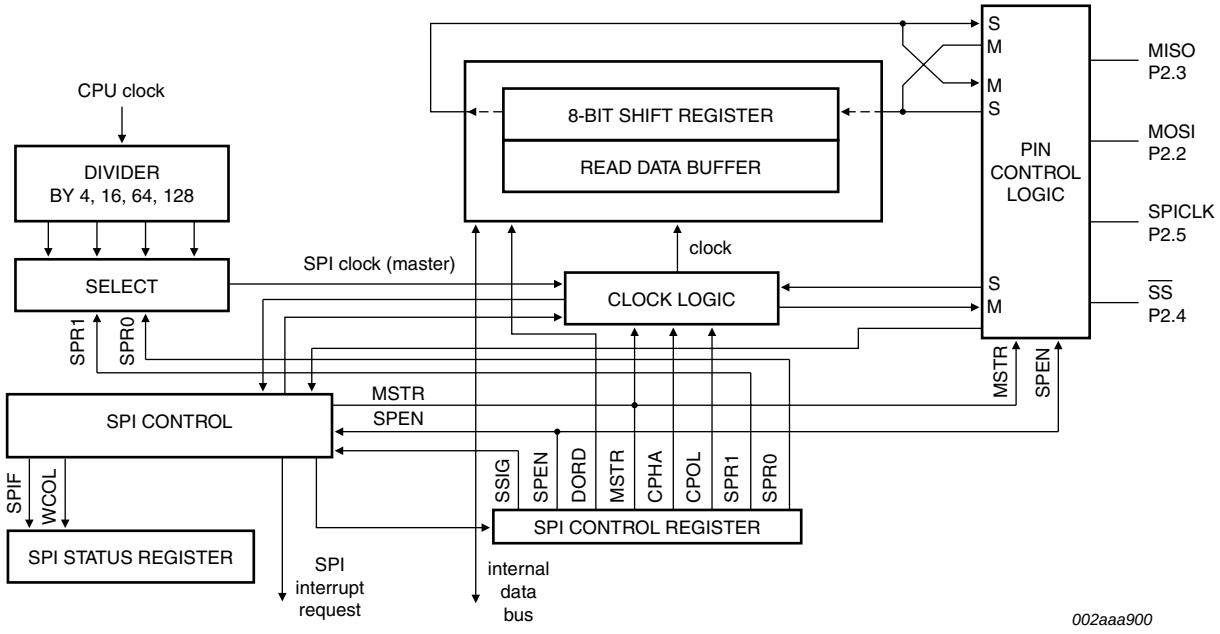


Fig 14. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 15 through Figure 17.

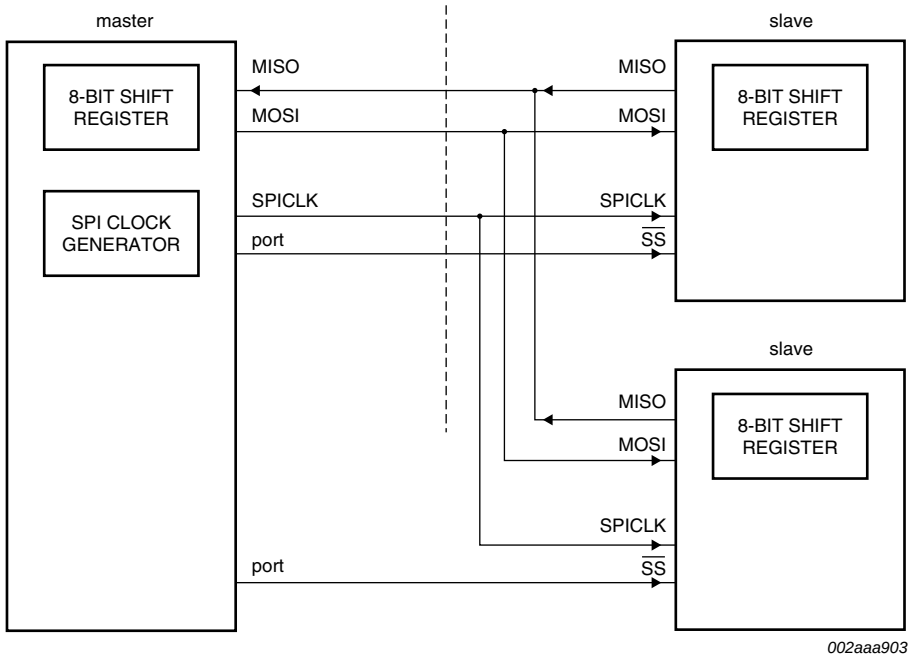


Fig 17. SPI single master multiple slaves configuration

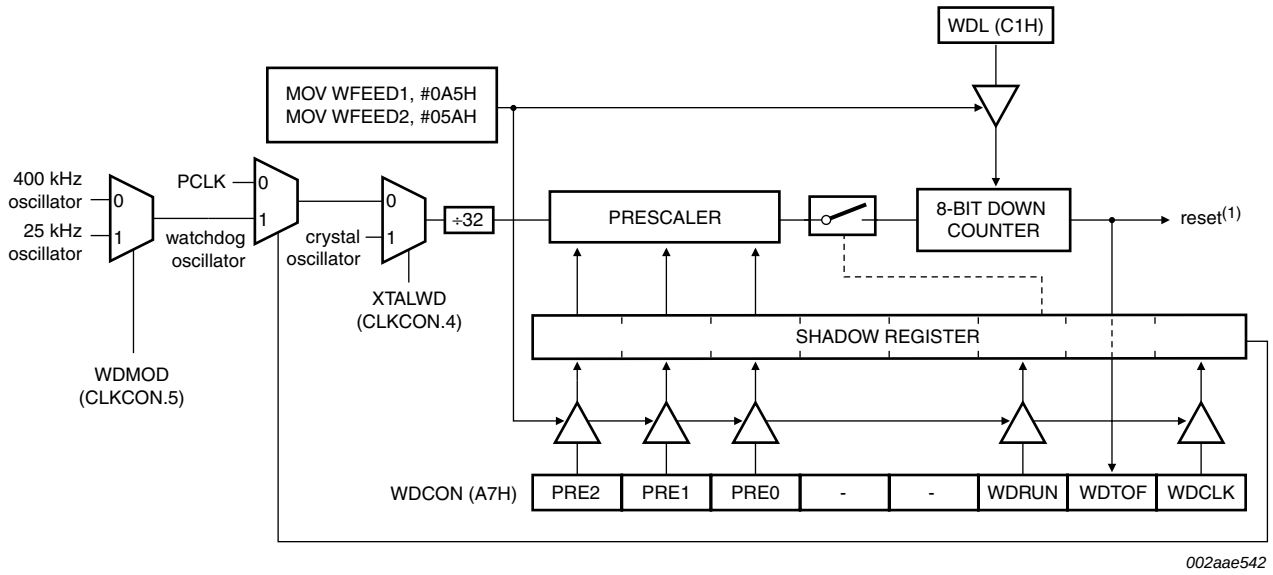
7.25 Analog comparators

Two analog comparators are provided on the P89LPC980/982/983/985. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable pins) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The overall connections to both comparators are shown in Figure 18. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μs. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COn, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFn. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFn, after disabling the comparator.



(1) Watchdog reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 19. Watchdog timer in Watchdog mode (WDTE = 1)

7.28 Additional features

7.28.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.28.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29 Flash program memory

7.29.1 General description

The P89LPC980/982/983/985 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC980/982/983/985 flash reliably stores memory contents even after 100000 erase and program cycles. The cell is designed to

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this bootloader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom bootloader can be written with the Boot Vector set to the custom bootloader, if desired.

Table 11. Default boot vector values and ISP entry points

Device	Default boot vector	Default bootloader entry point	Default bootloader code range	1 kB sector range
P89LPC980	0FH	0F00H	0E00H to 0FFFH	0C00H to 0FFFH
P89LPC982	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH
P89LPC983	0FH	0F00H	0E00H to 0FFFH	0C00H to 0FFFH
P89LPC985	1FH	1F00H	1E00H to 1FFFH	1C00H to 1FFFH

7.29.10 Hardware activation of the bootloader

The bootloader can also be executed by forcing the device into ISP mode during a power-on sequence (see the *P89LPC980/982/983/985 User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot is changed, it will no longer point to the factory pre-programmed ISP bootloader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.30 User configuration bytes

Some user-configurable features of the P89LPC980/982/983/985 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the *P89LPC980/982/983/985 User Manual* for additional details.

7.31 User sector security bytes

There are four/eight User Sector Security Bytes on the P89LPC980/982/983/985. Each byte corresponds to one sector. Please see the *P89LPC980/982/983/985 User manual* for additional details.

8. ADC (P89LPC983/985)

8.1 General description

The P89LPC985 has a 10-bit, 8-channel multiplexed successive approximation analog-to-digital converter modules. The P89LPC983 has a 10-bit, 4-channel multiplexed successive approximation analog-to-digital converter modules. A block diagram of the ADC is shown in Figure 20 "ADC block diagram".

8.4.4 Auto scan, continuous conversion mode

Any combination of the eight input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.

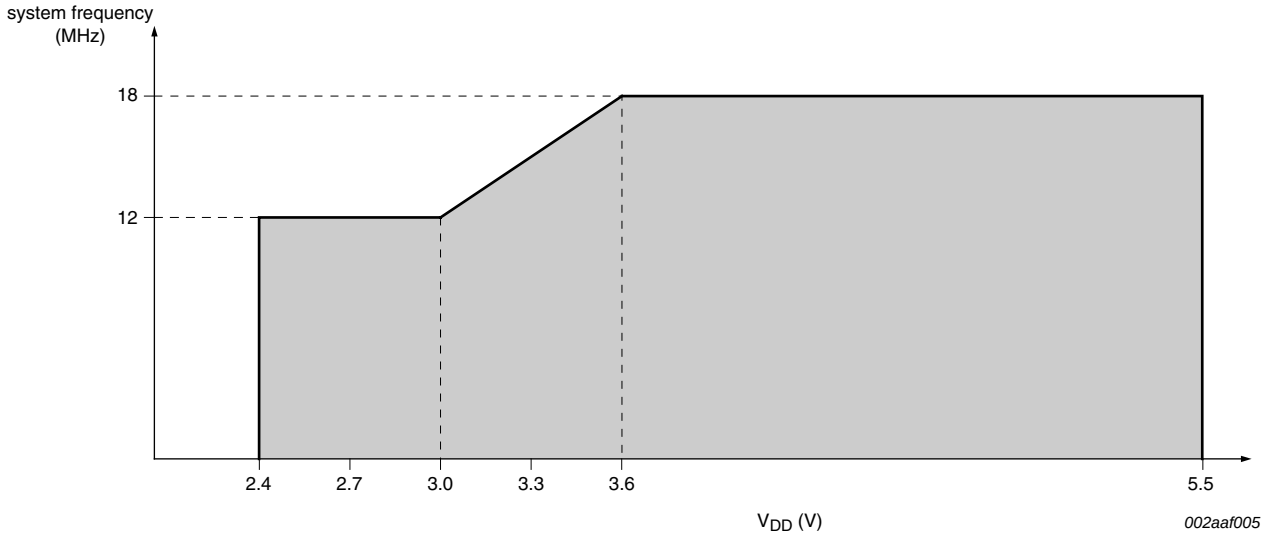


Fig 21. Frequency vs. supply voltage

10. Static characteristics

Table 13. Static characteristics

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	5	6	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	9	10	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	7	8	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	10	11	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	8	9	mA
		f_{osc} = 18 MHz, high speed mode of regulators	[2]	-	11	12	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 2.4 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	3.5	4.5	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	3	4	mA
		V_{DD} = 3.3 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	5	6	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	4	5	mA
		V_{DD} = 5.5 V					
		f_{osc} = 12 MHz, high speed mode of regulators	[2]	-	6	7	mA
		f_{osc} = 12 MHz, low current mode of regulators	[2]	-	4	5	mA
		f_{osc} = 18 MHz, high speed mode of regulators	[2]	-	6.5	7.5	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 2.4 V; voltage comparators powered down	[3]	-	28	35	μA
		V_{DD} = 3.3 V; voltage comparators powered down	[3]	-	32	40	μA
		V_{DD} = 5.5 V; voltage comparators powered down	[3]	-	38	45	μA

Table 13. Static characteristics *…continued*
V_{DD} = 2.4 V to 5.5 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
BOD reset						
V_{trip}	trip voltage	falling stage				
		BOE2, BOE1, BOE0 = 010	2.15	-	2.35	V
		BOE2, BOE1, BOE0 = 011	2.45	-	2.65	V
		BOE2, BOE1, BOE0 = 100	2.75	-	2.95	V
		BOE2, BOE1, BOE0 = 101	3.05	-	3.25	V
		BOE2, BOE1, BOE0 = 110	3.75	-	3.95	V
		BOE2, BOE1, BOE0 = 111	3.95	-	4.15	V
		rising stage				
		BOE2, BOE1, BOE0 = 010	2.30	-	2.50	V
		BOE2, BOE1, BOE0 = 011	2.60	-	2.80	V
		BOE2, BOE1, BOE0 = 100	2.90	-	3.10	V
		BOE2, BOE1, BOE0 = 101	3.20	-	3.40	V
		BOE2, BOE1, BOE0 = 110	3.85	-	4.05	V
		BOE2, BOE1, BOE0 = 111	4.05	-	4.25	V
BOD flash						
V_{trip}	trip voltage	falling stage	2.30	-	2.55	V
		rising stage	2.40	-	2.65	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$ and $I_{DD(idle)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(pd)}$ and $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 9 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 14. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 5.5 V unless otherwise specified.

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1][2]

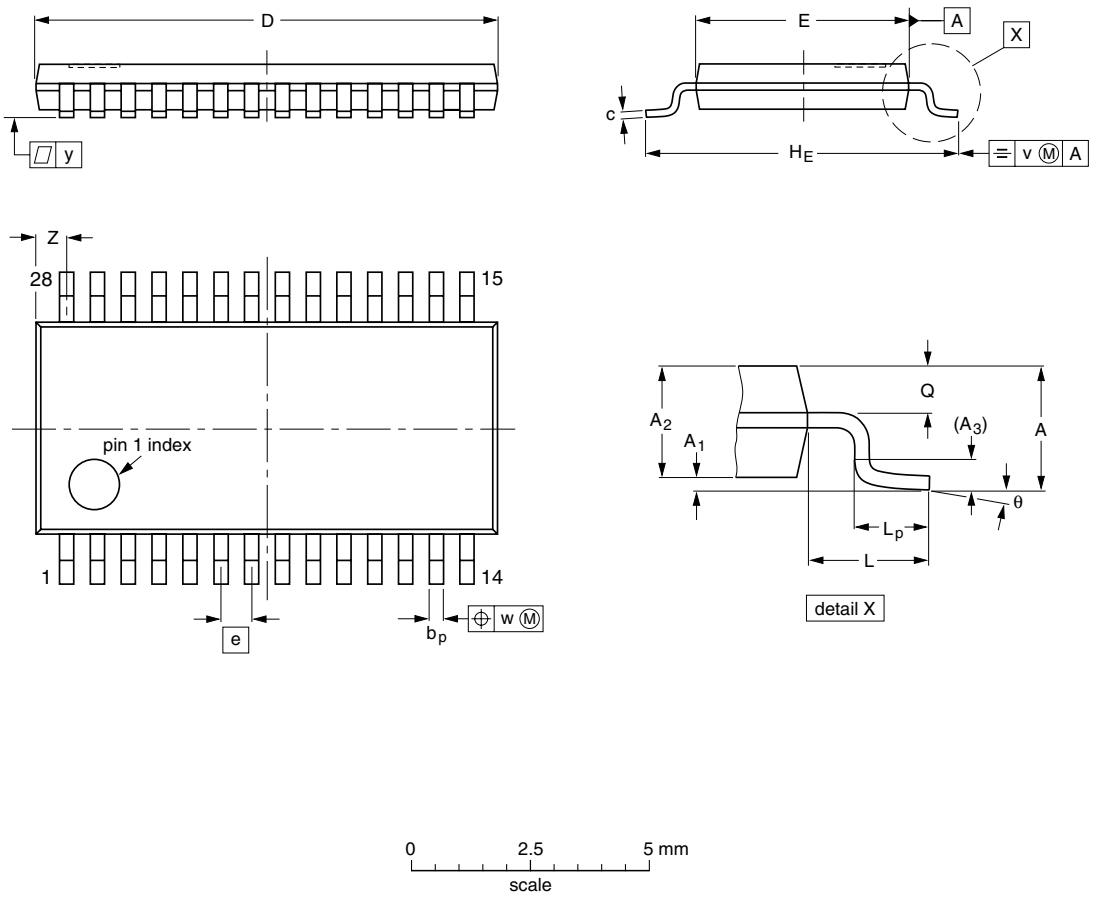
Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
T_{SPICYC}	SPI cycle time	see Figure 24, 25, 26, 27					
	slave		$^{6}/_{CCLK}$	-	500	-	ns
	master		$^{4}/_{CCLK}$	-	333	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 26, 27					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 26, 27					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 24, 25, 26, 27					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 24, 25, 26, 27					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 24, 25, 26, 27	100	-	100	-	ns
	master or slave						
t_{SPIDH}	SPI data hold time	see Figure 24, 25, 26, 27	100	-	100	-	ns
	master or slave						
t_{SPIA}	SPI access time	see Figure 26, 27					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 26, 27					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 24, 25, 26, 27					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 24, 25, 26, 27	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 24, 25, 26, 27					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

13. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 29. Package outline SOT361-1 (TSSOP28)