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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	28-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc985fdh-529

4. Block diagram

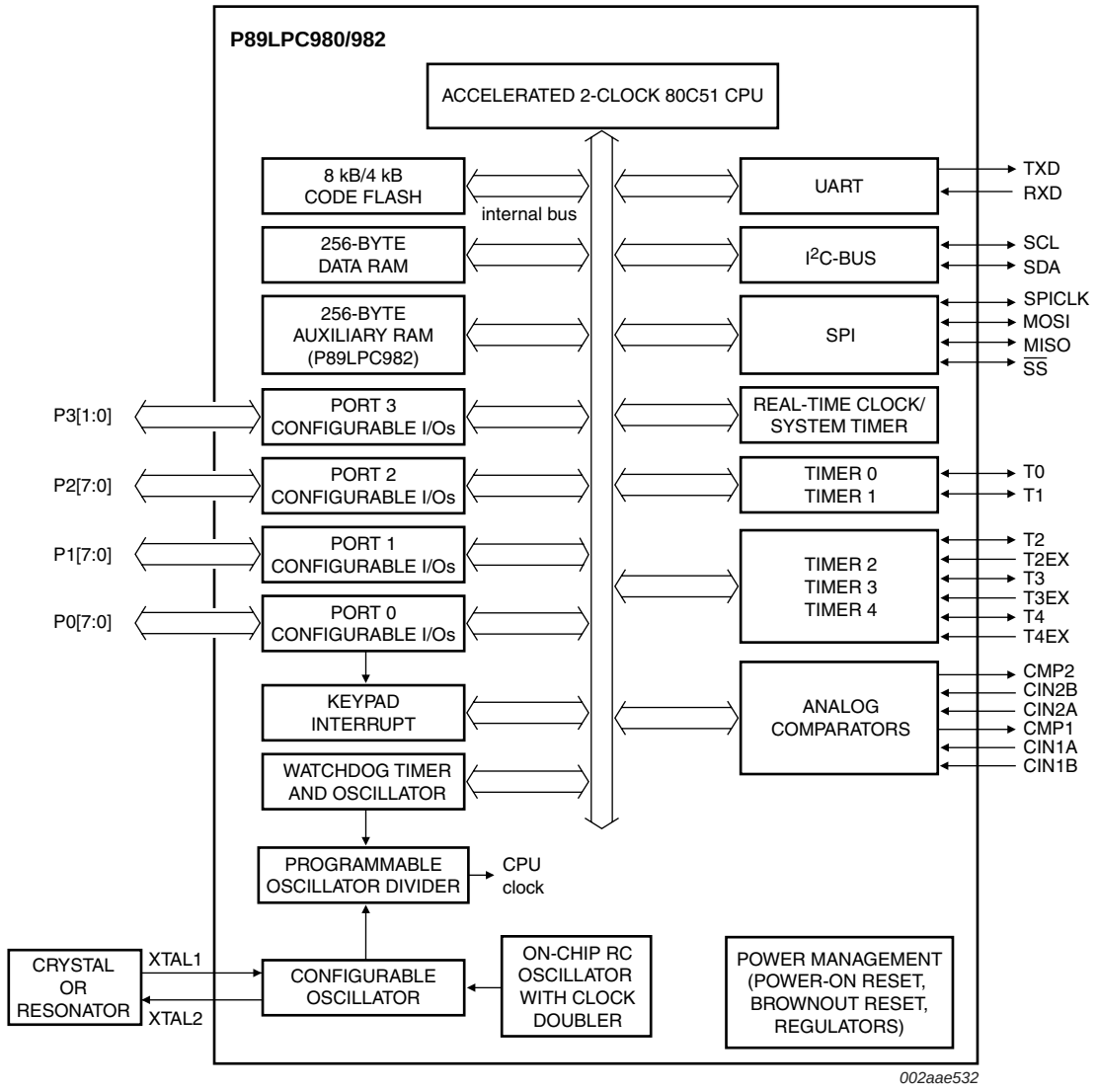


Fig 1. P89LPC980/982 block diagram

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
	PLCC28, TSSOP28		
P3.0/XTAL2/ CLKOUT	9	I/O	**P3.0 —** Port 3 bit 0.
		O	**XTAL2 —** Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration.
		O	**CLKOUT —** CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer.
P3.1/XTAL1	8	I/O	**P3.1 —** Port 3 bit 1.
		I	**XTAL1 —** Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, **and** if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer.
V_{SS}	7	I	**Ground:** 0 V reference.
V_{DD}	21	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

Table 4. Special function registers - P89LPC980/982 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
SPCTL	SPI control register	E2H	SSIG	SPEN	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	04	0000 0100
SPSTAT	SPI status register	E1H	SPIF	WCOL	-	-	-	-	-	-	00	00xx xxxx
SPDAT	SPI data register	E3H									00	0000 0000
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**	**88**		
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00	0000 0000
TH0	Timer 0 high	8CH									00	0000 0000
TH1	Timer 1 high	8DH									00	0000 0000
TL0	Timer 0 low	8AH									00	0000 0000
TL1	Timer 1 low	8BH									00	0000 0000
TMOD	Timer 0 and 1 mode	89H	T1GATE	T1C/T	T1M1	T1M0	T0GATE	T0C/T	T0M1	T0M0	00	0000 0000
T2CON	Timer/Counter 2 Control	FFH	PSEL2	ENT2	TIEN2	PWM2	EXEN2	TR2	C/NT2	CP/NRL2	00	0000 0000
TH2	Timer/Counter 2 High Byte	FEH									00	0000 0000
TL2	Timer/Counter 2 Low Byte	FDH									00	0000 0000
T3CON	Timer/Counter 3 Control	EFH	PSEL3	ENT3	TIEN3	PWM3	EXEN3	TR3	C/NT3	CP/NRL3	00	0000 0000
TH3	Timer/Counter 3 High Byte	EEH									00	0000 0000
TL3	Timer/Counter 3 Low Byte	EDH									00	0000 0000
T4CON	Timer/Counter 2 Control	CDH	PSEL4	ENT4	TIEN4	PWM4	EXEN4	TR4	C/NT4	CP/NRL4	00	0000 0000
TH4	Timer/Counter 4 High Byte	CCH									00	0000 0000

Table 6. Special function registers - P89LPC983/985

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
AD0CON	A/D control register 0	97H	ENBI0	ENADCI0	TMM10	EDGE0	ADCI0	ENADC0	ADCS01	ADCS00	00	0000 0000
AD0INS	A/D input select	A3H	AIN07	AIN06	AIN05	AIN04	AIN03	AIN02	AIN01	AIN00	00	0000 0000
AD0MODA	A/D mode register A	C0H	BNDI0	BURST0	SCC0	SCAN0	-	-	-	-	00	0000 0000
AD0MODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	INBND0	-	-	BSA0	FCIIS	00	000x 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0[1]	Baud rate generator 0 rate low	BEH									00	0000 0000
BRGR1[1]	Baud rate generator 0 rate high	BFH									00	0000 0000
BRGCON	Baud rate generator 0 control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[1]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	OE1	CO1	CMF1	00[2]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[2]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000

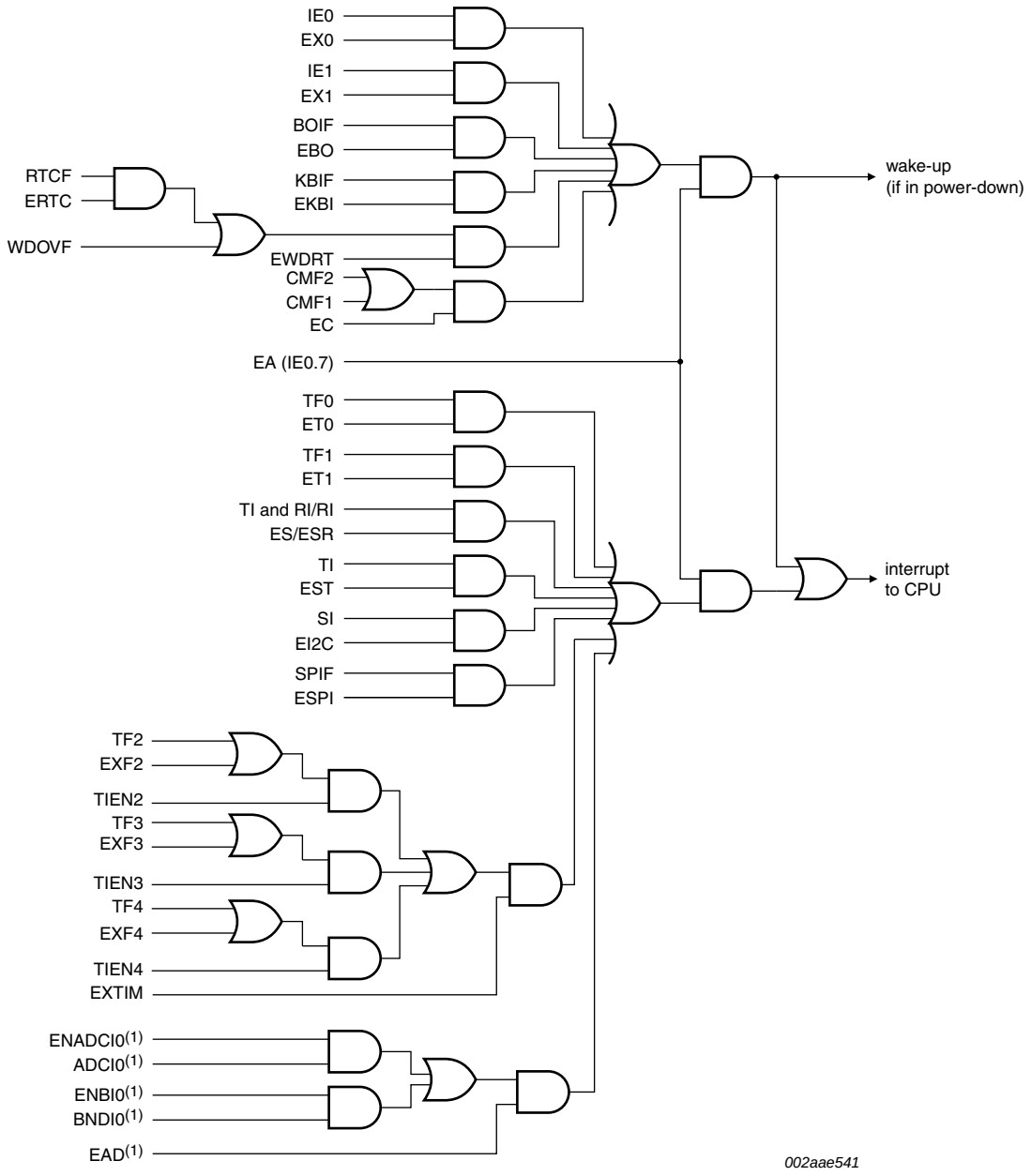
Table 6. Special function registers - P89LPC983/985 *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
PWMD3L	PWM Free Cycle Register 3 Low Byte	EAH									00	0000 0000
PWMD4H	PWM Free Cycle Register 4 High Byte	AAH									00	0000 0000
PWMD4L	PWM Free Cycle Register 4 Low Byte	ABH									00	0000 0000
RCAP2H	Capture Register 2 High Byte	FCH									00	0000 0000
RCAP2L	Capture Register 2 Low Byte	FBH									00	0000 0000
RCAP3H	Capture Register 3 High Byte	ECH									00	0000 0000
RCAP3L	Capture Register 3 Low Byte	EBH									00	0000 0000
RCAP4H	Capture Register 4 High Byte	CAH									00	0000 0000
RCAP4L	Capture Register 4 Low Byte	C9H									00	0000 0000
RSTSRC	Reset source register	DFH	-	BOIF	BORF	POF	R_KB	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[2][4]	011x xx00
RTCH	RTC register high	D2H									00[4]	0000 0000
RTCL	RTC register low	D3H									00[4]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000

Table 7. Extended special function registers - P89LPC983/985[1] *…continued*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
AD0DAT6L	ADC0 data register 6, left (MSB)	FFF3H	AD0DAT6 [9:2]								00	0000 0000
AD0DAT6R	ADC0 data register 6, right (LSB)	FFF2H	AD0DAT6 [7:0]								00	0000 0000
AD0DAT7L	ADC0 data register 7, left (MSB)	FFF1H	AD0DAT7 [9:2]								00	0000 0000
AD0DAT7R	ADC0 data register 7, right (LSB)	FFF0H	AD0DAT7 [7:0]								00	0000 0000
ADC0HBND	ADC0 high boundary register	FFEFH									FF	1111 1111
ADC0LBND	ADC0 Low boundary register	FFEEH									00	0000 0000
BNDSTA0	ADC0 boundary status register	FFEDH	BST07	BST06	BST05	BST04	BST03	BST02	BST01	BST00		
BODCFG	BOD configuration register	FFC8H	-	-	-	-	-	BOICFG2	BOICFG1	BOICFG0	[2]	
CLKCON	CLOCK Control register	FFDEH	CLKOK	-	WDMOD	XTALWD	CLKDBL	FOSC2	FOSC1	FOSC0	[3]	1000 xxxx



(1) P89LPC983/985.

Fig 10. Interrupt sources, interrupt enables, and power-down wake-up sources

7.16 I/O ports

The P89LPC980/982/983/985 has four I/O ports: Port 0, Port 1, Port 2 and Port 3. Ports 0, 1, and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in Table 9.

Table 9. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (28-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	26
	External $\overline{\text{RST}}$ pin supported	25
External clock input	No external reset (except during power-up)	25
	External $\overline{\text{RST}}$ pin supported	24
Low/medium/high speed oscillator (external crystal or resonator)	No external reset (except during power-up)	24
	External $\overline{\text{RST}}$ pin supported	23

7.16.1 Port configurations

All but three I/O port pins on the P89LPC980/982/983/985 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/$\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

7.16.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

or not. When switching back to high speed mode, first clear LPMOD bit to select high speed mode, then check HCOK bit. If HCOK bit turns to '1', it means the switch was completed.

7.18 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.18.1 Reset vector

Following reset, the P89LPC980/982/983/985 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see *P89LPC980/982/983/985 User manual*). Otherwise, instructions will be fetched from address 0000H.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding count input pin(T2/T3 /T4). In this function, the count input is sampled once during every machine cycle.

Only external Timer 2/3/4 has the external input pin TxEX (x = 2, 3 or 4). A 1-to-0 transition on this pin can trigger a reload or capture event.

Timers 2, 3 and 4 have three operating modes (Modes 0, 1 and 2).

7.20.1 Mode 0: 16-bit timer/counter with auto-reload

Mode 0 configures the timer register as an 16-bit Timer/counter with automatic reload. An overflow upon the timer or a 1-to-0 transition at TxEX pin can cause the reload event.

7.20.2 Mode 1: 16-bit timer/counter with input capture

Mode 1 configures the timer register as an 16-bit Timer/counter with input capture. A 1-to-0 transition at TxEX pin can cause the capture event.

7.20.3 Mode 2: 16-bit PWM mode

In this mode, the corresponding timer can be changed to a 16-bit PWM generator with adjustable duty cycle. In this mode, the corresponding timer can be changed to a 16-bit PWM generator with adjustable duty cycle and adjustable full period (from 0, theoretically, to 131072).

7.20.4 Timer overflow toggle output

Timers 2, 3 and 4 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T2, T3 and T4 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.21 RTC/system timer

The P89LPC980/982/983/985 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

7.22 UART

The P89LPC980/982/983/985 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC980/982/983/985 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection,

- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in Figure 12. The P89LPC980/982/983/985 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

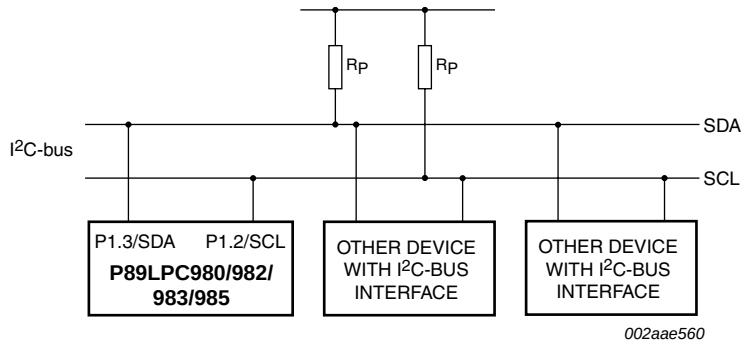


Fig 12. I²C-bus configuration

7.29.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC980/982/983/985 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application - using commercially available programmers - possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC980/982/983/985 User manual*.

7.29.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC980/982/983/985 User manual*.

7.29.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC980/982/983/985 through the serial port. This firmware is provided by NXP and embedded within each P89LPC980/982/983/985 device. The NXP ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD}, V_{SS}, TXD, RXD, and $\overline{RST}$). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.29.9 Power-on reset code execution

The P89LPC980/982/983/985 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC980/982/983/985 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 11 shows the factory default Boot Vector setting for these devices. A factory-provided bootloader is pre-programmed into the address space indicated and uses the indicated bootloader entry point to perform ISP functions. This code can be erased by the user.

8.4.4 Auto scan, continuous conversion mode

Any combination of the eight input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register pair which corresponds to the selected input channel. The user may select whether an interrupt, if enabled, will be generated after either the first four conversions have occurred or all selected channels have been converted. If the user selects to generate an interrupt after the four input channels have been converted, a second interrupt will be generated after the remaining input channels have been converted. After all selected channels have been converted, the process will repeat starting with the first selected channel. Additional conversion results will again cycle through the eight result register pairs, overwriting the previous results. Continuous conversions continue until terminated by the user.

8.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in the result register pair, AD0DAT0R and AD0DAT0L. The result of the conversion of the second channel is placed in result register pair, AD0DAT1R and AD0DAT1L. The first channel is again converted and its result stored in AD0DAT2R and AD0DAT2L. The second channel is again converted and its result placed in AD0DAT3R and AD0DAT3L. An interrupt is generated, if enabled, after every set of four or eight conversions (user selectable).

8.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the eight input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

8.5 Conversion start modes

8.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all ADC operating modes.

8.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all ADC operating modes.

8.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all ADC operating modes.

8.6 Boundary limits interrupt

The ADC has both a high and low boundary limit register. The user may select whether an interrupt is generated when the conversion result is within (or equal to) the high and low boundary limits or when the conversion result is outside the boundary limits. An interrupt will be generated, if enabled, if the result meets the selected interrupt criteria. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

An early detection mechanism exists when the interrupt criteria has been selected to be outside the boundary limits. In this case, after the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion meet the interrupt criteria (i.e., outside the boundary limits) an interrupt will be generated, if enabled. If the four MSBs do not meet the interrupt criteria, the boundary limits will again be compared after all 8 MSBs have been converted. A boundary status register (BNDSTA0) flags the channels which caused a boundary interrupt.

8.7 Clock divider

The ADC requires that its internal clock source be in the range of 500 kHz to 6.6 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

8.8 Power-down and Idle mode

In Idle mode the ADC, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the ADC does not function. If the ADC is enabled, they will consume power. Power can be reduced by disabling the ADC.

11.1 Waveforms

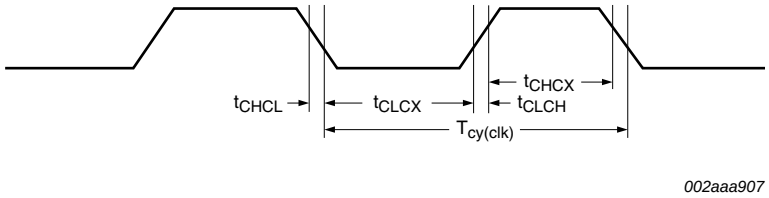


Fig 22. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

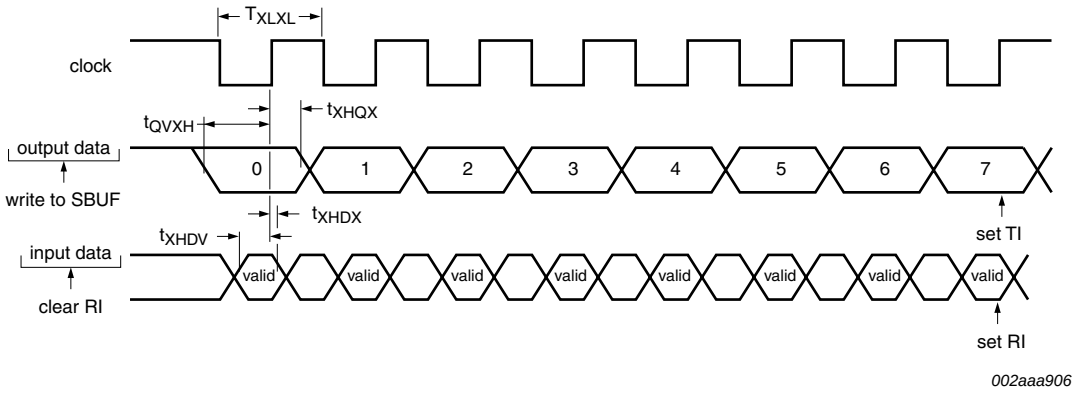


Fig 23. Shift register mode timing

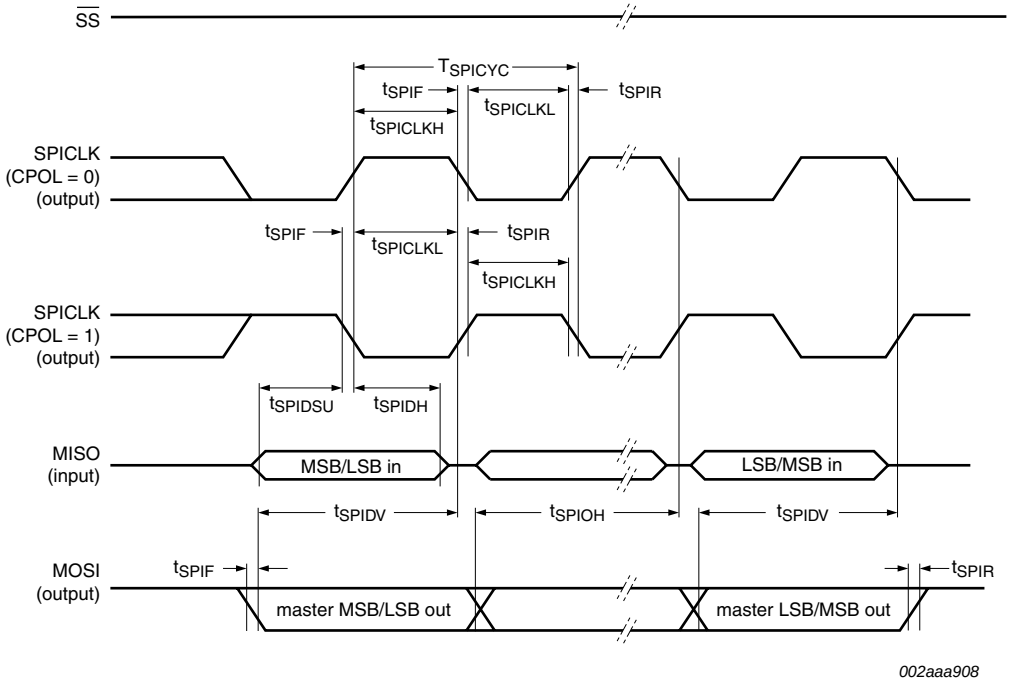
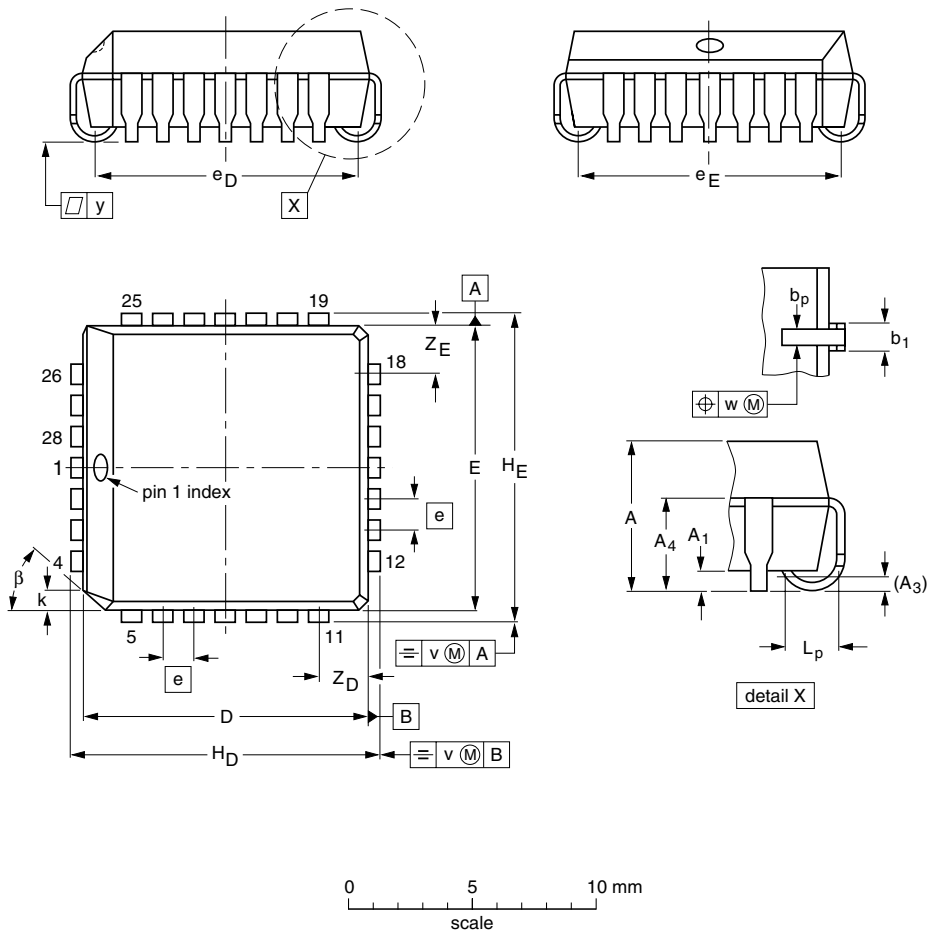


Fig 24. SPI master timing (CPHA = 0)

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (mm dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	1.44 1.02	0.18	0.18	0.1	2.16	2.16	45°
inches	0.180 0.165	0.02	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.43 0.39	0.43 0.39	0.495 0.485	0.495 0.485	0.048 0.042	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT261-2	112E08	MS-018	EDR-7319			~~99-12-27~~ 01-11-15

Fig 30. Package outline SOT261-2 (PLCC28)

14. Abbreviations

Table 19. Abbreviations

Acronym	Description
ADC	Analog to Digital Converter
BOD	BrownOut Detect
CPU	Central Processing Unit
CCU	Capture/Compare Unit
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
GPIO	General Purpose Input/Output
LSB	Least Significant Bit
MSB	Most Significant Bit
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
WDT	WatchDog Timer

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18. Contents

continued >>

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