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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8250acvvmhbc

  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3® CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - One multichannel controller (MCC2)
    - Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    - Transparent
    - UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
    - Microwire compatible
    - Multiple-master, single-master, and slave modes
  - Up to four TDM interfaces
    - Supports one group of four TDM channels

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2

Figure 4 shows the FCC internal clock.

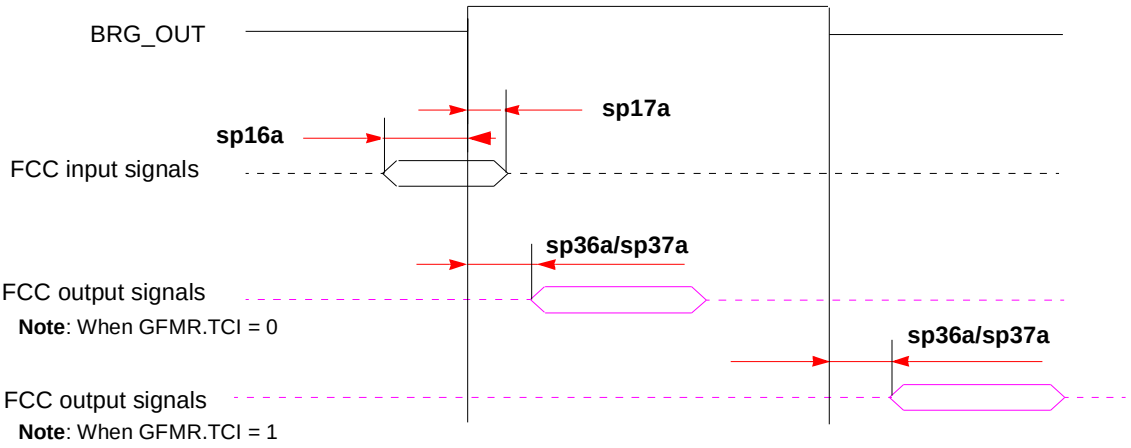
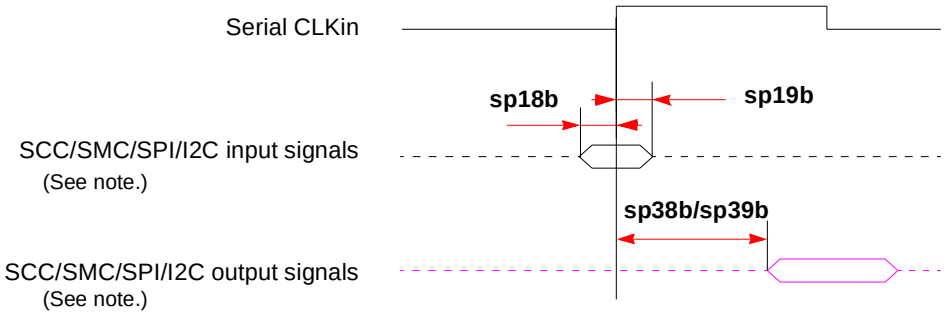


Figure 4. FCC Internal Clock Diagram

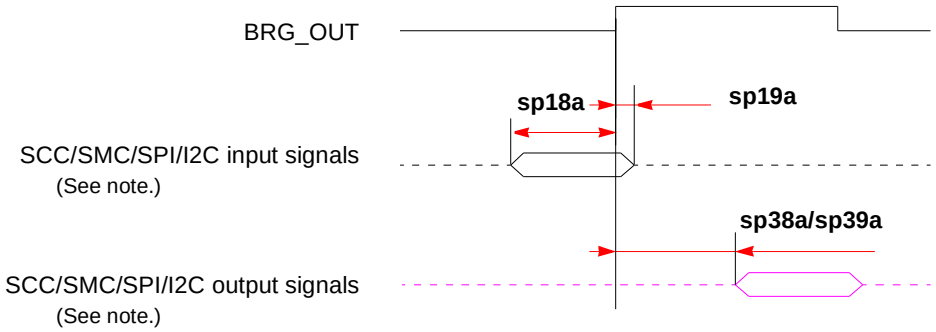
Figure 5 shows the SCC/SMC/SPI/I^{2}C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^{2}C External Clock Diagram

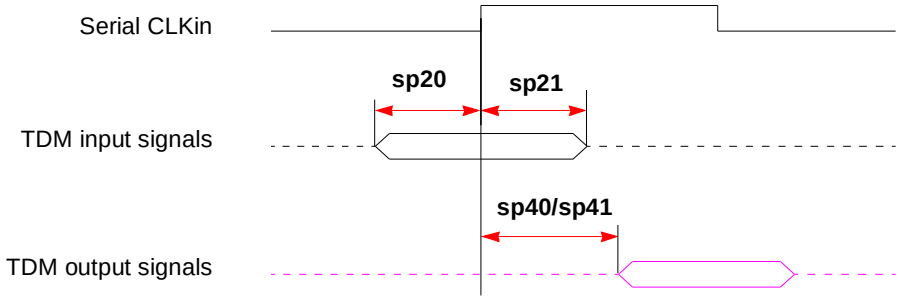
Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Figure 7 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000 [5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 12

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency / bus division factor

5 In this mode, PCI_MODCK must be “1”.

4 Pinout

This section provides the pin assignments and pinout list for the MPC8250.

4.1 TBGA Package

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, refer to Section 4.2, “PBGA Package.”

4.1.1 TBGA Pin Assignments

Figure 13 shows the pinout of the TBGA package as viewed from the top surface.

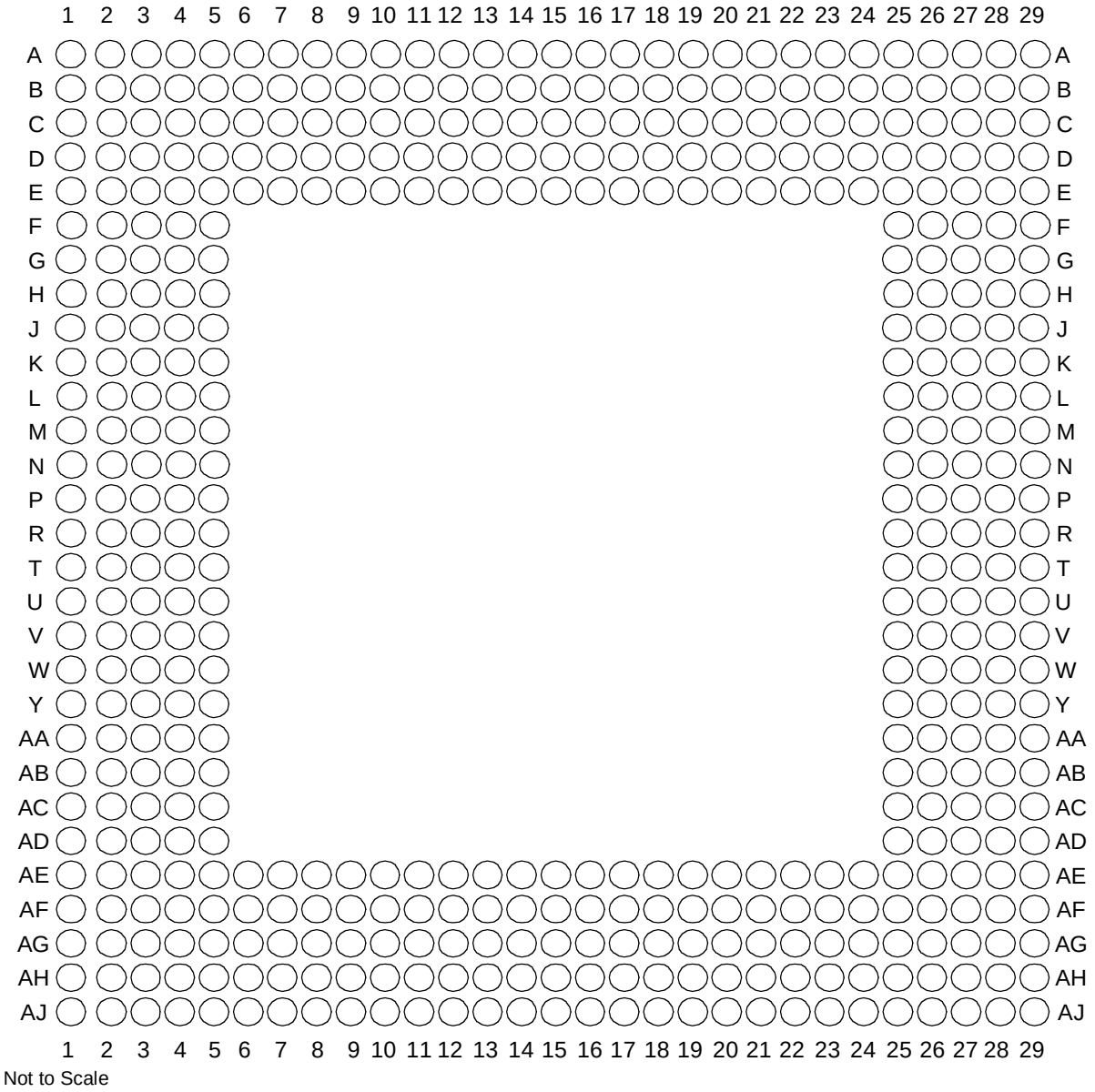


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20

Table 20. MPC8250 TBGA Package Pinout List (continued)

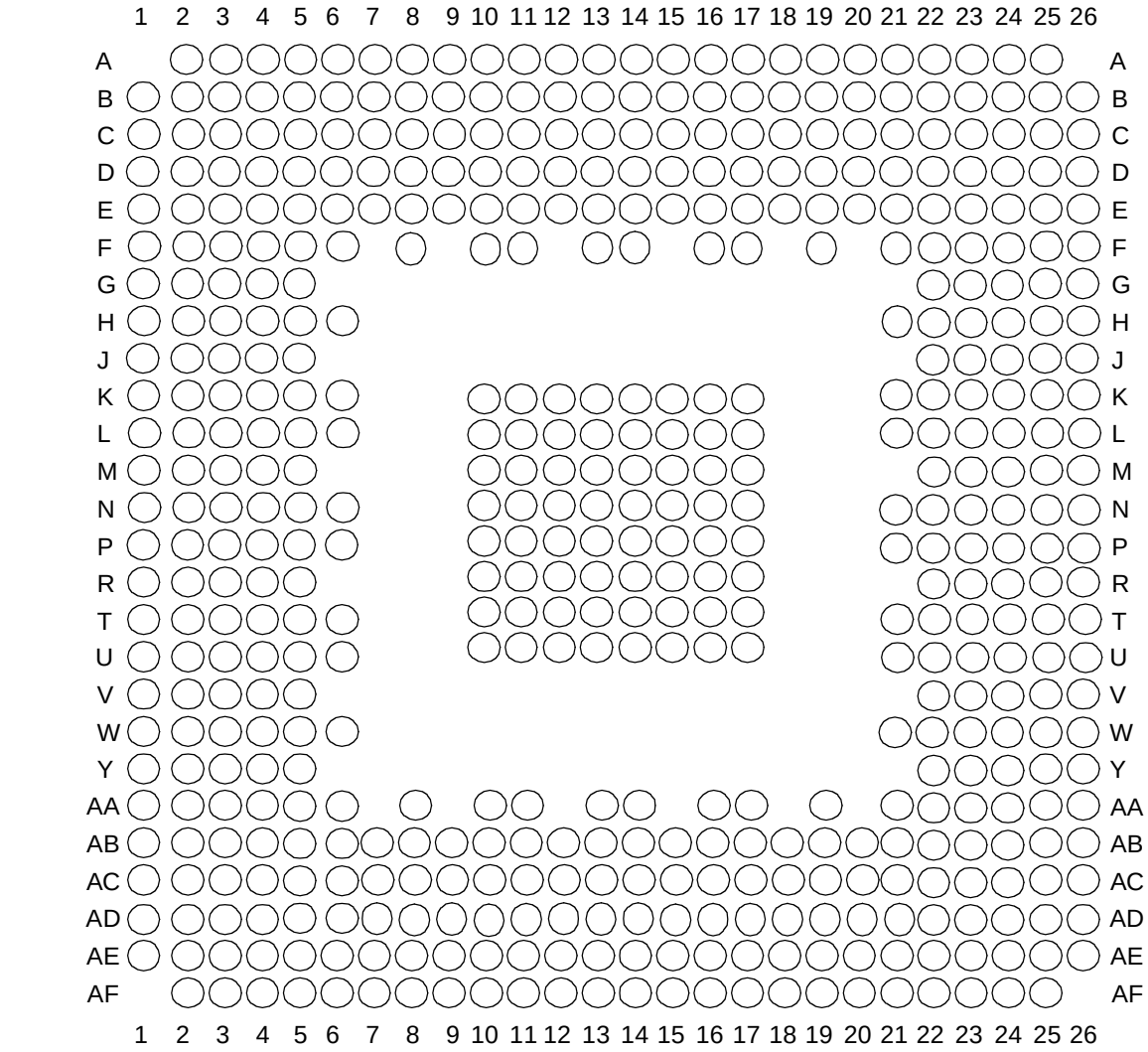
Pin Name	Ball
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{\text{BE0}}$	L28
LCL_DP1/C1/$\overline{\text{BE1}}$	N28
LCL_DP2/C2/$\overline{\text{BE2}}$	T28
LCL_DP3/C3/$\overline{\text{BE3}}$	W28

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1\_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

4.2.1 PBGA Pin Assignments

Figure 15 shows the pinout of the PBGA package as viewed from the top surface.



Not to Scale

Figure 15. Pinout of the 516 PBGA Package (View from Top)

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
A14	F11
A15	B7
A16	B8
A17	C9
A18	A7
A19	B9
A20	E11
A21	A8
A22	D11
A23	B10
A24	C11
A25	A9
A26	B11
A27	C12
A28	D12
A29	A10
A30	B12
A31	B13
TT0	E7
TT1	B3
TT2	F8
TT3	A3
TT4	C3
TBST	F5
TSIZ0	E3
TSIZ1	E2
TSIZ2	E1
TSIZ3	E4
AACK	D3
ARTRY	C2
DBG	A14
DBB/IRQ3	C15
D0	W4
D1	Y1
D2	V1

Table 22. MPC8250 PBGA Package Pinout List (continued)

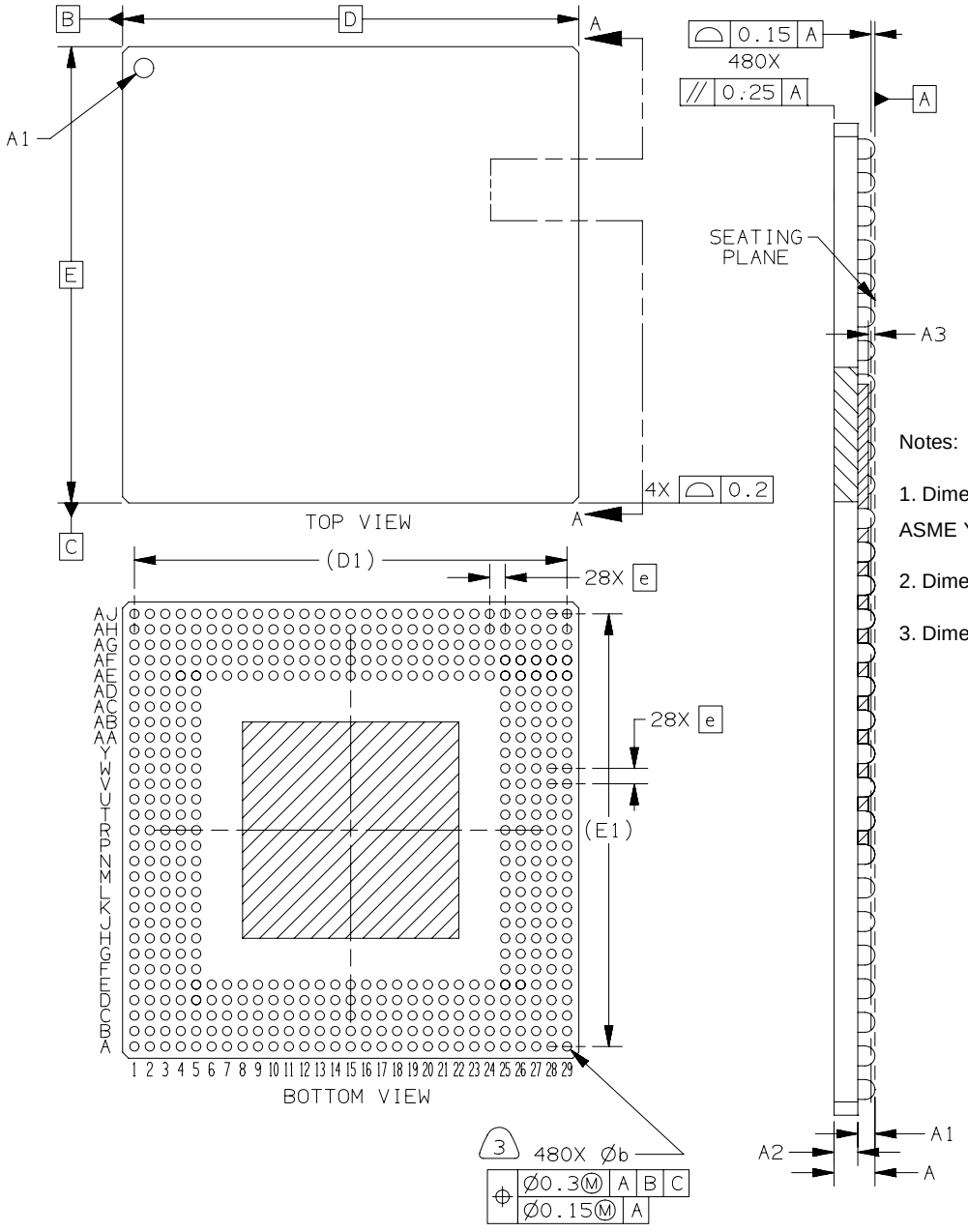
Pin Name	Ball
IRQ7/INT_OUT/APE	E5
TRST	F22
TCK	A24
TMS	C24
TDI	A25
TDO	B24
TRIS	C19
PORESET	B25
HRESET	D24
SRESET	E23
QREQ	D18
RSTCONF	E24
MODCK1/AP1/TC0/BNKSEL0	B16
MODCK2/AP2/TC1/BNKSEL1	F16
MODCK3/AP3/TC2/BNKSEL2	A15
XFC	A18
CLKIN1	G22
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC20 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC21[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AF25[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AE24[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AA21[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AD25[1]
PA6	AC24[1]
PA7/SMSYN2	AA22[1]
PA8/SMRXD2	AA23[1]
PA9/SMTXD2	Y26[1]
PA10/MSNUM5	W22[1]
PA11/MSNUM4	W23[1]
PA12/MSNUM3	V26[1]
PA13/MSNUM2	V25[1]
PA14/FCC1_RXD3	T22[1]
PA15/FCC1_RXD2	T25[1]
PA16/FCC1_RXD1	R24[1]
PA17/FCC1_RXD0/FCC1_RXD	P22[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	E22[1]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	E21[1]
PC30/CLK2/TOUT1	D21[1]
PC31/CLK1/BRGO1	B20[1]
PD4/BRGO8/FCC3_RTS/SMRXD2	AF23[1]
PD5/DONE1	AE23[1]
PD6/DACK1	AB21[1]
PD7/SMSYN1/FCC1_TXCLAV2	AD23[1]
PD8/SMRXD1/BRGO5	AD26[1]
PD9/SMTXD1/BRGO3	Y22[1]
PD10/L1CLKOB2/BRGO4	AB24[1]
PD11/L1RQB2	Y23[1]
PD12	AA26[1]
PD13	W24[1]
PD14/L1CLKOC2/I2CSCL	V22[1]
PD15/L1RQC2/I2CSDA	U26[1]
PD16/SPIMISO	T23[1]
PD17/BRGO2/SPIMOSI	R25[1]
PD18/SPICLK	P23[1]
PD19/SPISEL/BRGO1	N22[1]
PD20/RTS4/TENA4/L1RSYNCA2	M25[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	L25[1]
PD22/RXD4L1TXD0A2/L1TXDA2	J26[1]
PD23/RTS3/TENA3	K22[1]
PD24/TXD3	G25[1]
PD25/RXD3	H24[1]
PD26/RTS2/TENA2	F24[1]
PD27/TXD2	H22[1]
PD28/RXD2	B22[1]
PD29/RTS1/TENA1	D22[1]
PD30/TXD1	C21[1]
PD31/RXD1	E19[1]
VCCSYN	D19
VCCSYN1	K6
GNDSYN	B18

5.2.1 TBGA Package Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

Table 24. Document Revision History (continued)

Revision	Date	Substantive Changes
0.6	10/2002	Table 22, “VR Pinout”: corrected ball assignment for the following pins—A12–A17, $\overline{TA}$, PD5, PC2.
0.5	9/2002	Addition of VR (516 PBGA) package information. Refer to sections 2.2, 4.2, and 5.
0.4	5/2002	• Table 2: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 14: Note 3 • Table 16: Note 1 • Table 18: Note 3
0.3	3/2002	• Table 20: modified note to pin AF25.
0.2	3/2202	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.1	2/2002	• Note 2 for Table 4 (changes in italics): “...greater than *or equal to 266* MHz, *200* MHz CPM...” • Table 18: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: footnotes added to pins at AE11, AF25, U5, and V4.
0	11/2001	Initial version

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