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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8250avrihbc

Figure 1 shows the block diagram for the MPC8250.

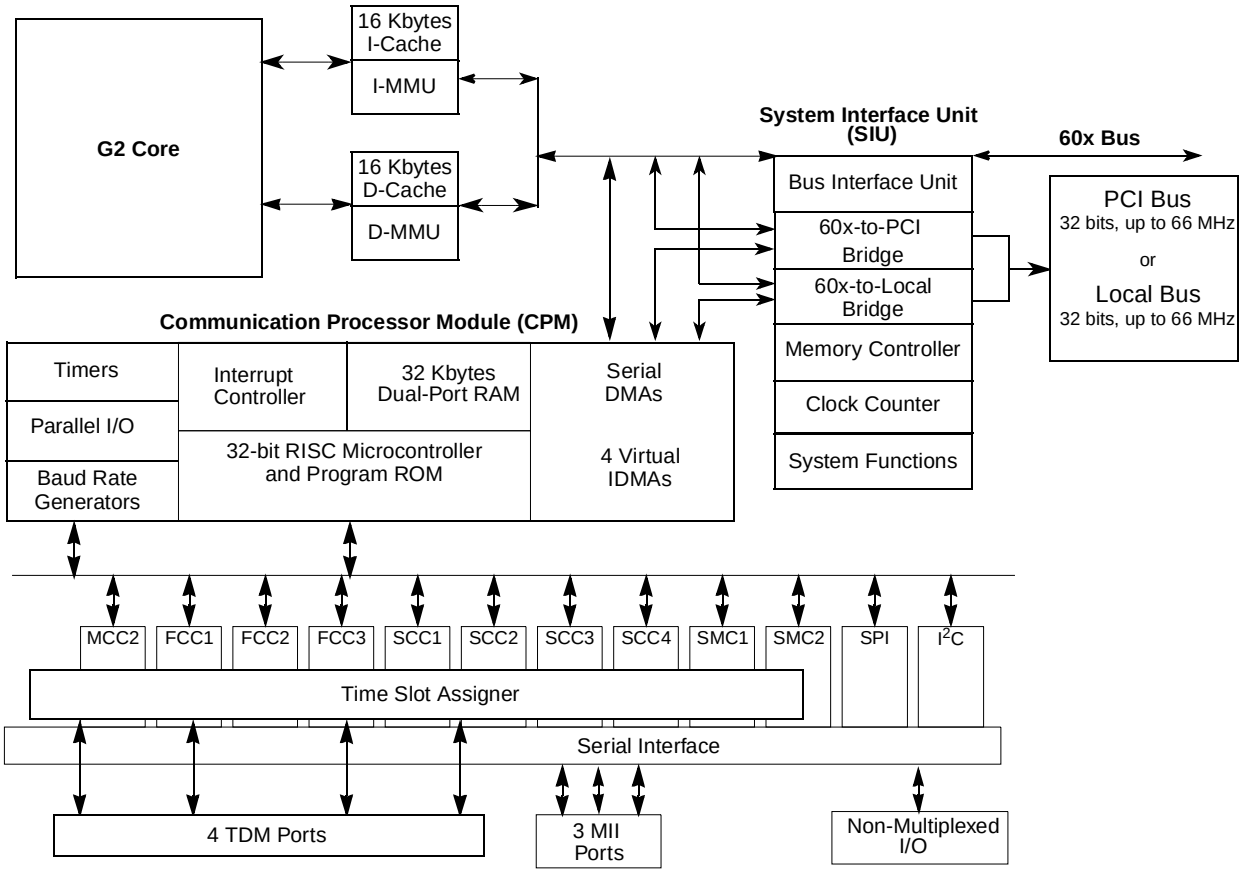


Figure 1. MPC8250 Block Diagram

1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–200 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC8250.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC8250. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings [1]

Rating	Symbol	Value	Unit
Core supply voltage [2]	VDD	-0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	-0.3 – 2.5	V
I/O supply voltage [3]	VDDH	-0.3 – 4.0	V
Input voltage [4]	VIN	GND(-0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(-55) – (+150)	°C

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions [1]

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9 [2]	1.7–2.1 [3]	1.9 –2.2 [4]	V
PLL supply voltage	VCCSYN	1.7 – 1.9[2]	1.7–2.1[3]	1.9–2.2[4]	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (-0.3) – 3.465			V
Junction temperature (maximum)	T_j	105 [5]			°C
Ambient temperature	T_A	0–70[5]			°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

2 CPU frequency less than or equal to 200 MHz.

3 CPU frequency greater than 200 MHz but less than 233 MHz.

4 CPU frequency greater than or equal to 233 MHz.

5 Note that for extended temperature parts the range is $(-40)_{T_A}$ – 105_{T_j}.

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC8250 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3W (when the ambient temperature is 70° C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations [1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W) [2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

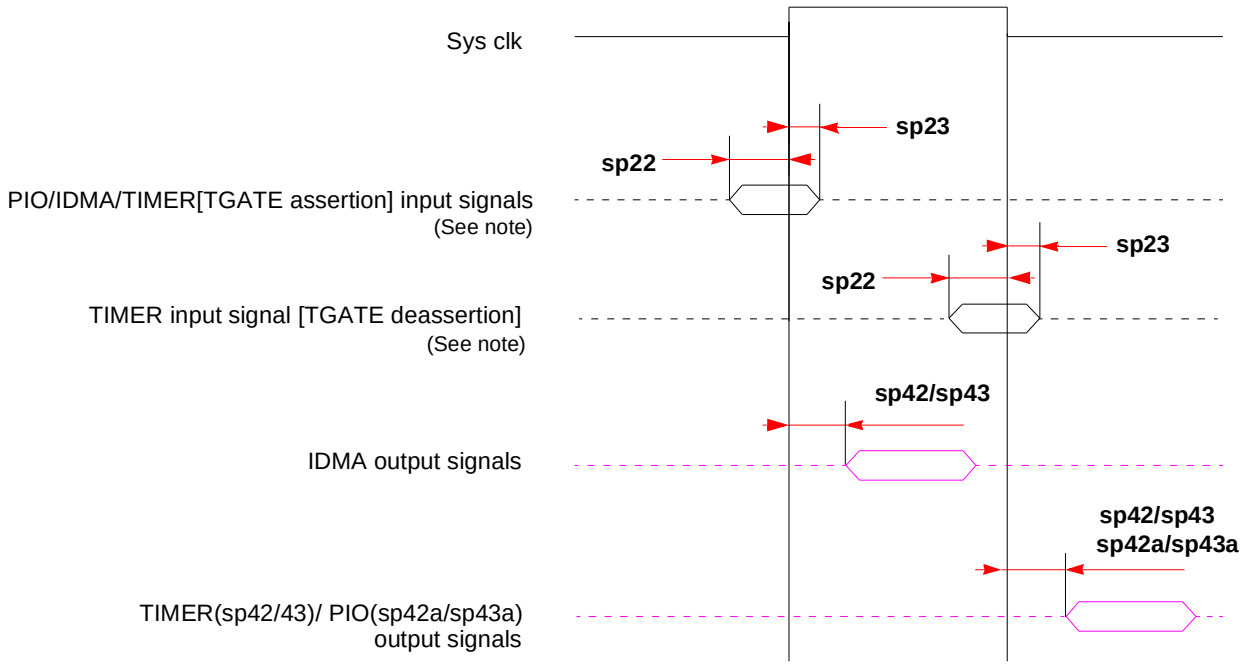
1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 9 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Figure 11 shows signal behavior in MEMC mode.

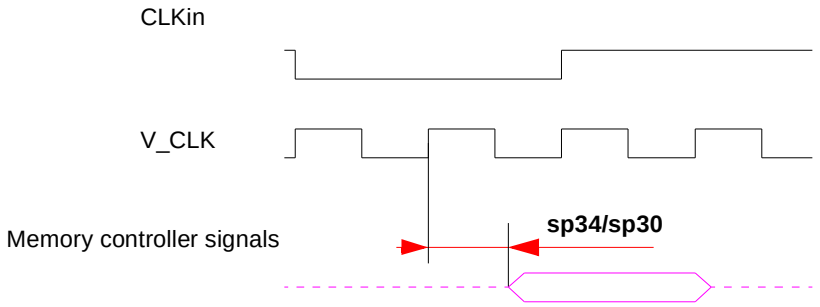


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC8250 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

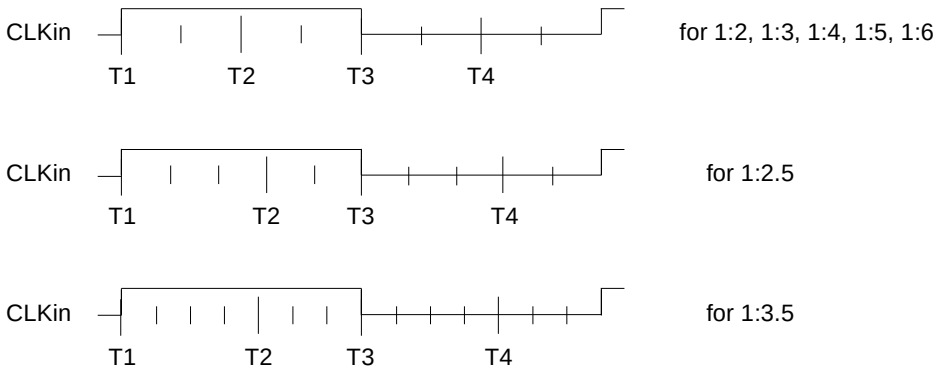


Figure 12. Internal Tick Spacing for Memory Controller Signals

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 133 MHz (150 MHz for extended temperature parts) and the CPM ranges between 66–233 MHz.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

3.2 PCI Mode

The PCI mode is selected according to three input pins, as shown in Table 12. In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000 [5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

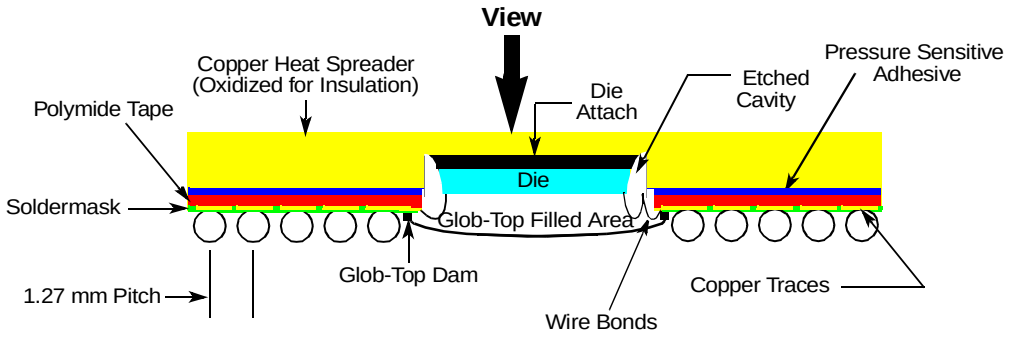


Figure 14. Side View of the TBGA Package

Table 20 shows the pinout list of the TBGA package of the MPC8250. Table 19 defines the conventions and acronyms used in Table 20.

Table 19. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 20. MPC8250 TBGA Package Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3	G29
LSDA10/LGPL0/PCI_MODCKH0	D27
LSDWE/LGPL1/PCI_MODCKH1	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2	E26
LSDCAS/LGPL3/PCI_MODCKH3	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK	B27
LWR	D28
L_A14/PAR	N27
L_A15/FRAME/SMI	T29
L_A16/TRDY	R27
L_A17/IRDY/CKSTP_OUT	R26
L_A18/STOP	R29
L_A19/DEVSEL	R28
L_A20/IDSEL	W29
L_A21/PERR	P28
L_A22/SERR	N26
L_A23/REQ0	AA27
L_A24/REQ1/HSEJSW	P29
L_A25/GNT0	AA26
L_A26/GNT1/HSLED	N25
L_A27/GNT2/HSENUM	AA25
L_A28/RST/CORE_SRESET	AB29
L_A29/INTA	AB28
L_A30/REQ2	P25
L_A31/DLLOUT	AB27
LCL_D0/AD0	H29

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC29 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC25[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AE28[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AG28[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AG26[1]
PA6	AE24[1]
PA7/SMSYN2	AH25[1]
PA8/SMRXD2	AF23[1]
PA9/SMTXD2	AH23[1]
PA10/MSNUM5	AE22[1]
PA11/MSNUM4	AH22[1]
PA12/MSNUM3	AJ21[1]
PA13/MSNUM2	AH20[1]
PA14/FCC1_RXD3	AG19[1]
PA15/FCC1_RXD2	AF18[1]
PA16/FCC1_RXD1	AF17[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1\_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
GNDSYN	AB1
CLKIN2	AE11
SPARE4 [2]	U5
$\overline{\text{PCI\_MODE}}$ [3]	AF25
SPARE6[2]	V4
THERMAL0 [4]	AA1
THERMAL1[4]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, this pin should be pulled up or left floating.

4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D) available at www.freescale.com.

4.2 PBGA Package

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8250, refer to Section 4.1, “TBGA Package.”

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
A14	F11
A15	B7
A16	B8
A17	C9
A18	A7
A19	B9
A20	E11
A21	A8
A22	D11
A23	B10
A24	C11
A25	A9
A26	B11
A27	C12
A28	D12
A29	A10
A30	B12
A31	B13
TT0	E7
TT1	B3
TT2	F8
TT3	A3
TT4	C3
TBST	F5
TSIZ0	E3
TSIZ1	E2
TSIZ2	E1
TSIZ3	E4
AACK	D3
ARTRY	C2
DBG	A14
DBB/IRQ3	C15
D0	W4
D1	Y1
D2	V1

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D38	H3
D39	F2
D40	Y2
D41	U3
D42	T2
D43	N2
D44	M5
D45	K1
D46	H4
D47	F1
D48	W2
D49	T4
D50	R3
D51	N4
D52	M1
D53	J2
D54	H5
D55	F3
D56	V3
D57	R5
D58	R2
D59	N5
D60	L2
D61	J3
D62	H1
D63	F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	AD1
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	AC1
$\overline{\text{IRQ6}}$/DP6/CSE0	AB2
$\overline{\text{IRQ7}}$/DP7/CSE1	Y3
PSDVAL	D15

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PA18/FCC1_TXD0/FCC1_TXD	N26[1]
PA19/FCC1_TXD1	N23[1]
PA20/FCC1_TXD2	K26[1]
PA21/FCC1_TXD3	L23[1]
PA22	K23[1]
PA23	H26[1]
PA24/MSNUM1	F25[1]
PA25/MSNUM0	D26[1]
PA26/FCC1_MII_RX_ER	D25[1]
PA27/FCC1_MII_RX_DV	C25[1]
PA28/FCC1_MII_TX_EN	C22[1]
PA29/FCC1_MII_TX_ER	B21[1]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	A20[1]
PA31/FCC1_MII_COL	A19[1]
PB4/FCC3_TXD3/L1RSYNCA2/ $\overline{\text{FCC3\_RTS}}$	AD21[1]
PB5/FCC3_TXD2/L1TSYNCA2/ L1GNTA2	AD22[1]
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	AC22[1]
PB7/FCC3_TXD0/FCC3_TXD/ L1TXDA2/L1TXD0A2	AE26[1]
PB8/FCC3_RXD0/FCC3_RXD/TXD3	AB23[1]
PB9/FCC3_RXD1/L1TXD2A2	AC26[1]
PB10/FCC3_RXD2	AB26[1]
PB11/FCC3_RXD3	AA25[1]
PB12/FCC3_MII_CRS/TXD2	W26[1]
PB13/FCC3_MII_COL/L1TXD1A2	W25[1]
PB14/FCC3_MII_TX_EN/RXD3	V24[1]
PB15/FCC3_MII_TX_ER/RXD2	U24[1]
PB16/FCC3_MII_RX_ER/CLK18	R22[1]
PB17/FCC3_MII_RX_DV/CLK17	R23[1]
PB18/FCC2_RXD3/L1CLKOD2/ L1RXD2A2	M23[1]
PB19FCC2_RXD2/L1RQD2/L1RXD3A2	L24[1]
PB20/FCC2_RXD1/L1RSYNCD2/ L1TXD1A1	K24[1]
PB21/FCC2_RXD0/FCC2_RXD/ L1TSYNCD2/L1GNTD2	L21[1]
PB22/FCC2_TXD0/FCC2_TXD/ L1RXDD2	P25[1]
PB23/FCC2_TXD1/L1TXDD2	N25[1]
PB24/FCC2_TXD2/L1RSYNCC2	E26[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	H23[1]
PB26/FCC2_MII_CRS/L1RXDC2	C26[1]
PB27/FCC2_MII_COL/L1TXDC2	B26[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1	A22[1]
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	A21[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	E20[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	C20[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/ L1CLKOA2	AE22[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AA19[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AF24[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE25[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AB22[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AC25[1]
PC6/$\overline{\text{FCC1\_CD}}$	AB25[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AA24[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	Y24[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2	U22[1]
PC10/$\overline{\text{CD3}}$/RENA3	V23[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	U23[1]
PC12/$\overline{\text{CD2}}$/RENA2	T26[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	R26[1]
PC14/$\overline{\text{CD1}}$/RENA1	P26[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	P24[1]
PC16/CLK16/TIN4	M26[1]
PC17/CLK15/TIN3/BRGO8	L26[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	M24[1]
PC19/CLK13/BRGO7/SPICLK	L22[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	K25[1]
PC21/CLK11/BRGO6	J25[1]
PC22/CLK10/$\overline{\text{DONE1}}$	G26[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	F26[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	G24[1]
PC25/CLK7/BRGO4	E25[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	G23[1]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3	B23[1]

5.1 Package Parameters

Package parameters are provided in Table 23.

Table 23. Package Parameters

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8250	37.5 × 37.5	TBGA	480	1.27	1.55
VV			TBGA (Pb free)			
ZO		27 × 27	PBGA	516	1	2.25
VR			PBGA (Pb free)			

5.2 Mechanical Dimensions

This section discusses the TBGA and PBGA package dimensions.