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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8250avvpibc

Figure 1 shows the block diagram for the MPC8250.

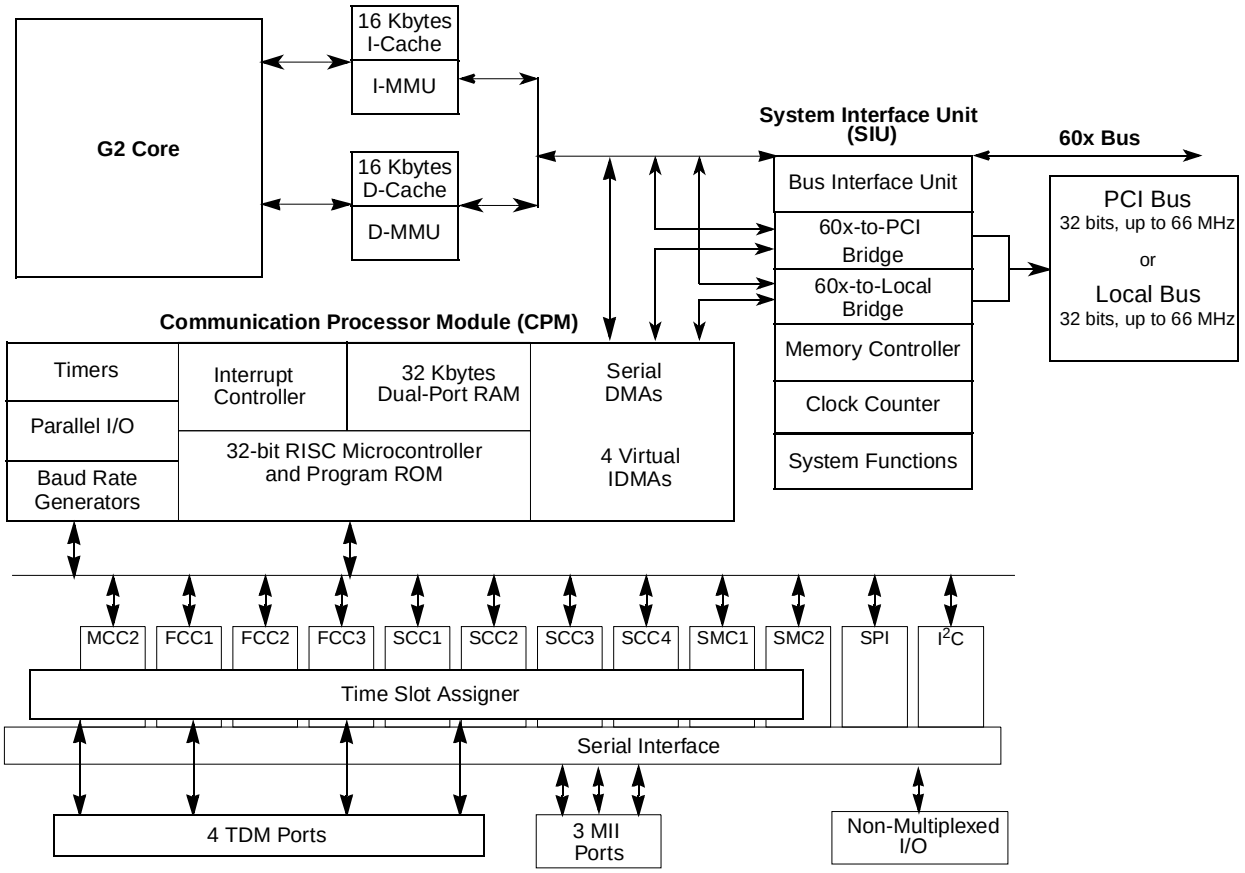


Figure 1. MPC8250 Block Diagram

1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–200 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm
  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)

  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic (1.8 V) and for I/O (3.3V)
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE 1149.1™ JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation
  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)

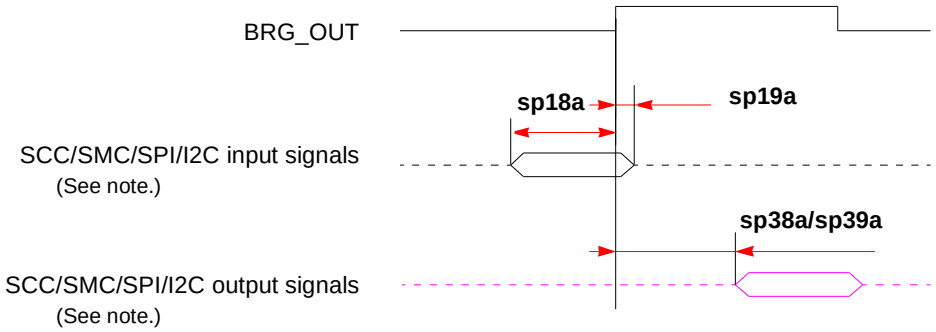
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  - Supports the I_2O standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  - Makes use of the local bus signals, so there is no need for additional pins

Table 3. DC Electrical Characteristics [1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0:3]/LBS[0–3]/PCI_CFG[0–3 LSDA10/LGPL0/PCI_MODCKH0 LSDWE/LGPL1/PCI_MODCKH1 LOE/LSDRAS/LGPL2/PCI_MODCKH2 LSDCAS/LGPL3/PCI_MODCKH3 LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR L_A15/FRAME/SMI L_A16/TRDY L_A17/IRDY/CKSTP_OUT L_A18/STOP L_A19/DEVSEL L_A20/IDSEL L_A21/PERR L_A22/SERR L_A23/REQ0 L_A24/REQ1/HSEJSW L_A25/GNT0 L_A26/GNT1/HSLED L_A27/GNT2/HSENUM L_A28/RST/CORE_SRESET L_A29/INTA L_A30/REQ2 L_A31 LCL_D(0-31)/AD(0-31) LCL_DP(0-3)/C/BE(0-3) PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

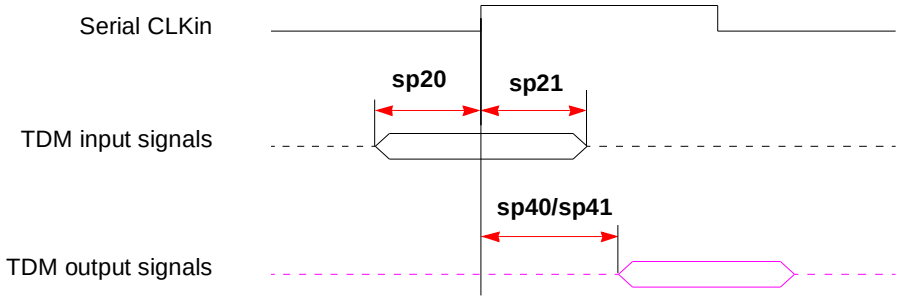
Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Figure 7 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Figure 9 shows the interaction of several bus signals.

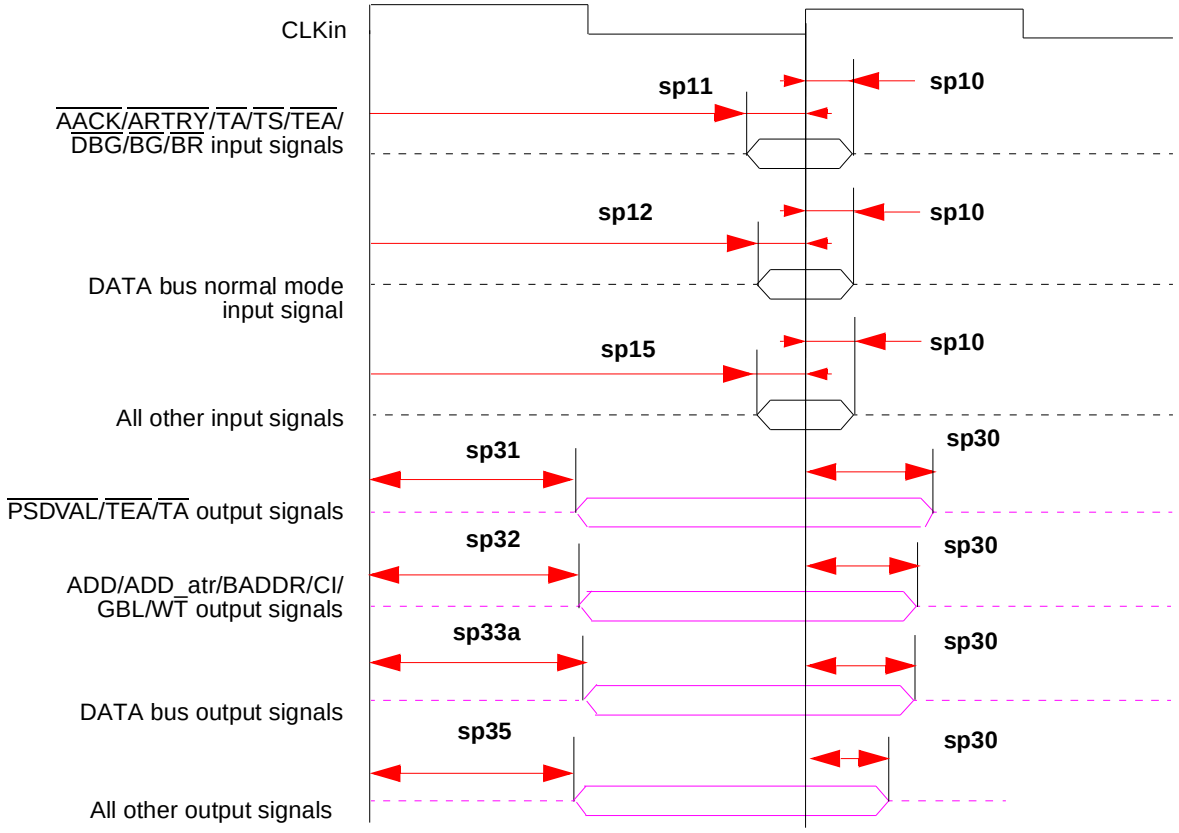


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

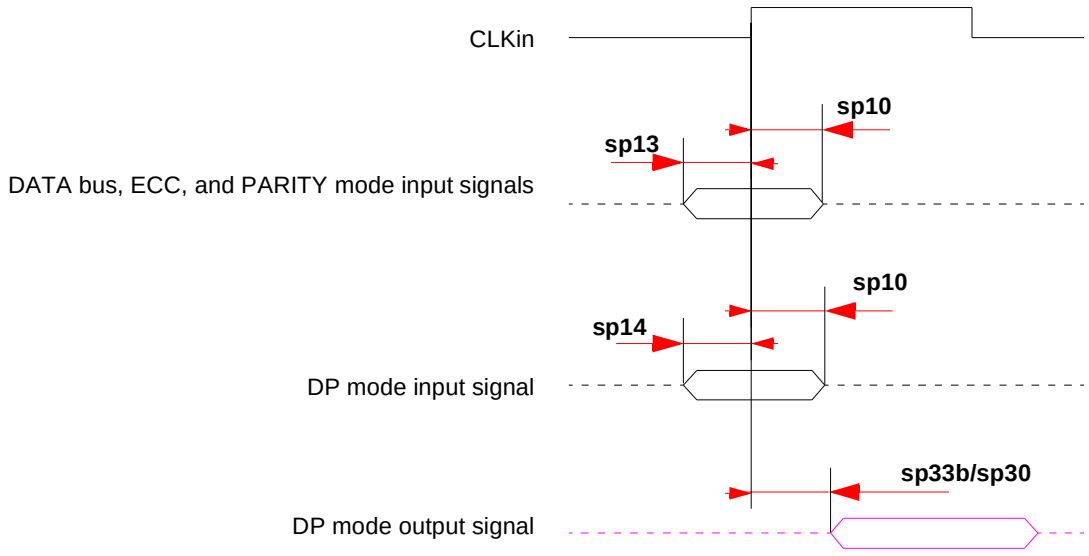


Figure 10. Parity Mode Diagram

Table 13. Clock Default Configurations

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note also that basic modes are shown in **boldface** type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 14. Clock Configuration Modes [1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 12

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency / bus division factor

5 In this mode, PCI_MODCK must be “1”.

4 Pinout

This section provides the pin assignments and pinout list for the MPC8250.

4.1 TBGA Package

The following figures and table represent the standard 480 TBGA package. For information on the alternate package, refer to Section 4.2, “PBGA Package.”

4.1.1 TBGA Pin Assignments

Figure 13 shows the pinout of the TBGA package as viewed from the top surface.

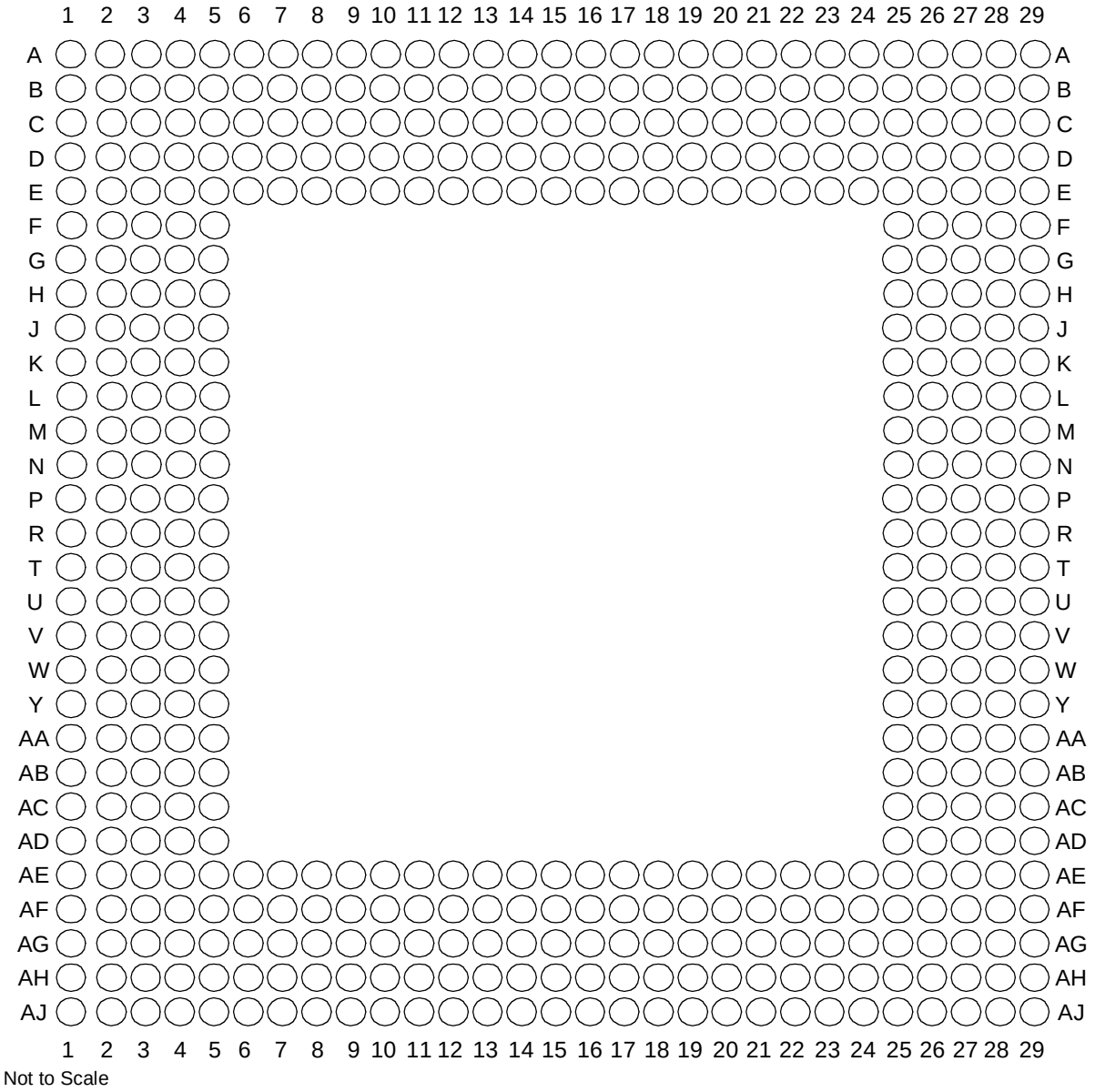


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3	G29
LSDA10/LGPL0/PCI_MODCKH0	D27
LSDWE/LGPL1/PCI_MODCKH1	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2	E26
LSDCAS/LGPL3/PCI_MODCKH3	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK	B27
LWR	D28
L_A14/PAR	N27
L_A15/FRAME/SMI	T29
L_A16/TRDY	R27
L_A17/IRDY/CKSTP_OUT	R26
L_A18/STOP	R29
L_A19/DEVSEL	R28
L_A20/IDSEL	W29
L_A21/PERR	P28
L_A22/SERR	N26
L_A23/REQ0	AA27
L_A24/REQ1/HSEJSW	P29
L_A25/GNT0	AA26
L_A26/GNT1/HSLED	N25
L_A27/GNT2/HSENUM	AA25
L_A28/RST/CORE_SRESET	AB29
L_A29/INTA	AB28
L_A30/REQ2	P25
L_A31/DLLOUT	AB27
LCL_D0/AD0	H29

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{\text{BE0}}$	L28
LCL_DP1/C1/$\overline{\text{BE1}}$	N28
LCL_DP2/C2/$\overline{\text{BE2}}$	T28
LCL_DP3/C3/$\overline{\text{BE3}}$	W28

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PA17/FCC1_RXD0/FCC1_RXD	AE16[1]
PA18/FCC1_TXD0/FCC1_TXD	AJ16[1]
PA19/FCC1_TXD1	AG15[1]
PA20/FCC1_TXD2	AJ13[1]
PA21/FCC1_TXD3	AE13[1]
PA22	AF12[1]
PA23	AG11[1]
PA24/MSNUM1	AH9[1]
PA25/MSNUM0	AJ8[1]
PA26/FCC1_MII_RX_ER	AH7[1]
PA27/FCC1_MII_RX_DV	AF7[1]
PA28/FCC1_MII_TX_EN	AD5[1]
PA29/FCC1_MII_TX_ER	AF1[1]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	AD3[1]
PA31/FCC1_MII_COL	AB5[1]
PB4/FCC3_TXD3/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28[1]
PB5/FCC3_TXD2/L1TSYNCA2/L1GNTA2	AD26[1]
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	AD25[1]
PB7/FCC3_TXD0/FCC3_TXD/L1TXDA2/L1TXD0A2	AE26[1]
PB8/FCC3_RXD0/FCC3_RXD/TXD3	AH27[1]
PB9/FCC3_RXD1/L1TXD2A2	AG24[1]
PB10/FCC3_RXD2	AH24[1]
PB11/FCC3_RXD3	AJ24[1]
PB12/FCC3_MII_CRS/TXD2	AG22[1]
PB13/FCC3_MII_COL/L1TXD1A2	AH21[1]
PB14/FCC3_MII_TX_EN/RXD3	AG20[1]
PB15/FCC3_MII_TX_ER/RXD2	AF19[1]
PB16/FCC3_MII_RX_ER/CLK18	AJ18[1]
PB17/FCC3_MII_RX_DV/CLK17	AJ17[1]
PB18/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[1]
PB19/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[1]
PB20/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[1]
PB21/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2	AH11[1]
PB22/FCC2_TXD0/FCC2_TXD/L1RXDD2	AH16[1]
PB23/FCC2_TXD1/L1TXDD2	AE15[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1\_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[1]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[1]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[1]
PC30/CLK2/$\overline{\text{TOUT1}}$	AE1[1]
PC31/CLK1/BRGO1	AD1[1]
PD4/BRGO8/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[1]
PD5/$\overline{\text{DONE1}}$	AD27[1]
PD6/$\overline{\text{DACK1}}$	AF29[1]
PD7/SMSYN1FCC1_TXCLAV2	AF28[1]
PD8/SMRXD1/BRGO5	AG25[1]
PD9/SMTXD1/BRGO3	AH26[1]
PD10/L1CLKOB2/BRGO4	AJ27[1]
PD11/$\overline{\text{L1RQB2}}$	AJ23[1]
PD12	AG23[1]
PD13	AJ22[1]
PD14/L1CLKOC2/I2CSCL	AE20[1]
PD15/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[1]
PD16/SPIMISO	AG18[1]
PD17/BRGO2/SPIMOSI	AG17[1]
PD18/SPICLK	AF16[1]
PD19/SPISEL/BRGO	AH15[1]
PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2	AJ14[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	AH13[1]
PD22/RXD4/L1TXD0A2/L1TXDA2	AJ12[1]
PD23/$\overline{\text{RTS3}}$/TENA3	AE12[1]
PD24/TXD3	AF10[1]
PD25/RXD3	AG9[1]
PD26/$\overline{\text{RTS2}}$/TENA2	AH8[1]
PD27/TXD2	AG7[1]
PD28/RXD2	AE4[1]
PD29/$\overline{\text{RTS1}}$/TENA1	AG1[1]
PD30/TXD1	AD4[1]
PD31/RXD1	AD2[1]
VCCSYN	AB3
VCCSYN1	B9

Figure 16 shows the side profile of the PBGA package to indicate the direction of the top surface view.

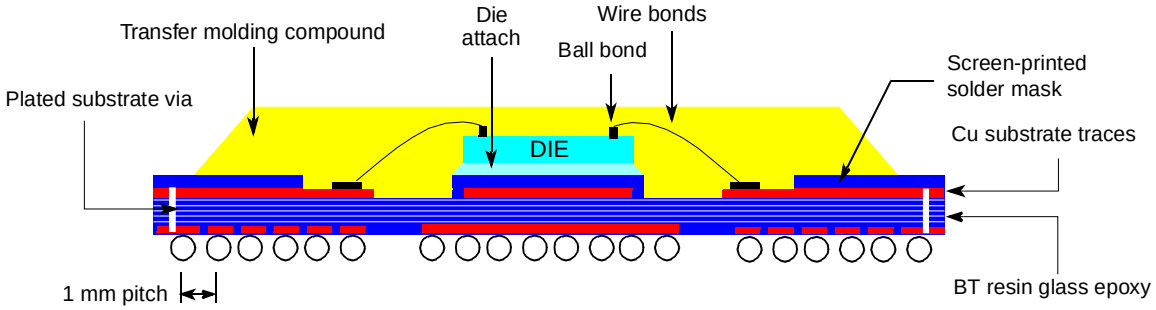


Figure 16. Side View of the PBGA Package

Table 22 shows the pinout list of the PBGA package of the MPC8250. Table 21 defines conventions and acronyms used in Table 22.

Table 21. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 22. MPC8250 PBGA Package Pinout List

Pin Name	Ball
BR	C16
BG	D2
ABB/IRQ2	C1
TS	D1
A0	D5
A1	E8
A2	C4
A3	B4
A4	A4
A5	D7
A6	D8
A7	C6
A8	B5
A9	B6
A10	C7
A11	C8
A12	A6
A13	D9

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D38	H3
D39	F2
D40	Y2
D41	U3
D42	T2
D43	N2
D44	M5
D45	K1
D46	H4
D47	F1
D48	W2
D49	T4
D50	R3
D51	N4
D52	M1
D53	J2
D54	H5
D55	F3
D56	V3
D57	R5
D58	R2
D59	N5
D60	L2
D61	J3
D62	H1
D63	F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	AD1
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	AC1
$\overline{\text{IRQ6}}$/DP6/CSE0	AB2
$\overline{\text{IRQ7}}$/DP7/CSE1	Y3
PSDVAL	D15

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	E22[1]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	E21[1]
PC30/CLK2/TOUT1	D21[1]
PC31/CLK1/BRGO1	B20[1]
PD4/BRGO8/FCC3_RTS/SMRXD2	AF23[1]
PD5/DONE1	AE23[1]
PD6/DACK1	AB21[1]
PD7/SMSYN1/FCC1_TXCLAV2	AD23[1]
PD8/SMRXD1/BRGO5	AD26[1]
PD9/SMTXD1/BRGO3	Y22[1]
PD10/L1CLKOB2/BRGO4	AB24[1]
PD11/L1RQB2	Y23[1]
PD12	AA26[1]
PD13	W24[1]
PD14/L1CLKOC2/I2CSCL	V22[1]
PD15/L1RQC2/I2CSDA	U26[1]
PD16/SPIMISO	T23[1]
PD17/BRGO2/SPIMOSI	R25[1]
PD18/SPICLK	P23[1]
PD19/SPISEL/BRGO1	N22[1]
PD20/RTS4/TENA4/L1RSYNCA2	M25[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	L25[1]
PD22/RXD4L1TXD0A2/L1TXDA2	J26[1]
PD23/RTS3/TENA3	K22[1]
PD24/TXD3	G25[1]
PD25/RXD3	H24[1]
PD26/RTS2/TENA2	F24[1]
PD27/TXD2	H22[1]
PD28/RXD2	B22[1]
PD29/RTS1/TENA1	D22[1]
PD30/TXD1	C21[1]
PD31/RXD1	E19[1]
VCCSYN	D19
VCCSYN1	K6
GNDSYN	B18

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
CLKIN2	K21
SPARE4 [2]	C14
$\overline{\text{PCI\_MODE}}$ [3]	AD24
SPARE6[2]	B15
THERMAL0 [4]	E17
THERMAL1[4]	C23
I/O power	E6, F6, H6, L5, L6, P6, T6, U6, V5, Y5, AA6, AA8, AA10, AA11, AA14, AA16, AA17, AB19, AB20, W21, U21, T21, P21, N21, M22, J22, H21, F21, F19, F17, E16, F14, E13, E12, F10, E10, E9
Core Power	L3, V4, W3, AC11, AD11, AB15, U25, T24, J24, H25, F23, B19, D17, C17, D10, C10
Ground	A2, B1, B2, A5, C5, C18, D4, D6, G2, L4, P1, R1, R4, AC4, AE7, AC23, Y25, N24, J23, A23, D23, D20, E18, A13, A16, K10, K11, K12, K13, K14, K15, K16, K17, L10, L11, L12, L13, L14, L15, L16, L17, M10, M11, M12, M13, M14, M15, M16, M17, N10, N11, N12, N13, N14, N15, N16, N17, P10, P11, P12, P13, P14, P15, P16, P17, R10, R11,R12, R13, R14, R15, R16, R17, T10, T11, T12, T13, T14, T15, T16, T17, U10, U11, U12, U13, U14, U15, U16, U17

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, must be pulled up or left floating.

4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D).

5 Package Description

The following sections provide the package parameters and mechanical dimensions.

5.1 Package Parameters

Package parameters are provided in Table 23.

Table 23. Package Parameters

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8250	37.5 × 37.5	TBGA	480	1.27	1.55
VV			TBGA (Pb free)			
ZO		27 × 27	PBGA	516	1	2.25
VR			PBGA (Pb free)			

5.2 Mechanical Dimensions

This section discusses the TBGA and PBGA package dimensions.