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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8250acvvmhbc

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

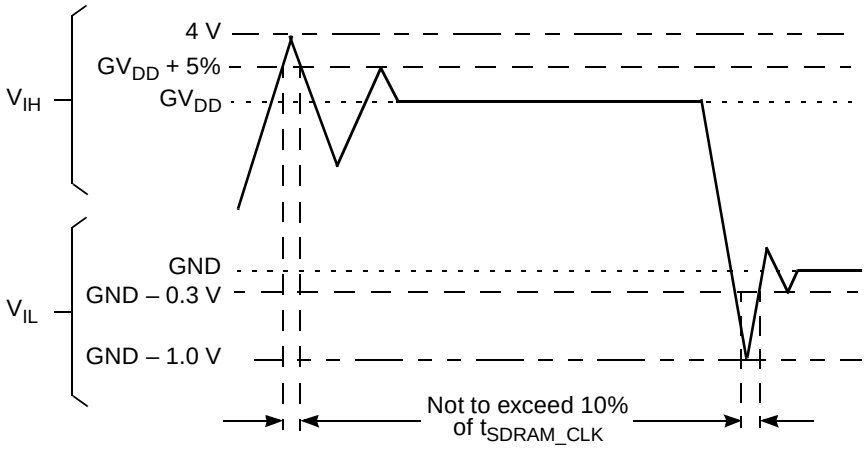


Figure 2. Overshoot/Undershoot Voltage

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics [1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH [2]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA
Output high voltage, I_{OH} = –2 mA	V_{OH}	2.4	—	V

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

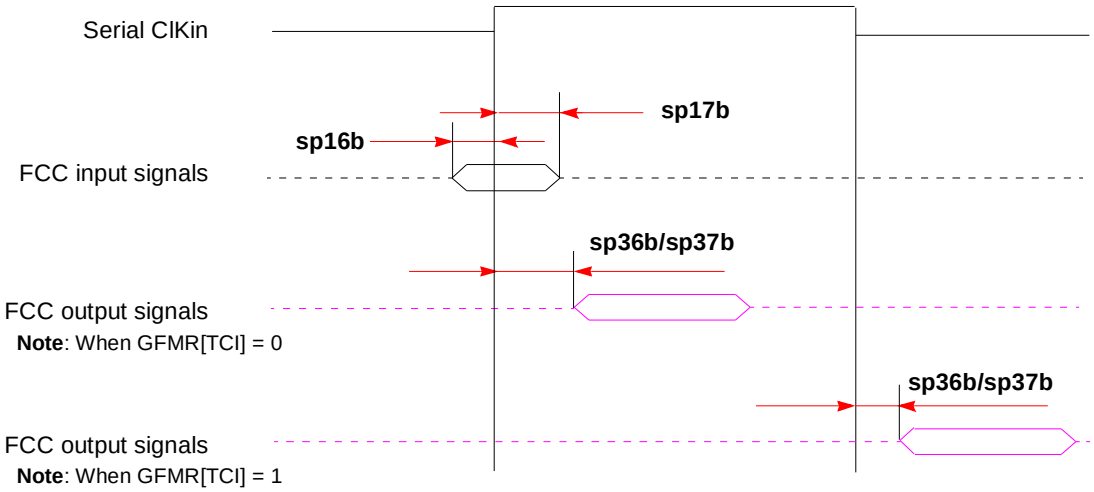


Figure 3. FCC External Clock Diagram

Figure 9 shows the interaction of several bus signals.

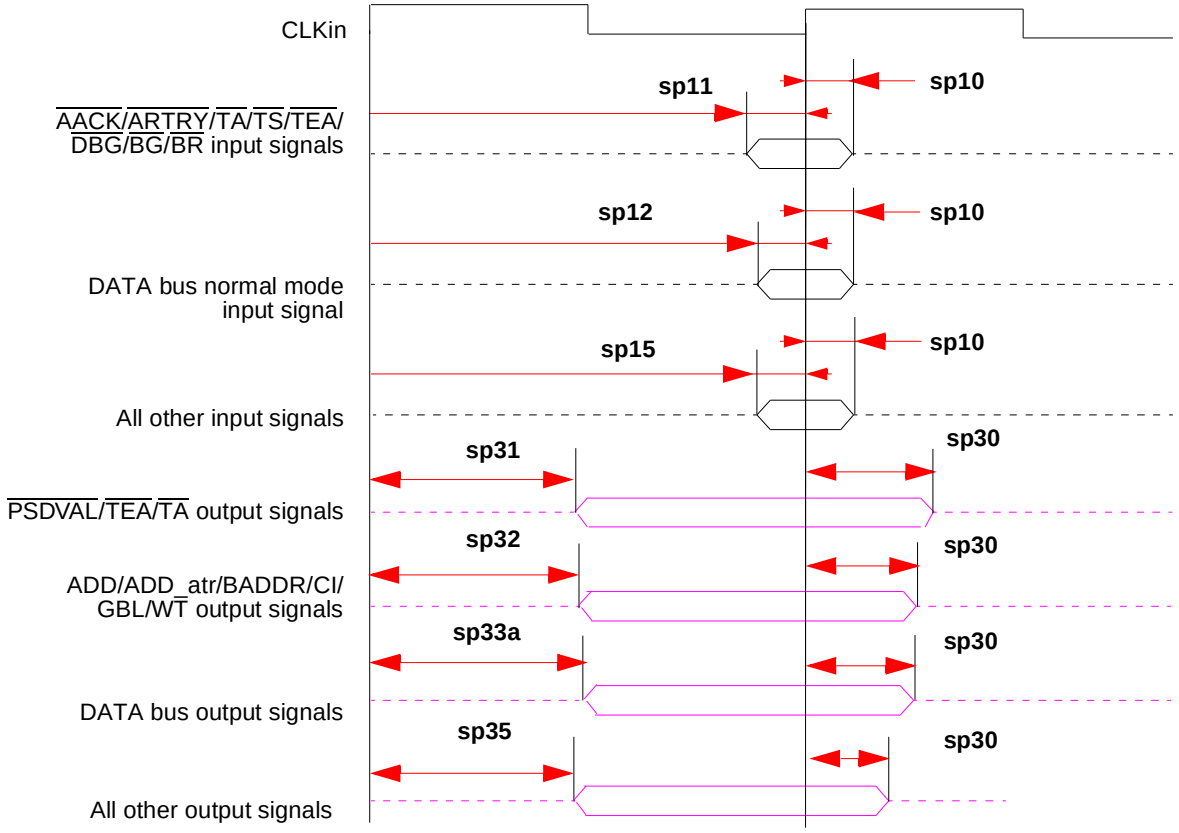


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

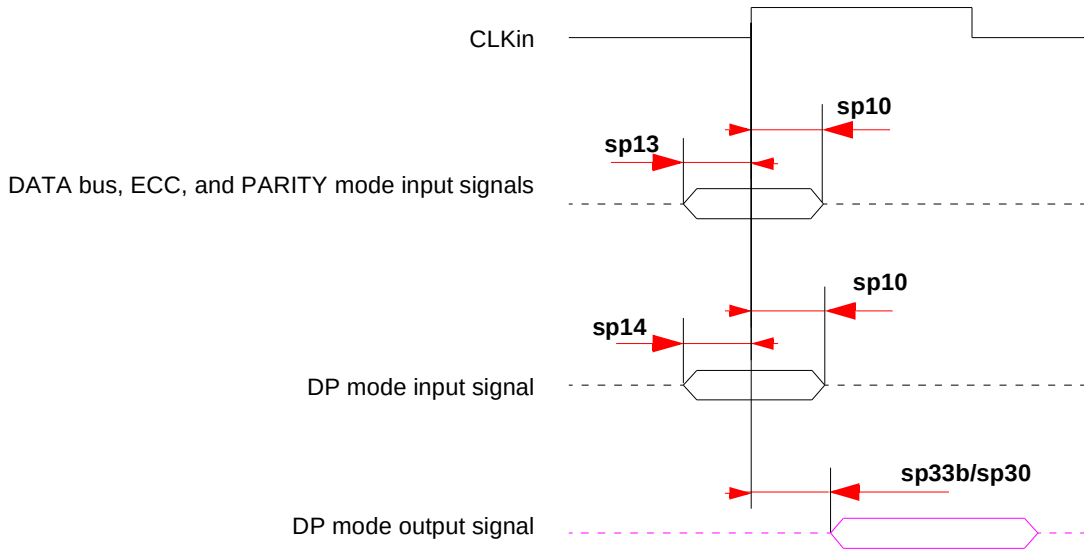


Figure 10. Parity Mode Diagram

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz

3.2.1 PCI Host Mode

The frequencies listed in Table 15 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 15. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

1 Assumes MODCK_HI = 0000.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to Table 12.

Table 16 describes all possible clock configurations when using the MPC8250's internal PCI bridge in host mode.

Table 16. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**	**4/8**	**33**/16 **MHz**
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 [3]	33 MHz	5	166 MHz	5	166 MHz	5	**33 MHz**
0011_001[3]	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz

4.1.1 TBGA Pin Assignments

Figure 13 shows the pinout of the TBGA package as viewed from the top surface.

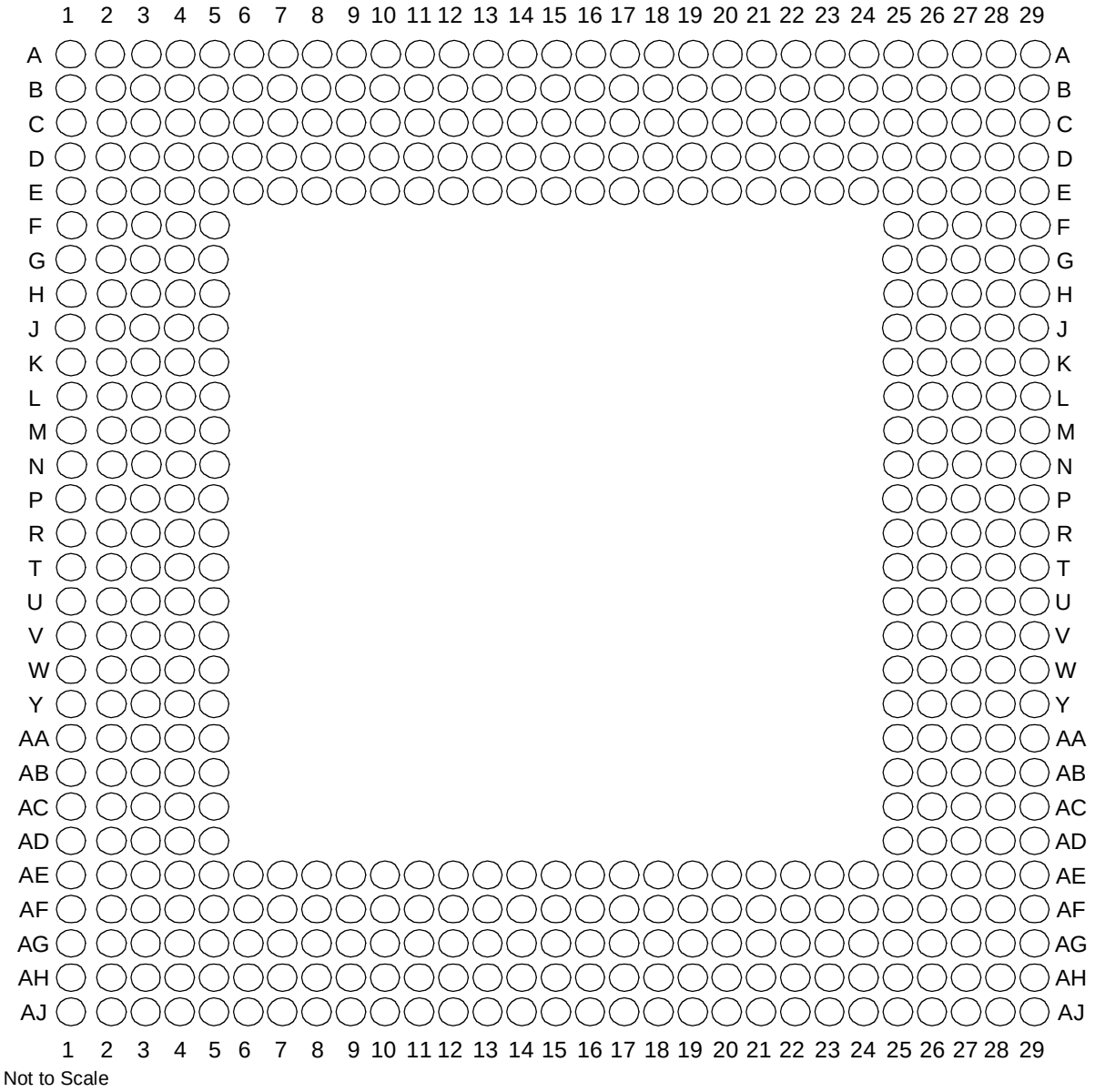


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PA17/FCC1_RXD0/FCC1_RXD	AE16[1]
PA18/FCC1_TXD0/FCC1_TXD	AJ16[1]
PA19/FCC1_TXD1	AG15[1]
PA20/FCC1_TXD2	AJ13[1]
PA21/FCC1_TXD3	AE13[1]
PA22	AF12[1]
PA23	AG11[1]
PA24/MSNUM1	AH9[1]
PA25/MSNUM0	AJ8[1]
PA26/FCC1_MII_RX_ER	AH7[1]
PA27/FCC1_MII_RX_DV	AF7[1]
PA28/FCC1_MII_TX_EN	AD5[1]
PA29/FCC1_MII_TX_ER	AF1[1]
PA30/FCC1_MII_CRS/$\overline{\text{FCC1\_RTS}}$	AD3[1]
PA31/FCC1_MII_COL	AB5[1]
PB4/FCC3_TXD3/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28[1]
PB5/FCC3_TXD2/L1TSYNCA2/L1GNTA2	AD26[1]
PB6/FCC3_TXD1/L1RXDA2/L1RXD0A2	AD25[1]
PB7/FCC3_TXD0/FCC3_TXD/L1TXDA2/L1TXD0A2	AE26[1]
PB8/FCC3_RXD0/FCC3_RXD/TXD3	AH27[1]
PB9/FCC3_RXD1/L1TXD2A2	AG24[1]
PB10/FCC3_RXD2	AH24[1]
PB11/FCC3_RXD3	AJ24[1]
PB12/FCC3_MII_CRS/TXD2	AG22[1]
PB13/FCC3_MII_COL/L1TXD1A2	AH21[1]
PB14/FCC3_MII_TX_EN/RXD3	AG20[1]
PB15/FCC3_MII_TX_ER/RXD2	AF19[1]
PB16/FCC3_MII_RX_ER/CLK18	AJ18[1]
PB17/FCC3_MII_RX_DV/CLK17	AJ17[1]
PB18/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[1]
PB19/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[1]
PB20/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[1]
PB21/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2	AH11[1]
PB22/FCC2_TXD0/FCC2_TXD/L1RXDD2	AH16[1]
PB23/FCC2_TXD1/L1TXDD2	AE15[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[1]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[1]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[1]
PC30/CLK2/$\overline{\text{TOUT1}}$	AE1[1]
PC31/CLK1/BRGO1	AD1[1]
PD4/BRGO8/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[1]
PD5/$\overline{\text{DONE1}}$	AD27[1]
PD6/$\overline{\text{DACK1}}$	AF29[1]
PD7/SMSYN1FCC1_TXCLAV2	AF28[1]
PD8/SMRXD1/BRGO5	AG25[1]
PD9/SMTXD1/BRGO3	AH26[1]
PD10/L1CLKOB2/BRGO4	AJ27[1]
PD11/$\overline{\text{L1RQB2}}$	AJ23[1]
PD12	AG23[1]
PD13	AJ22[1]
PD14/L1CLKOC2/I2CSCL	AE20[1]
PD15/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[1]
PD16/SPIMISO	AG18[1]
PD17/BRGO2/SPIMOSI	AG17[1]
PD18/SPICLK	AF16[1]
PD19/SPISEL/BRGO	AH15[1]
PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2	AJ14[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	AH13[1]
PD22/RXD4/L1TXD0A2/L1TXDA2	AJ12[1]
PD23/$\overline{\text{RTS3}}$/TENA3	AE12[1]
PD24/TXD3	AF10[1]
PD25/RXD3	AG9[1]
PD26/$\overline{\text{RTS2}}$/TENA2	AH8[1]
PD27/TXD2	AG7[1]
PD28/RXD2	AE4[1]
PD29/$\overline{\text{RTS1}}$/TENA1	AG1[1]
PD30/TXD1	AD4[1]
PD31/RXD1	AD2[1]
VCCSYN	AB3
VCCSYN1	B9

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
GNDSYN	AB1
CLKIN2	AE11
SPARE4 [2]	U5
$\overline{\text{PCI\_MODE}}$ [3]	AF25
SPARE6[2]	V4
THERMAL0 [4]	AA1
THERMAL1[4]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, this pin should be pulled up or left floating.

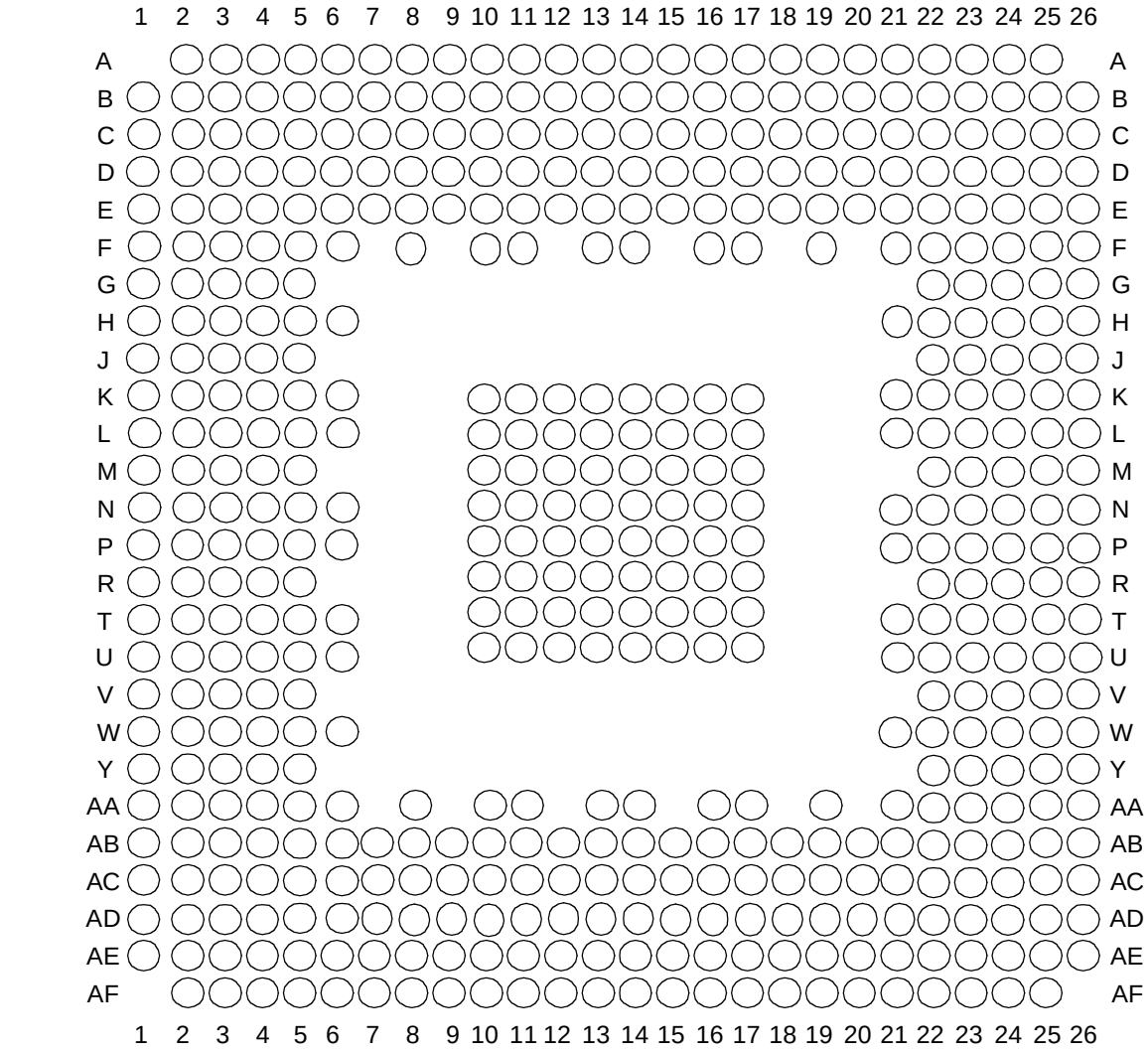
4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D) available at www.freescale.com.

4.2 PBGA Package

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8250, refer to Section 4.1, “TBGA Package.”

4.2.1 PBGA Pin Assignments

Figure 15 shows the pinout of the PBGA package as viewed from the top surface.



Not to Scale

Figure 15. Pinout of the 516 PBGA Package (View from Top)

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
IRQ7/INT_OUT/APE	E5
TRST	F22
TCK	A24
TMS	C24
TDI	A25
TDO	B24
TRIS	C19
PORESET	B25
HRESET	D24
SRESET	E23
QREQ	D18
RSTCONF	E24
MODCK1/AP1/TC0/BNKSEL0	B16
MODCK2/AP2/TC1/BNKSEL1	F16
MODCK3/AP3/TC2/BNKSEL2	A15
XFC	A18
CLKIN1	G22
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC20 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC21[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AF25[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AE24[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AA21[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AD25[1]
PA6	AC24[1]
PA7/SMSYN2	AA22[1]
PA8/SMRXD2	AA23[1]
PA9/SMTXD2	Y26[1]
PA10/MSNUM5	W22[1]
PA11/MSNUM4	W23[1]
PA12/MSNUM3	V26[1]
PA13/MSNUM2	V25[1]
PA14/FCC1_RXD3	T22[1]
PA15/FCC1_RXD2	T25[1]
PA16/FCC1_RXD1	R24[1]
PA17/FCC1_RXD0/FCC1_RXD	P22[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	E22[1]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	E21[1]
PC30/CLK2/TOUT1	D21[1]
PC31/CLK1/BRGO1	B20[1]
PD4/BRGO8/FCC3_RTS/SMRXD2	AF23[1]
PD5/DONE1	AE23[1]
PD6/DACK1	AB21[1]
PD7/SMSYN1/FCC1_TXCLAV2	AD23[1]
PD8/SMRXD1/BRGO5	AD26[1]
PD9/SMTXD1/BRGO3	Y22[1]
PD10/L1CLKOB2/BRGO4	AB24[1]
PD11/L1RQB2	Y23[1]
PD12	AA26[1]
PD13	W24[1]
PD14/L1CLKOC2/I2CSCL	V22[1]
PD15/L1RQC2/I2CSDA	U26[1]
PD16/SPIMISO	T23[1]
PD17/BRGO2/SPIMOSI	R25[1]
PD18/SPICLK	P23[1]
PD19/SPISEL/BRGO1	N22[1]
PD20/RTS4/TENA4/L1RSYNCA2	M25[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	L25[1]
PD22/RXD4L1TXD0A2/L1TXDA2	J26[1]
PD23/RTS3/TENA3	K22[1]
PD24/TXD3	G25[1]
PD25/RXD3	H24[1]
PD26/RTS2/TENA2	F24[1]
PD27/TXD2	H22[1]
PD28/RXD2	B22[1]
PD29/RTS1/TENA1	D22[1]
PD30/TXD1	C21[1]
PD31/RXD1	E19[1]
VCCSYN	D19
VCCSYN1	K6
GNDSYN	B18

5.1 Package Parameters

Package parameters are provided in Table 23.

Table 23. Package Parameters

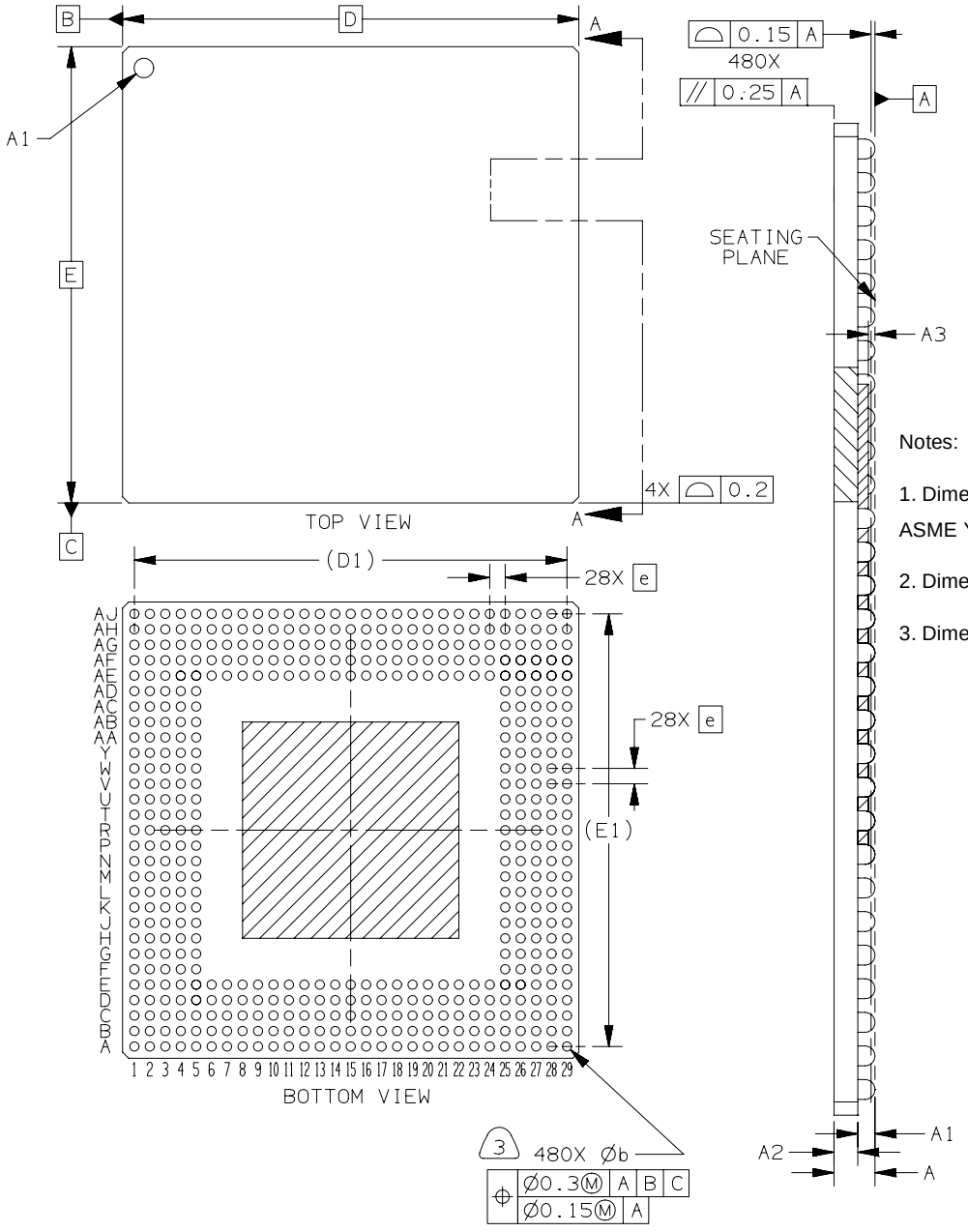
Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8250	37.5 × 37.5	TBGA	480	1.27	1.55
VV			TBGA (Pb free)			
ZO		27 × 27	PBGA	516	1	2.25
VR			PBGA (Pb free)			

5.2 Mechanical Dimensions

This section discusses the TBGA and PBGA package dimensions.

5.2.1 TBGA Package Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

5.2.2 PBGA Package Dimensions

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

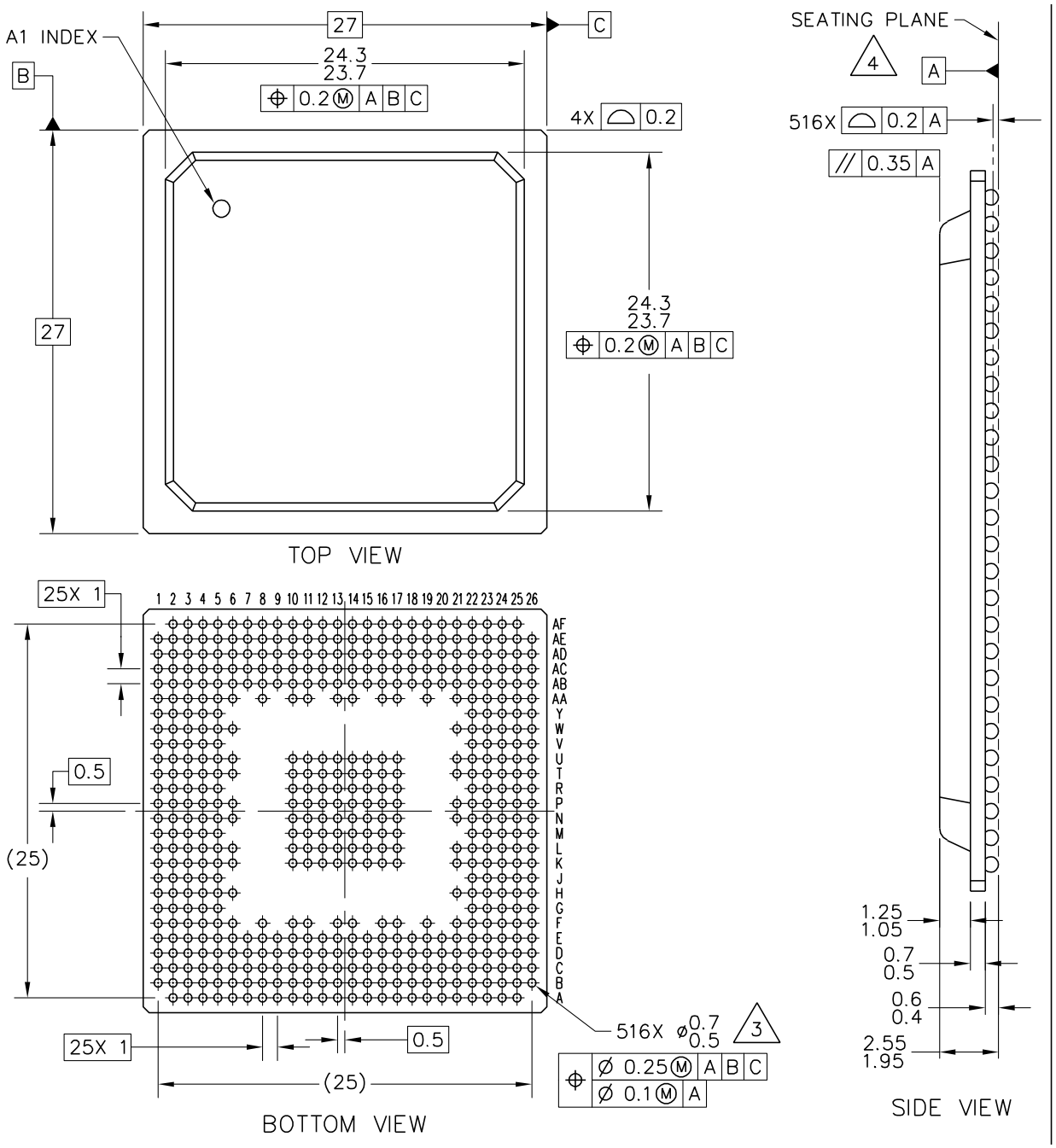


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

Table 24. Document Revision History (continued)

Revision	Date	Substantive Changes
0.6	10/2002	Table 22, “VR Pinout”: corrected ball assignment for the following pins—A12–A17, $\overline{TA}$, PD5, PC2.
0.5	9/2002	Addition of VR (516 PBGA) package information. Refer to sections 2.2, 4.2, and 5.
0.4	5/2002	• Table 2: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 14: Note 3 • Table 16: Note 1 • Table 18: Note 3
0.3	3/2002	• Table 20: modified note to pin AF25.
0.2	3/2202	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.1	2/2002	• Note 2 for Table 4 (changes in italics): “...greater than *or equal to 266* MHz, *200* MHz CPM...” • Table 18: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: footnotes added to pins at AE11, AF25, U5, and V4.
0	11/2001	Initial version

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