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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TJ)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8250avvpibc

Figure 1 shows the block diagram for the MPC8250.

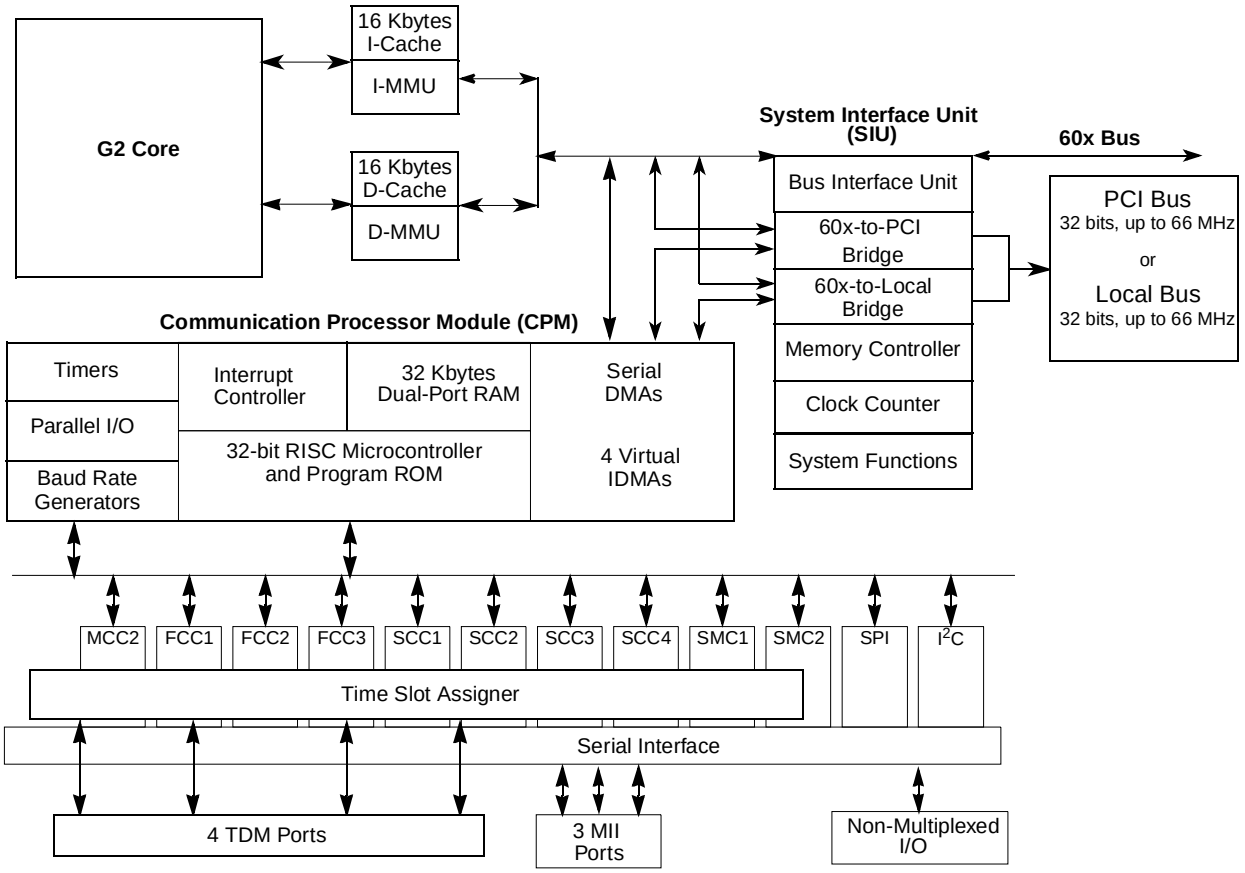


Figure 1. MPC8250 Block Diagram

1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - — A core version of the EC603e microprocessor
  - — System core microprocessor supporting frequencies of 150–200 MHz
  - — Separate 16-Kbyte data and instruction caches:
    - – Four-way set associative
    - – Physically addressed
    - – LRU replacement algorithm
  - — PowerPC architecture-compliant memory management unit (MMU)
  - — Common on-chip processor (COP) test interface
  - — High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)

  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3® CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - One multichannel controller (MCC2)
    - Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    - Transparent
    - UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
    - Microwire compatible
    - Multiple-master, single-master, and slave modes
  - Up to four TDM interfaces
    - Supports one group of four TDM channels

  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

- PCI bridge
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265A) required by the PCI standard as well as message and doorbell registers
  - Supports the I_2O standard
  - Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
  - Support for 66 MHz, 3.3 V specification
  - 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
  - Makes use of the local bus signals, so there is no need for additional pins

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC8250 device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances [1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

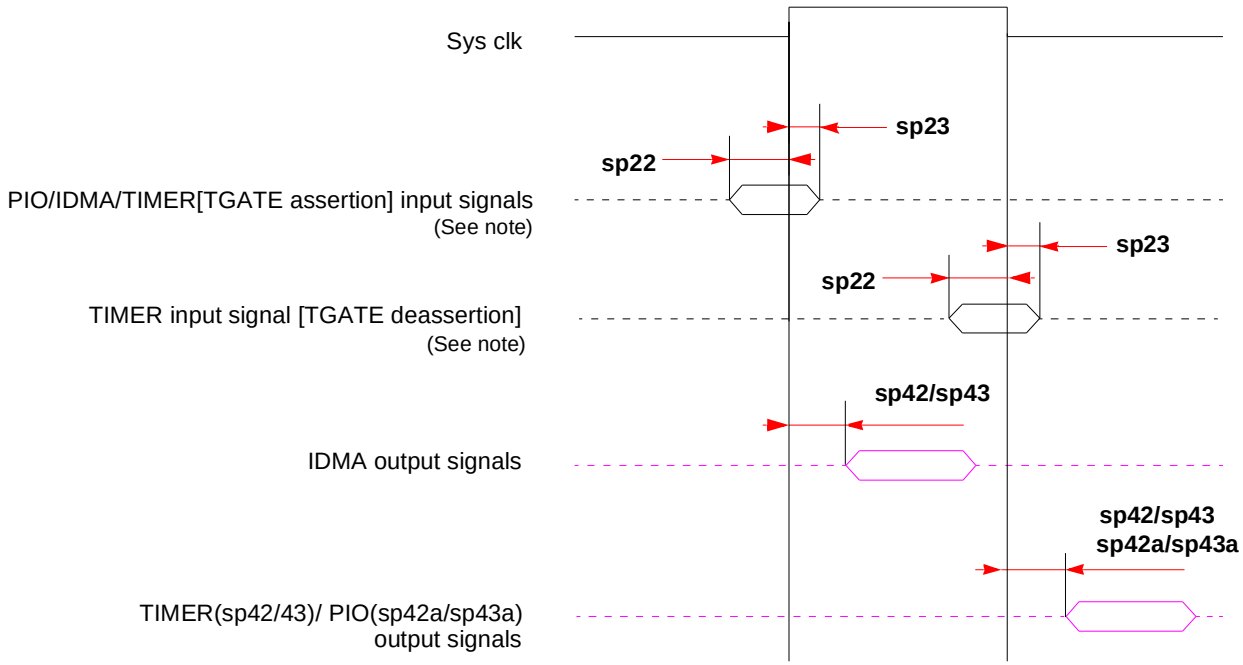
1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 9 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}$/$\overline{\text{ARTRY}}$/$\overline{\text{TA}}$/$\overline{\text{TS}}$/$\overline{\text{TEA}}$/$\overline{\text{DBG}}$/$\overline{\text{BG}}$/$\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{\text{BE0}}$	L28
LCL_DP1/C1/$\overline{\text{BE1}}$	N28
LCL_DP2/C2/$\overline{\text{BE2}}$	T28
LCL_DP3/C3/$\overline{\text{BE3}}$	W28

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1\_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
GNDSYN	AB1
CLKIN2	AE11
SPARE4 [2]	U5
$\overline{\text{PCI\_MODE}}$ [3]	AF25
SPARE6[2]	V4
THERMAL0 [4]	AA1
THERMAL1[4]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 Must be pulled down or left floating.

3 If PCI is not desired, this pin should be pulled up or left floating.

4 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* (AN2271/D) available at www.freescale.com.

4.2 PBGA Package

The following figures and table represent the alternate 516 PBGA package. For information on the standard package for the MPC8250, refer to Section 4.1, “TBGA Package.”

Figure 16 shows the side profile of the PBGA package to indicate the direction of the top surface view.

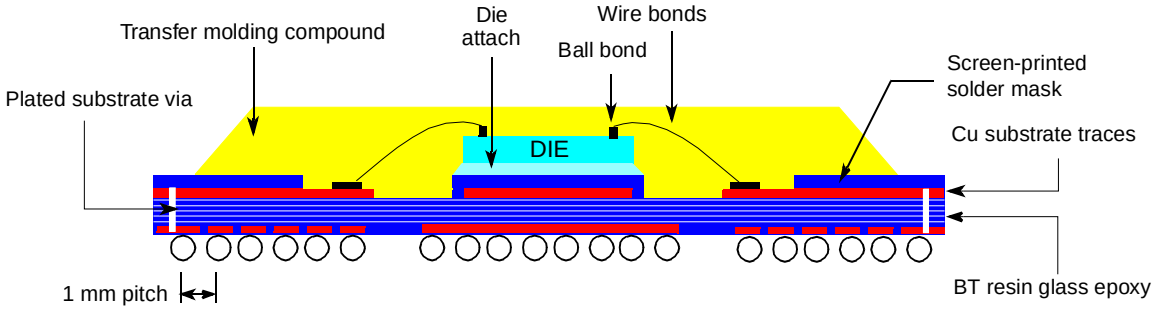


Figure 16. Side View of the PBGA Package

Table 22 shows the pinout list of the PBGA package of the MPC8250. Table 21 defines conventions and acronyms used in Table 22.

Table 21. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 22. MPC8250 PBGA Package Pinout List

Pin Name	Ball
BR	C16
BG	D2
ABB/IRQ2	C1
TS	D1
A0	D5
A1	E8
A2	C4
A3	B4
A4	A4
A5	D7
A6	D8
A7	C6
A8	B5
A9	B6
A10	C7
A11	C8
A12	A6
A13	D9

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
A14	F11
A15	B7
A16	B8
A17	C9
A18	A7
A19	B9
A20	E11
A21	A8
A22	D11
A23	B10
A24	C11
A25	A9
A26	B11
A27	C12
A28	D12
A29	A10
A30	B12
A31	B13
TT0	E7
TT1	B3
TT2	F8
TT3	A3
TT4	C3
TBST	F5
TSIZ0	E3
TSIZ1	E2
TSIZ2	E1
TSIZ3	E4
AACK	D3
ARTRY	C2
DBG	A14
DBB/IRQ3	C15
D0	W4
D1	Y1
D2	V1

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D3	P4
D4	N3
D5	K5
D6	J4
D7	G1
D8	AB1
D9	U4
D10	U2
D11	N6
D12	N1
D13	L1
D14	J5
D15	G3
D16	AA2
D17	W1
D18	T3
D19	T1
D20	M2
D21	K2
D22	J1
D23	G4
D24	U5
D25	T5
D26	P5
D27	P3
D28	M3
D29	K3
D30	H2
D31	G5
D32	AA1
D33	V2
D34	U1
D35	P2
D36	M4
D37	K4

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
POE/PSDRAS/PGPL2	AE1
PSDCAS/PGPL3	AC3
PGTA/PUPMWAIT/PGPL4/PPBS	W6
PSDAMUX/PGPL5	AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0	AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1	AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2	AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3	AF9
LSDA10/LGPL0/PCI_MODCKH0	AB6
LSDWE/LGPL1/PCI_MODCKH1	AF5
LOE/LSDRAS/LGPL2/PCI_MODCKH2	AE5
LSDCAS/LGPL3/PCI_MODCKH3	AD5
LGTA/LUPMWAIT/LGPL4/LPBS	AC5
LGPL5/LSDAMUX/PCI_MODCK	AB5
LWR	AF6
L_A14/PAR	AE13
L_A15/FRAME/SMI	AD15
L_A16/TRDY	AF16
L_A17/IRDY/CKSTP_OUT	AF15
L_A18/STOP	AE15
L_A19/DEVSEL	AE14
L_A20/IDSEL	AC17
L_A21/PERR	AD14
L_A22/SERR	AF13
L_A23/REQ0	AE20
L_A24/REQ1/HSEJSW	AC14
L_A25/GNT0	AC19
L_A26/GNT1/HSLED	AD13
L_A27/GNT2/HSENUM	AF21
L_A28/RST/CORE_SRESET	AF22
L_A29/INTA	AE21
L_A30/REQ2	AB14
L_A31/DLLOUT	AD20
LCL_D0/AD0	AB9
LCL_D1/AD1	AB10

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	H23[1]
PB26/FCC2_MII_CRS/L1RXDC2	C26[1]
PB27/FCC2_MII_COL/L1TXDC2	B26[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1	A22[1]
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	A21[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	E20[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	C20[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/ L1CLKOA2	AE22[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AA19[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AF24[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE25[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AB22[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AC25[1]
PC6/$\overline{\text{FCC1\_CD}}$	AB25[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AA24[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	Y24[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2	U22[1]
PC10/$\overline{\text{CD3}}$/RENA3	V23[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	U23[1]
PC12/$\overline{\text{CD2}}$/RENA2	T26[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	R26[1]
PC14/$\overline{\text{CD1}}$/RENA1	P26[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	P24[1]
PC16/CLK16/TIN4	M26[1]
PC17/CLK15/TIN3/BRGO8	L26[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	M24[1]
PC19/CLK13/BRGO7/SPICLK	L22[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	K25[1]
PC21/CLK11/BRGO6	J25[1]
PC22/CLK10/$\overline{\text{DONE1}}$	G26[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	F26[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	G24[1]
PC25/CLK7/BRGO4	E25[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	G23[1]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3	B23[1]

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PC28/CLK4/TIN1/TOUT2/CTS2/CLSN2	E22[1]
PC29/CLK3/TIN2/BRGO2/CTS1/CLSN1	E21[1]
PC30/CLK2/TOUT1	D21[1]
PC31/CLK1/BRGO1	B20[1]
PD4/BRGO8/FCC3_RTS/SMRXD2	AF23[1]
PD5/DONE1	AE23[1]
PD6/DACK1	AB21[1]
PD7/SMSYN1/FCC1_TXCLAV2	AD23[1]
PD8/SMRXD1/BRGO5	AD26[1]
PD9/SMTXD1/BRGO3	Y22[1]
PD10/L1CLKOB2/BRGO4	AB24[1]
PD11/L1RQB2	Y23[1]
PD12	AA26[1]
PD13	W24[1]
PD14/L1CLKOC2/I2CSCL	V22[1]
PD15/L1RQC2/I2CSDA	U26[1]
PD16/SPIMISO	T23[1]
PD17/BRGO2/SPIMOSI	R25[1]
PD18/SPICLK	P23[1]
PD19/SPISEL/BRGO1	N22[1]
PD20/RTS4/TENA4/L1RSYNCA2	M25[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	L25[1]
PD22/RXD4L1TXD0A2/L1TXDA2	J26[1]
PD23/RTS3/TENA3	K22[1]
PD24/TXD3	G25[1]
PD25/RXD3	H24[1]
PD26/RTS2/TENA2	F24[1]
PD27/TXD2	H22[1]
PD28/RXD2	B22[1]
PD29/RTS1/TENA1	D22[1]
PD30/TXD1	C21[1]
PD31/RXD1	E19[1]
VCCSYN	D19
VCCSYN1	K6
GNDSYN	B18

5.1 Package Parameters

Package parameters are provided in Table 23.

Table 23. Package Parameters

Package	Devices	Outline (mm)	Type	Interconnects	Pitch (mm)	Nominal Unmounted Height (mm)
ZU	MPC8250	37.5 × 37.5	TBGA	480	1.27	1.55
VV			TBGA (Pb free)			
ZO		27 × 27	PBGA	516	1	2.25
VR			PBGA (Pb free)			

5.2 Mechanical Dimensions

This section discusses the TBGA and PBGA package dimensions.

5.2.2 PBGA Package Dimensions

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

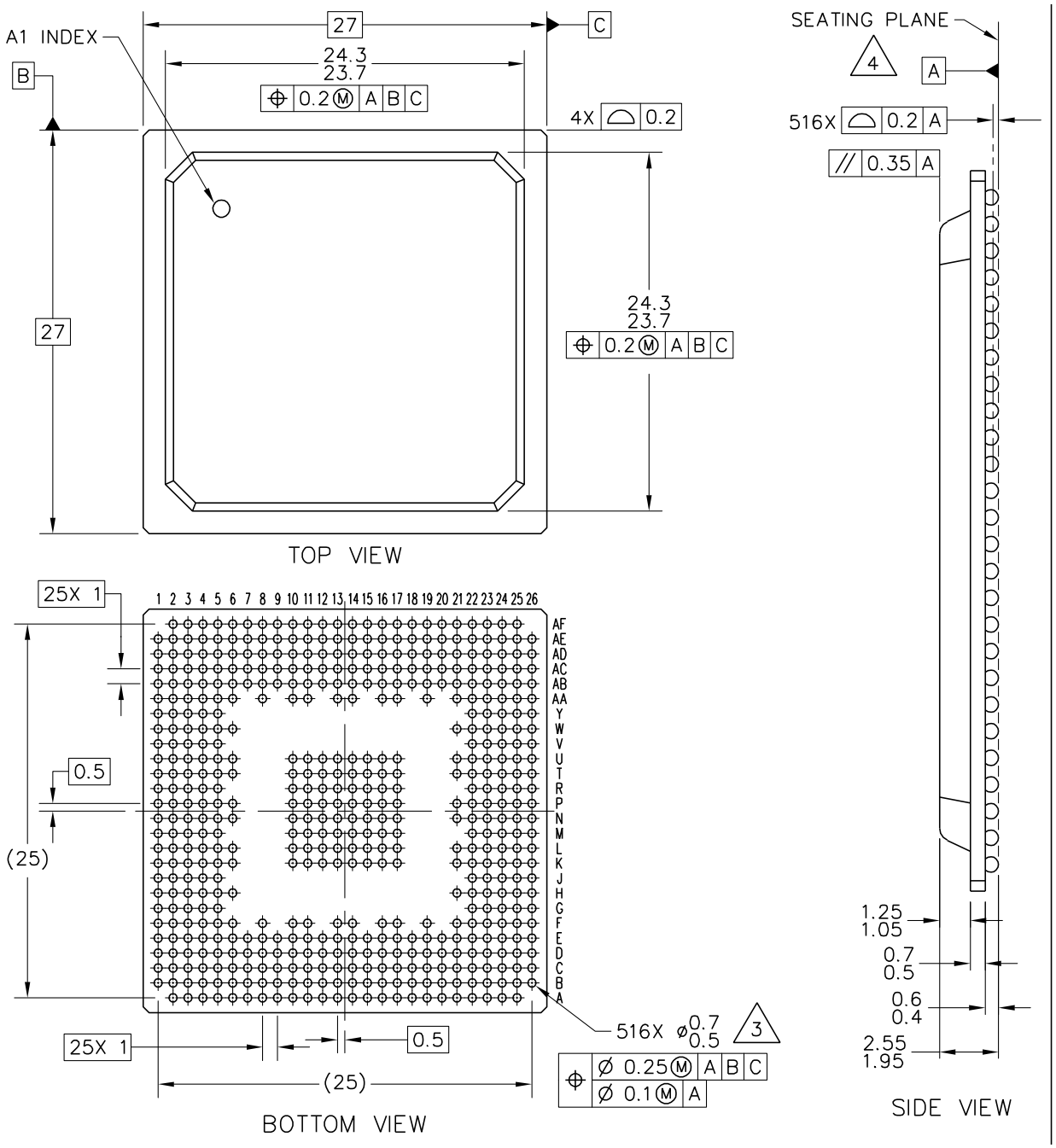


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

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