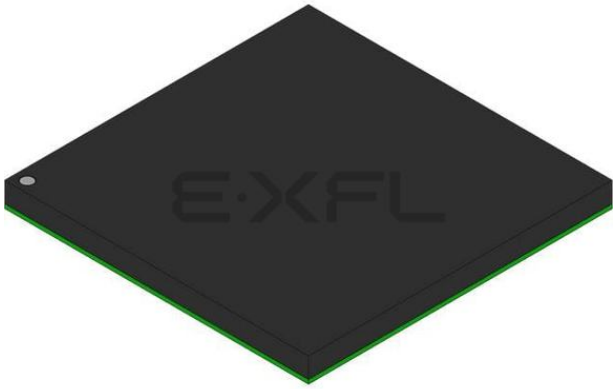

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8250azqihbc

Table 8. AC Characteristics for CPM Inputs [1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

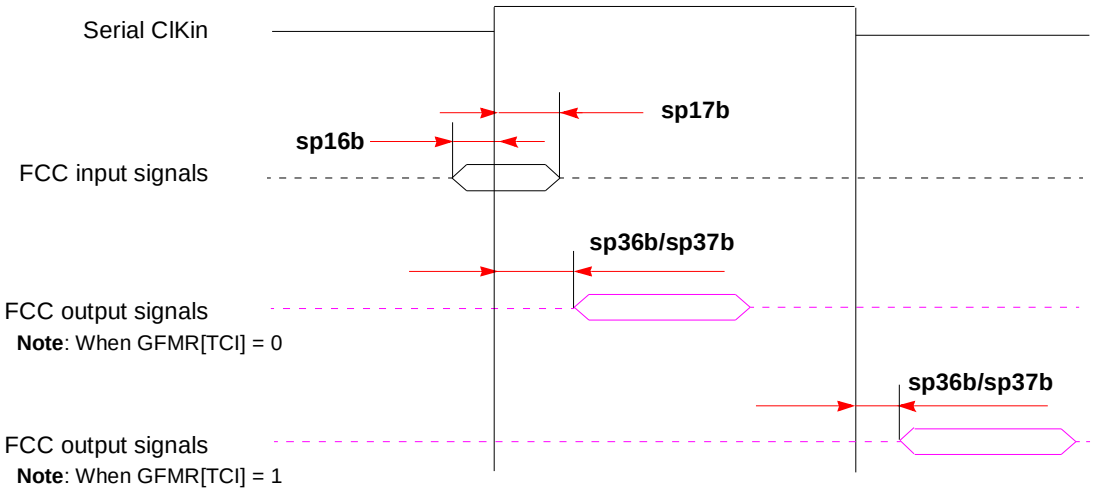


Figure 3. FCC External Clock Diagram

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 11 shows signal behavior in MEMC mode.

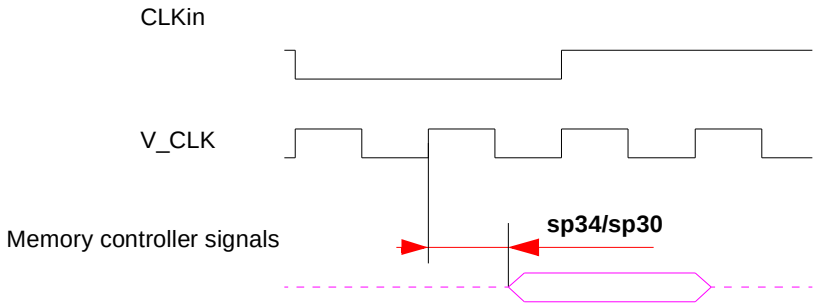


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC8250 bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

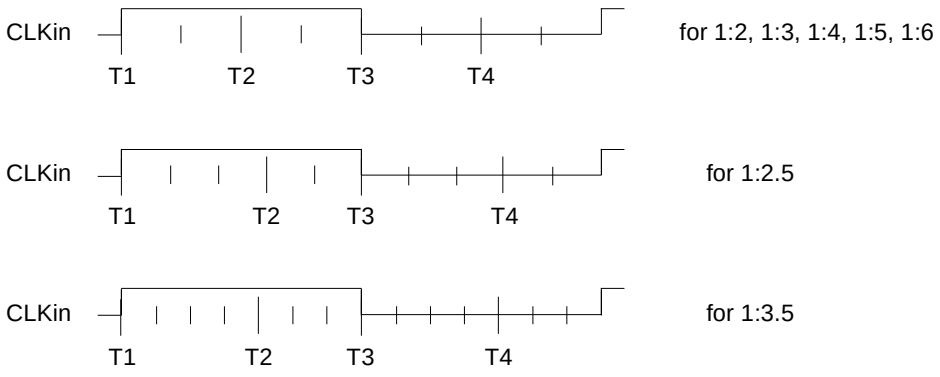


Figure 12. Internal Tick Spacing for Memory Controller Signals

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

The MPC8250 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 12.

Table 12. MPC8250 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 13 and Table 14
0	0	0	PCI host	50–66	Table 15 and Table 16
0	0	1		25–50	
0	1	0	PCI agent	50–66	Table 17 and Table 18
0	1	1		25–50	

1 Determines PCI clock frequency range. Refer to Section 3.2, "PCI Mode."

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected MPC8250 clock operation mode as described in the following sections.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 shows the eight basic clock configurations for the MPC8250. Another 49 configurations are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

Table 13. Clock Default Configurations

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 133 MHz (150 MHz for extended temperature parts) and the CPM ranges between 66–233 MHz.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

3.2 PCI Mode

The PCI mode is selected according to three input pins, as shown in Table 12. In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

1 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to Table 12

3 In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in Table 17 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 17. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor [2]	CPM Frequency	Core Multiplication Factor	Core Frequency [3]	Bus Division Factor	60x Bus Frequency[4]
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 17. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor [2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 Assumes MODCK_HI = 0000.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 12

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency / bus division factor

Table 18 describes all possible clock configurations when using the MPC8250’s internal PCI bridge in agent mode.

Table 18. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**

Table 18. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) [1, 2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000 [5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
LCL_D1/AD1	J29
LCL_D2/AD2	J28
LCL_D3/AD3	J27
LCL_D4/AD4	J26
LCL_D5/AD5	J25
LCL_D6/AD6	K25
LCL_D7/AD7	L29
LCL_D8/AD8	L27
LCL_D9/AD9	L26
LCL_D10/AD10	L25
LCL_D11/AD11	M29
LCL_D12/AD12	M28
LCL_D13/AD13	M27
LCL_D14/AD14	M26
LCL_D15/AD15	N29
LCL_D16/AD16	T25
LCL_D17/AD17	U27
LCL_D18/AD18	U26
LCL_D19/AD19	U25
LCL_D20/AD20	V29
LCL_D21/AD21	V28
LCL_D22/AD22	V27
LCL_D23/AD23	V26
LCL_D24/AD24	W27
LCL_D25/AD25	W26
LCL_D26/AD26	W25
LCL_D27/AD27	Y29
LCL_D28/AD28	Y28
LCL_D29/AD29	Y25
LCL_D30/AD30	AA29
LCL_D31/AD31	AA28
LCL_DP0/C0/$\overline{\text{BE0}}$	L28
LCL_DP1/C1/$\overline{\text{BE1}}$	N28
LCL_DP2/C2/$\overline{\text{BE2}}$	T28
LCL_DP3/C3/$\overline{\text{BE3}}$	W28

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC29 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC25[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AE28[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AG28[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AG26[1]
PA6	AE24[1]
PA7/SMSYN2	AH25[1]
PA8/SMRXD2	AF23[1]
PA9/SMTXD2	AH23[1]
PA10/MSNUM5	AE22[1]
PA11/MSNUM4	AH22[1]
PA12/MSNUM3	AJ21[1]
PA13/MSNUM2	AH20[1]
PA14/FCC1_RXD3	AG19[1]
PA15/FCC1_RXD2	AF18[1]
PA16/FCC1_RXD1	AF17[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PB24/FCC2_TXD2/L1RSYNCC2	AJ9[1]
PB25/FCC2_TXD3/L1TSYNCC2/L1GNTC2	AE9[1]
PB26/FCC2_MII_CRS/L1RXDC2	AJ7[1]
PB27/FCC2_MII_COL/L1TXDC2	AH6[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[1]
PB29/L1RSYNCB2/FCC2_MII_TX_EN	AE2[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	AC5[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	AC4[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/L1CLKOA2	AB26[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AD29[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AE29[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE27[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AF27[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AF24[1]
PC6/$\overline{\text{FCC1\_CD}}$	AJ26[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AJ25[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	AF22[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[1]
PC10/$\overline{\text{CD3}}$/RENA3	AF20[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	AE19[1]
PC12/$\overline{\text{CD2}}$/RENA2	AE18[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	AH18[1]
PC14/$\overline{\text{CD1}}$/RENA1	AH17[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	AG16[1]
PC16/CLK16/TIN4	AF15[1]
PC17/CLK15/TIN3/BRGO8	AJ15[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[1]
PC19/CLK13/BRGO7/SPICLK	AG13[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[1]
PC21/CLK11/BRGO6	AJ11[1]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	AF9[1]
PC25/CLK7/BRGO4	AE8[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[1]

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[1]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[1]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[1]
PC30/CLK2/$\overline{\text{TOUT1}}$	AE1[1]
PC31/CLK1/BRGO1	AD1[1]
PD4/BRGO8/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[1]
PD5/$\overline{\text{DONE1}}$	AD27[1]
PD6/$\overline{\text{DACK1}}$	AF29[1]
PD7/SMSYN1FCC1_TXCLAV2	AF28[1]
PD8/SMRXD1/BRGO5	AG25[1]
PD9/SMTXD1/BRGO3	AH26[1]
PD10/L1CLKOB2/BRGO4	AJ27[1]
PD11/$\overline{\text{L1RQB2}}$	AJ23[1]
PD12	AG23[1]
PD13	AJ22[1]
PD14/L1CLKOC2/I2CSCL	AE20[1]
PD15/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[1]
PD16/SPIMISO	AG18[1]
PD17/BRGO2/SPIMOSI	AG17[1]
PD18/SPICLK	AF16[1]
PD19/SPISEL/BRGO	AH15[1]
PD20/$\overline{\text{RTS4}}$/TENA4/L1RSYNCA2	AJ14[1]
PD21/TXD4/L1RXD0A2/L1RXDA2	AH13[1]
PD22/RXD4/L1TXD0A2/L1TXDA2	AJ12[1]
PD23/$\overline{\text{RTS3}}$/TENA3	AE12[1]
PD24/TXD3	AF10[1]
PD25/RXD3	AG9[1]
PD26/$\overline{\text{RTS2}}$/TENA2	AH8[1]
PD27/TXD2	AG7[1]
PD28/RXD2	AE4[1]
PD29/$\overline{\text{RTS1}}$/TENA1	AG1[1]
PD30/TXD1	AD4[1]
PD31/RXD1	AD2[1]
VCCSYN	AB3
VCCSYN1	B9

Table 22. MPC8250 PBGA Package Pinout List (continued)

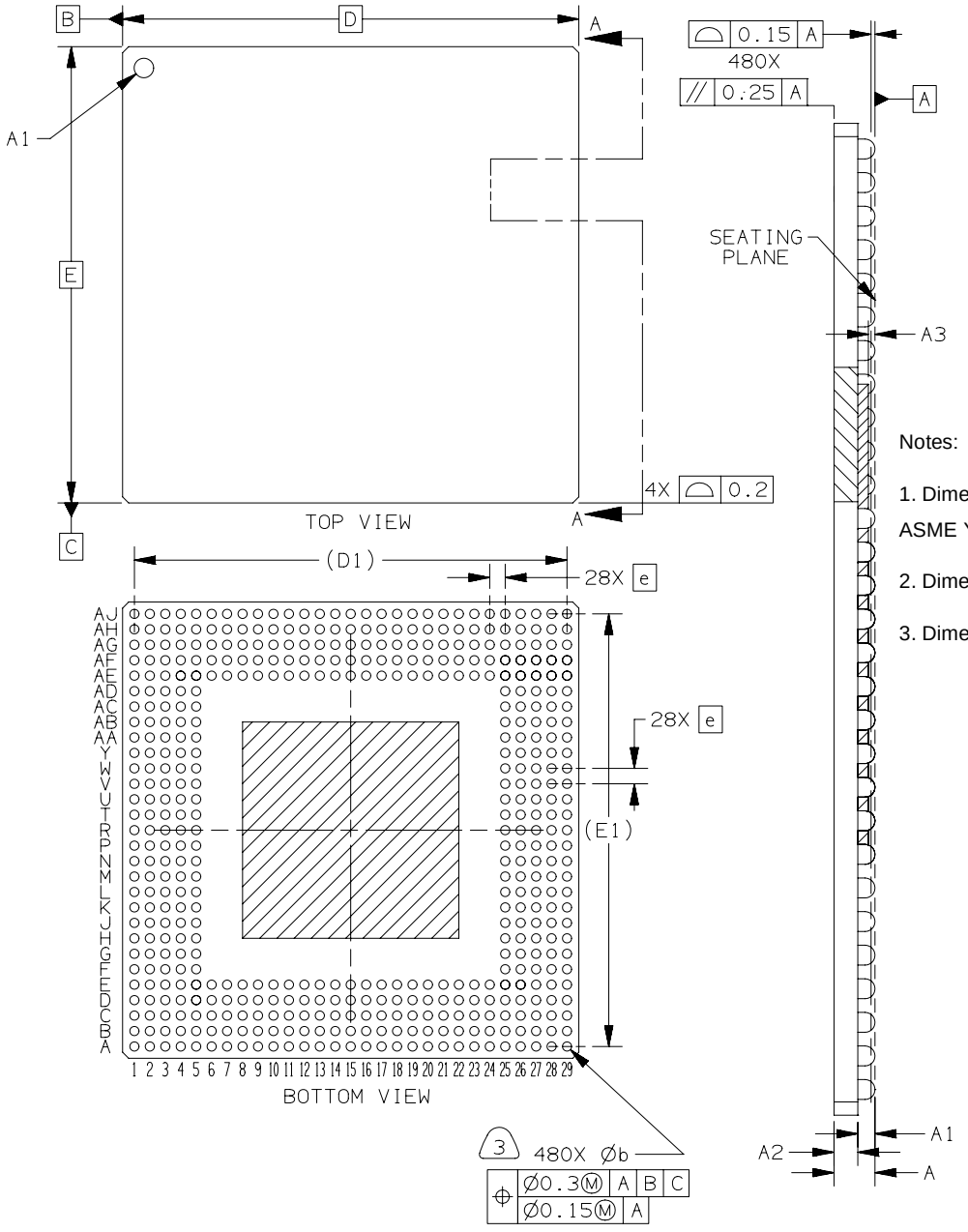
Pin Name	Ball
POE/PSDRAS/PGPL2	AE1
PSDCAS/PGPL3	AC3
PGTA/PUPMWAIT/PGPL4/PPBS	W6
PSDAMUX/PGPL5	AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0	AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1	AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2	AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3	AF9
LSDA10/LGPL0/PCI_MODCKH0	AB6
LSDWE/LGPL1/PCI_MODCKH1	AF5
LOE/LSDRAS/LGPL2/PCI_MODCKH2	AE5
LSDCAS/LGPL3/PCI_MODCKH3	AD5
LGTA/LUPMWAIT/LGPL4/LPBS	AC5
LGPL5/LSDAMUX/PCI_MODCK	AB5
LWR	AF6
L_A14/PAR	AE13
L_A15/FRAME/SMI	AD15
L_A16/TRDY	AF16
L_A17/IRDY/CKSTP_OUT	AF15
L_A18/STOP	AE15
L_A19/DEVSEL	AE14
L_A20/IDSEL	AC17
L_A21/PERR	AD14
L_A22/SERR	AF13
L_A23/REQ0	AE20
L_A24/REQ1/HSEJSW	AC14
L_A25/GNT0	AC19
L_A26/GNT1/HSLED	AD13
L_A27/GNT2/HSENUM	AF21
L_A28/RST/CORE_SRESET	AF22
L_A29/INTA	AE21
L_A30/REQ2	AB14
L_A31/DLLOUT	AD20
LCL_D0/AD0	AB9
LCL_D1/AD1	AB10

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
IRQ7/INT_OUT/APE	E5
TRST	F22
TCK	A24
TMS	C24
TDI	A25
TDO	B24
TRIS	C19
PORESET	B25
HRESET	D24
SRESET	E23
QREQ	D18
RSTCONF	E24
MODCK1/AP1/TC0/BNKSEL0	B16
MODCK2/AP2/TC1/BNKSEL1	F16
MODCK3/AP3/TC2/BNKSEL2	A15
XFC	A18
CLKIN1	G22
PA0/$\overline{\text{RESTART1}}$/DREQ3	AC20 [1]
PA1/$\overline{\text{REJECT1}}$/$\overline{\text{DONE3}}$	AC21[1]
PA2/CLK20/$\overline{\text{DACK3}}$	AF25[1]
PA3/CLK19/$\overline{\text{DACK4}}$/L1RXD1A2	AE24[1]
PA4/$\overline{\text{REJECT2}}$/$\overline{\text{DONE4}}$	AA21[1]
PA5/$\overline{\text{RESTART2}}$/DREQ4	AD25[1]
PA6	AC24[1]
PA7/SMSYN2	AA22[1]
PA8/SMRXD2	AA23[1]
PA9/SMTXD2	Y26[1]
PA10/MSNUM5	W22[1]
PA11/MSNUM4	W23[1]
PA12/MSNUM3	V26[1]
PA13/MSNUM2	V25[1]
PA14/FCC1_RXD3	T22[1]
PA15/FCC1_RXD2	T25[1]
PA16/FCC1_RXD1	R24[1]
PA17/FCC1_RXD0/FCC1_RXD	P22[1]

5.2.1 TBGA Package Dimensions

Figure 17 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 17. Mechanical Dimensions and Bottom Surface Nomenclature—480 TBGA

5.2.2 PBGA Package Dimensions

Figure 18 provides the mechanical dimensions and bottom surface nomenclature of the 516 PBGA package.

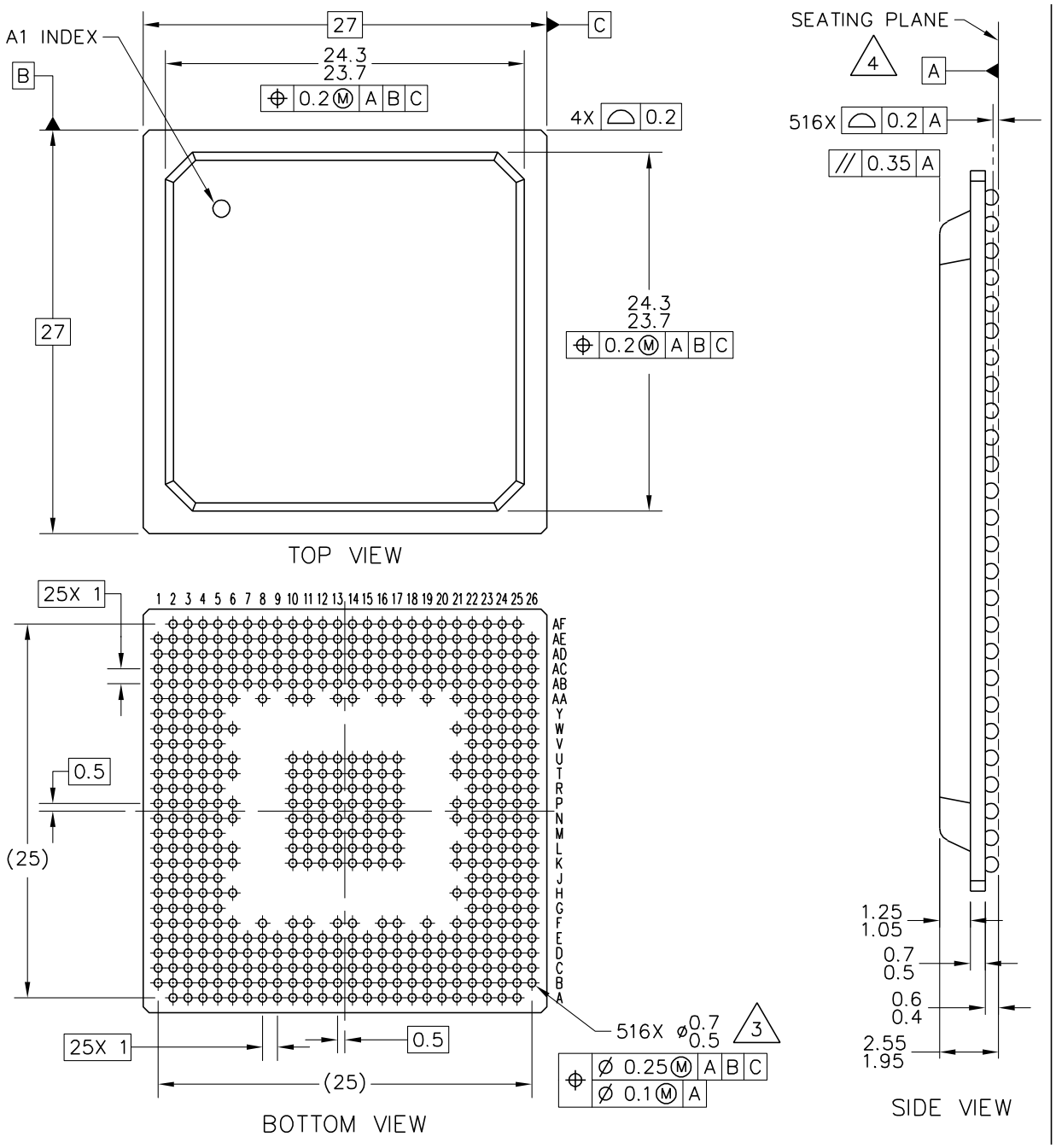


Figure 18. Mechanical Dimensions and Bottom Surface Nomenclature—516 PBGA

Table 24. Document Revision History (continued)

Revision	Date	Substantive Changes
0.6	10/2002	Table 22, “VR Pinout”: corrected ball assignment for the following pins—A12–A17, $\overline{TA}$, PD5, PC2.
0.5	9/2002	Addition of VR (516 PBGA) package information. Refer to sections 2.2, 4.2, and 5.
0.4	5/2002	• Table 2: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 14: Note 3 • Table 16: Note 1 • Table 18: Note 3
0.3	3/2002	• Table 20: modified note to pin AF25.
0.2	3/2202	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.1	2/2002	• Note 2 for Table 4 (changes in italics): “...greater than *or equal to 266* MHz, *200* MHz CPM...” • Table 18: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: footnotes added to pins at AE11, AF25, U5, and V4.
0	11/2001	Initial version

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