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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8250azupibc

Figure 1 shows the block diagram for the MPC8250.

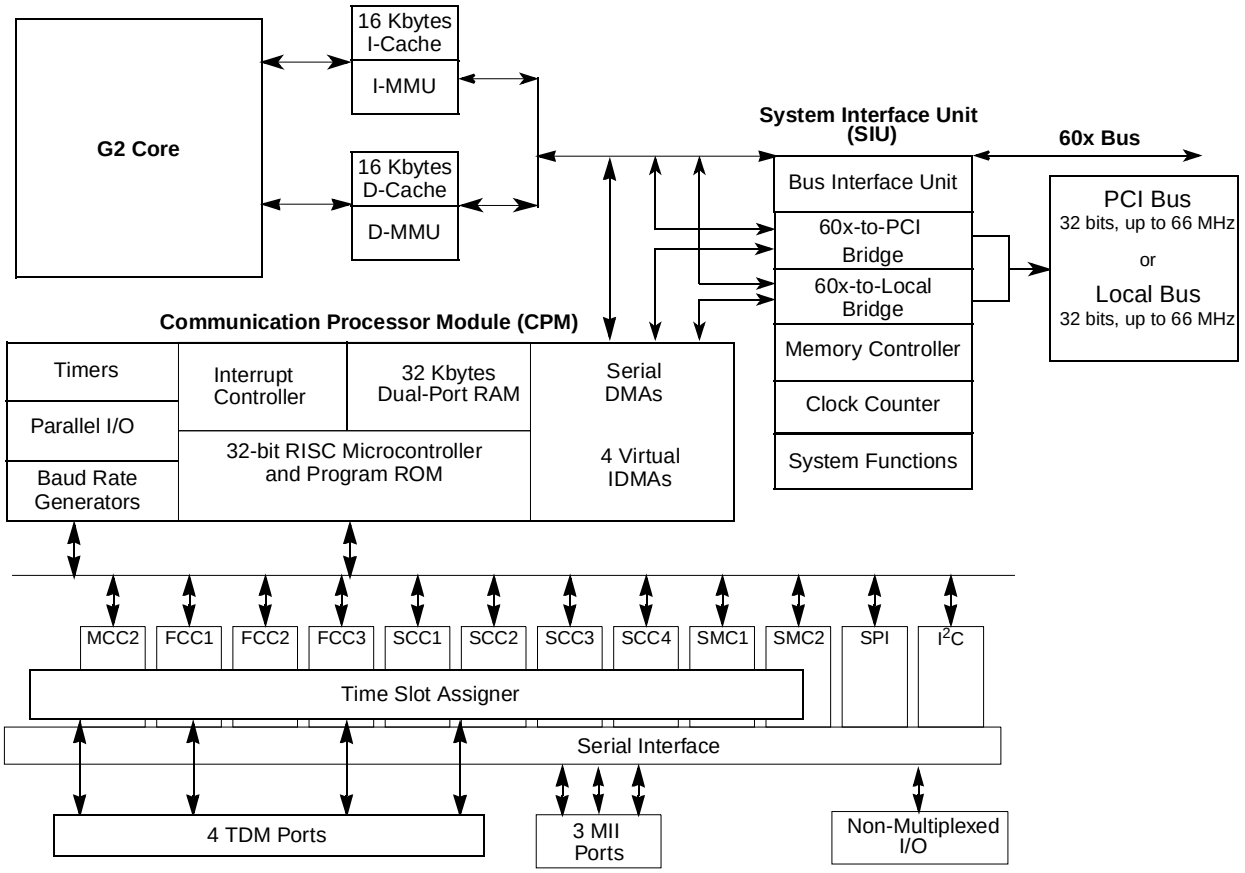

Figure 1. MPC8250 Block Diagram

1 Features

The major features of the MPC8250 are as follows:

- Footprint-compatible with the MPC8260
- Dual-issue integer core
  - — A core version of the EC603e microprocessor
  - — System core microprocessor supporting frequencies of 150–200 MHz
  - — Separate 16-Kbyte data and instruction caches:
    - – Four-way set associative
    - – Physically addressed
    - – LRU replacement algorithm
  - — PowerPC architecture-compliant memory management unit (MMU)
  - — Common on-chip processor (COP) test interface
  - — High-performance (4.4–5.1 SPEC95 benchmark at 200 MHz; 280 Dhrystones MIPS at 200 MHz)

  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols:
    - 10/100-Mbit Ethernet/IEEE 802.3® CDMA/CS interface through media independent interface (MII)
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - One multichannel controller (MCC2)
    - Handles 128 serial, full-duplex, 64-Kbps data channels. The MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels
    - Transparent
    - UART (low-speed operation)
  - One serial peripheral interface identical to the MPC860 SPI
  - One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
    - Microwire compatible
    - Multiple-master, single-master, and slave modes
  - Up to four TDM interfaces
    - Supports one group of four TDM channels

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

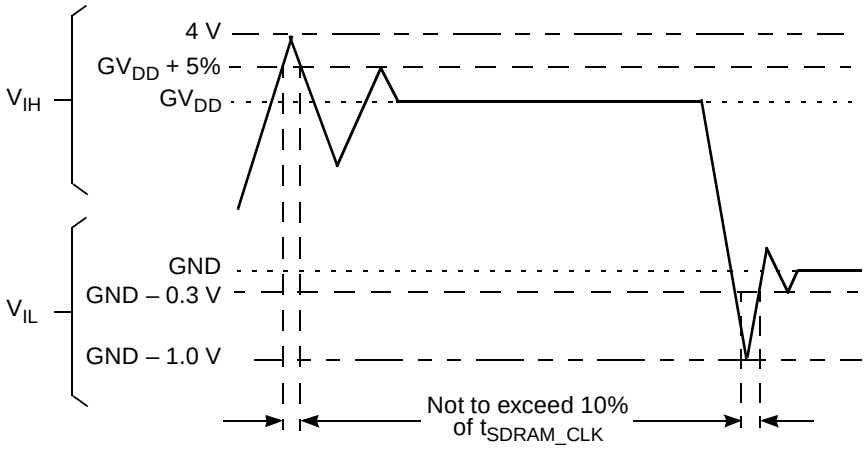

Figure 2. Overshoot/Undershoot Voltage

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics [1]

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, V_{IN} = VDDH [2]	I_{IN}	—	10	µA
Hi-Z (off state) leakage current, V_{IN} = VDDH[2]	I_{OZ}	—	10	µA
Signal low input current, V_{IL} = 0.8 V	I_L	—	1	µA
Signal high input current, V_{IH} = 2.0 V	I_H	—	1	µA
Output high voltage, I_{OH} = –2 mA	V_{OH}	2.4	—	V

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 The leakage current is measured for nominal VDD, VCCSYN, and VDD.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics

Characteristic	Symbol	Value		Unit	Air Flow
		480 TBGA	516 PBGA		
Junction to ambient—single-layer board [1]	θ_{JA}	13	24	°C/W	Natural convection
		10	18		1 m/s
Junction to ambient—four-layer board		11	16		Natural convection
		8	13		1 m/s
Junction to board [2]	θ_{JB}	4	8	°C/W	—
Junction to case [3]	θ_{JC}	1.1	6	°C/W	—

1 Assumes no thermal vias

2 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \quad (3)$$

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs [1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

The MPC8250 has three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 12.

Table 12. MPC8250 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHZ)	Reference
PCI_MODE	PCI_CFG[0]	PCI_MODCK[1]			
1	—	—	Local bus	—	Table 13 and Table 14
0	0	0	PCI host	50–66	Table 15 and Table 16
0	0	1		25–50	
0	1	0	PCI agent	50–66	Table 17 and Table 18
0	1	1		25–50	

1 Determines PCI clock frequency range. Refer to Section 3.2, "PCI Mode."

In each clocking mode, the configuration of bus, core, PCI, and CPM frequencies is determined by seven bits during the power-up reset—three hardware configuration pins (MODCK[1–3]) and four bits from hardware configuration word[28–31] (MODCK_H). Both the PLLs and the dividers are set according to the selected MPC8250 clock operation mode as described in the following sections.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 shows the eight basic clock configurations for the MPC8250. Another 49 configurations are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four pins on the data bus.

Table 13. Clock Default Configurations

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz

Table 14. Clock Configuration Modes [1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

1 Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

2 The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 133 MHz (150 MHz for extended temperature parts) and the CPM ranges between 66–233 MHz.

3 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

3.2 PCI Mode

The PCI mode is selected according to three input pins, as shown in Table 12. In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

Table 16. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency [1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor [2]	PCI Frequency[2]
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11

Table 20. MPC8250 TBGA Package Pinout List (continued)

Pin Name	Ball
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3	G29
LSDA10/LGPL0/PCI_MODCKH0	D27
LSDWE/LGPL1/PCI_MODCKH1	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2	E26
LSDCAS/LGPL3/PCI_MODCKH3	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK	B27
LWR	D28
L_A14/PAR	N27
L_A15/FRAME/SMI	T29
L_A16/TRDY	R27
L_A17/IRDY/CKSTP_OUT	R26
L_A18/STOP	R29
L_A19/DEVSEL	R28
L_A20/IDSEL	W29
L_A21/PERR	P28
L_A22/SERR	N26
L_A23/REQ0	AA27
L_A24/REQ1/HSEJSW	P29
L_A25/GNT0	AA26
L_A26/GNT1/HSLED	N25
L_A27/GNT2/HSENUM	AA25
L_A28/RST/CORE_SRESET	AB29
L_A29/INTA	AB28
L_A30/REQ2	P25
L_A31/DLLOUT	AB27
LCL_D0/AD0	H29

Figure 16 shows the side profile of the PBGA package to indicate the direction of the top surface view.

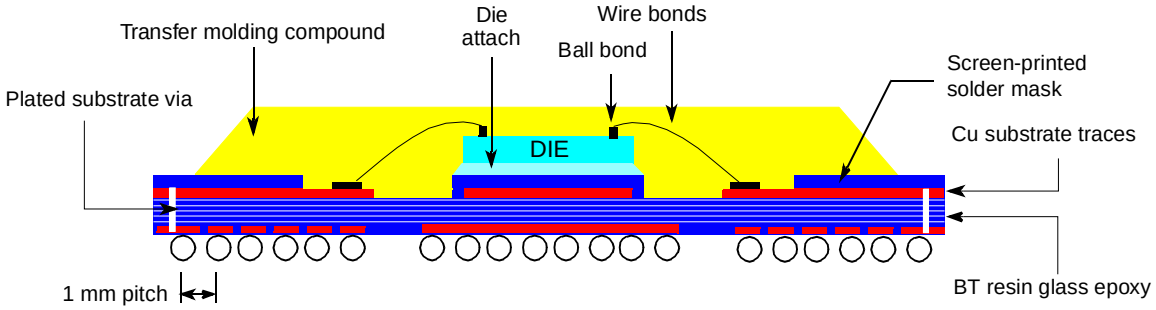

Figure 16. Side View of the PBGA Package

Table 22 shows the pinout list of the PBGA package of the MPC8250. Table 21 defines conventions and acronyms used in Table 22.

Table 21. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
MII	Indicates that a signal is part of the media independent interface.

Table 22. MPC8250 PBGA Package Pinout List

Pin Name	Ball
BR	C16
BG	D2
ABB/IRQ2	C1
TS	D1
A0	D5
A1	E8
A2	C4
A3	B4
A4	A4
A5	D7
A6	D8
A7	C6
A8	B5
A9	B6
A10	C7
A11	C8
A12	A6
A13	D9

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
A14	F11
A15	B7
A16	B8
A17	C9
A18	A7
A19	B9
A20	E11
A21	A8
A22	D11
A23	B10
A24	C11
A25	A9
A26	B11
A27	C12
A28	D12
A29	A10
A30	B12
A31	B13
TT0	E7
TT1	B3
TT2	F8
TT3	A3
TT4	C3
TBST	F5
TSIZ0	E3
TSIZ1	E2
TSIZ2	E1
TSIZ3	E4
AACK	D3
ARTRY	C2
DBG	A14
DBB/IRQ3	C15
D0	W4
D1	Y1
D2	V1

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D3	P4
D4	N3
D5	K5
D6	J4
D7	G1
D8	AB1
D9	U4
D10	U2
D11	N6
D12	N1
D13	L1
D14	J5
D15	G3
D16	AA2
D17	W1
D18	T3
D19	T1
D20	M2
D21	K2
D22	J1
D23	G4
D24	U5
D25	T5
D26	P5
D27	P3
D28	M3
D29	K3
D30	H2
D31	G5
D32	AA1
D33	V2
D34	U1
D35	P2
D36	M4
D37	K4

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
D38	H3
D39	F2
D40	Y2
D41	U3
D42	T2
D43	N2
D44	M5
D45	K1
D46	H4
D47	F1
D48	W2
D49	T4
D50	R3
D51	N4
D52	M1
D53	J2
D54	H5
D55	F3
D56	V3
D57	R5
D58	R2
D59	N5
D60	L2
D61	J3
D62	H1
D63	F4
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	AB3
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	W5
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	AC2
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	AA3
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	AD1
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	AC1
$\overline{\text{IRQ6}}$/DP6/CSE0	AB2
$\overline{\text{IRQ7}}$/DP7/CSE1	Y3
PSDVAL	D15

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
POE/PSDRAS/PGPL2	AE1
PSDCAS/PGPL3	AC3
PGTA/PUPMWAIT/PGPL4/PPBS	W6
PSDAMUX/PGPL5	AA4
LWE0/LSDDQM0/LBS0/PCI_CFG0	AC9
LWE1/LSDDQM1/LBS1/PCI_CFG1	AD9
LWE2/LSDDQM2/LBS2/PCI_CFG2	AE9
LWE3/LSDDQM3/LBS3/PCI_CFG3	AF9
LSDA10/LGPL0/PCI_MODCKH0	AB6
LSDWE/LGPL1/PCI_MODCKH1	AF5
LOE/LSDRAS/LGPL2/PCI_MODCKH2	AE5
LSDCAS/LGPL3/PCI_MODCKH3	AD5
LGTA/LUPMWAIT/LGPL4/LPBS	AC5
LGPL5/LSDAMUX/PCI_MODCK	AB5
LWR	AF6
L_A14/PAR	AE13
L_A15/FRAME/SMI	AD15
L_A16/TRDY	AF16
L_A17/IRDY/CKSTP_OUT	AF15
L_A18/STOP	AE15
L_A19/DEVSEL	AE14
L_A20/IDSEL	AC17
L_A21/PERR	AD14
L_A22/SERR	AF13
L_A23/REQ0	AE20
L_A24/REQ1/HSEJSW	AC14
L_A25/GNT0	AC19
L_A26/GNT1/HSLED	AD13
L_A27/GNT2/HSENUM	AF21
L_A28/RST/CORE_SRESET	AF22
L_A29/INTA	AE21
L_A30/REQ2	AB14
L_A31/DLLOUT	AD20
LCL_D0/AD0	AB9
LCL_D1/AD1	AB10

Table 22. MPC8250 PBGA Package Pinout List (continued)

Pin Name	Ball
PB25/FCC2_TXD3/L1TSYNCC2/ L1GNTC2	H23[1]
PB26/FCC2_MII_CRS/L1RXDC2	C26[1]
PB27/FCC2_MII_COL/L1TXDC2	B26[1]
PB28/FCC2_MII_RX_ER/$\overline{\text{FCC2\_RTS}}$/ L1TSYNCB2/L1GNTB2/TXD1	A22[1]
PB29/L1RSYNCB2/ FCC2_MII_TX_EN	A21[1]
PB30/FCC2_MII_RX_DV/L1RXDB2	E20[1]
PB31/FCC2_MII_TX_ER/L1TXDB2	C20[1]
PC0/DREQ1/BRGO7/$\overline{\text{SMSYN2}}$/ L1CLKOA2	AE22[1]
PC1/DREQ2/BRGO6/$\overline{\text{L1RQA2}}$	AA19[1]
PC2/$\overline{\text{FCC3\_CD}}$/$\overline{\text{DONE2}}$	AF24[1]
PC3/$\overline{\text{FCC3\_CTS}}$/$\overline{\text{DACK2}}$/$\overline{\text{CTS4}}$	AE25[1]
PC4/SI2_L1ST4/$\overline{\text{FCC2\_CD}}$	AB22[1]
PC5/SI2_L1ST3/$\overline{\text{FCC2\_CTS}}$	AC25[1]
PC6/$\overline{\text{FCC1\_CD}}$	AB25[1]
PC7/$\overline{\text{FCC1\_CTS}}$	AA24[1]
PC8/$\overline{\text{CD4}}$/RENA4/SI2_L1ST2/$\overline{\text{CTS3}}$	Y24[1]
PC9/$\overline{\text{CTS4}}$/CLSN4/SI2_L1ST1/ L1TSYNCA2/L1GNTA2	U22[1]
PC10/$\overline{\text{CD3}}$/RENA3	V23[1]
PC11/$\overline{\text{CTS3}}$/CLSN3/L1TXD3A2	U23[1]
PC12/$\overline{\text{CD2}}$/RENA2	T26[1]
PC13/$\overline{\text{CTS2}}$/CLSN2	R26[1]
PC14/$\overline{\text{CD1}}$/RENA1	P26[1]
PC15/$\overline{\text{CTS1}}$/CLSN1/SMTXD2	P24[1]
PC16/CLK16/TIN4	M26[1]
PC17/CLK15/TIN3/BRGO8	L26[1]
PC18/CLK14/$\overline{\text{TGATE2}}$	M24[1]
PC19/CLK13/BRGO7/SPICLK	L22[1]
PC20/CLK12/$\overline{\text{TGATE1}}$	K25[1]
PC21/CLK11/BRGO6	J25[1]
PC22/CLK10/$\overline{\text{DONE1}}$	G26[1]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	F26[1]
PC24/CLK8/$\overline{\text{TOUT4}}$	G24[1]
PC25/CLK7/BRGO4	E25[1]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	G23[1]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/ BRGO3	B23[1]

6 Ordering Information

Figure 19 provides an example of the Freescale part numbering nomenclature for the MPC8250. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

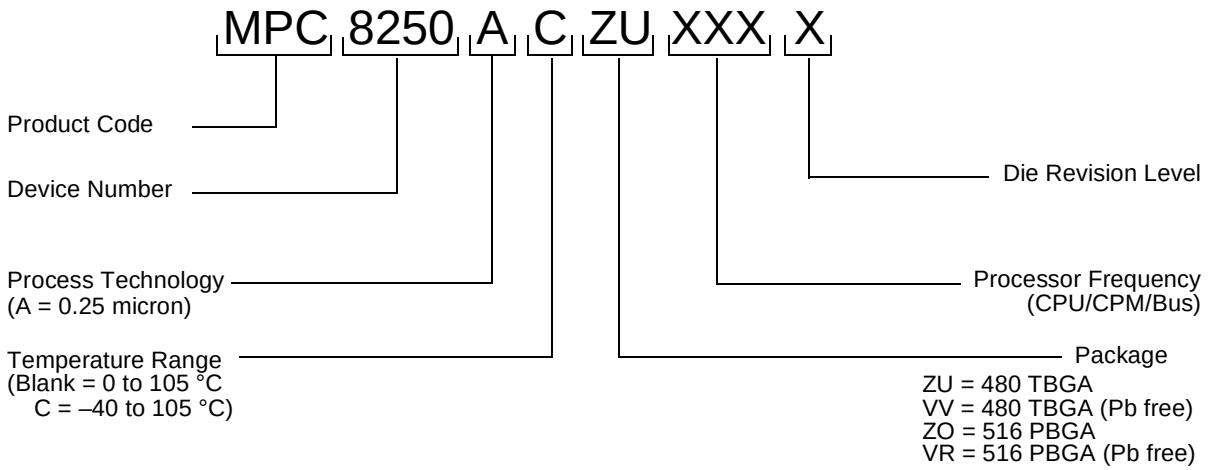

Figure 19. Freescale Part Number Key

7 Document Revision History

Table 24 provides a revision history for this template.

Table 24. Document Revision History

Revision	Date	Substantive Changes
2	7/2009	Updated TBGA and PBGA packaging information.
1	3/2005	Document template update
0.9	8/2003	• Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4 • Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 • Addition of Figure 2 • Addition of note 1 to Table 3 • Table 4: Changes to θ_{JA}. Addition of θ_{JB} and θ_{JC} • Table 7, Figure 8: Addition of sp42a/sp43a • Figure 3 through Figure 8: Addition of notes or modifications • Table 9: Change to sp10 • Table 14, Table 16, and Table 18: Removal of PLL bypass mode from clock tables • Table 20 and Table 22: Addition of note 1 • Addition of SPICLK to PC19 in Table 20 and Table 22. It is documented correctly in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 20 and Table 22.
0.8	11/2002	Table 22, “VR Pinout”: Addition of C18 to the Ground (GND) pin list (page 53)
0.7	10/2002	Table 22, “VR Pinout”: Addition of L3 to the Core (VDDx) pin list (page 53)

Table 24. Document Revision History (continued)

Revision	Date	Substantive Changes
0.6	10/2002	Table 22, “VR Pinout”: corrected ball assignment for the following pins—A12–A17, $\overline{TA}$, PD5, PC2.
0.5	9/2002	Addition of VR (516 PBGA) package information. Refer to sections 2.2, 4.2, and 5.
0.4	5/2002	• Table 2: Notes 2 and 3 • Addition of note on page 8:VDDH and VDD tracking • Table 14: Note 3 • Table 16: Note 1 • Table 18: Note 3
0.3	3/2002	• Table 20: modified note to pin AF25.
0.2	3/2202	• Table 20: modified notes to pins AE11 and AF25. • Table 20: added note to pins AA1 and AG4 (Therm0 and Therm1).
0.1	2/2002	• Note 2 for Table 4 (changes in italics): “...greater than *or equal to 266* MHz, *200* MHz CPM...” • Table 18: core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 20: footnotes added to pins at AE11, AF25, U5, and V4.
0	11/2001	Initial version

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