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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f18325-e-jq

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F18345) (CONTINUED)

I/O ⁽²⁾	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN ⁽¹⁾	—	CCP2 ⁽¹⁾	—	—	—	—	CLCIN1 ⁽¹⁾	—	IOC	Y	—
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 ⁽¹⁾	—	CCP1 ⁽¹⁾	—	—	—	—	—	—	IOC	Y	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS1 ⁽¹⁾	—	—	—	IOC	Y	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	—	—	C1OUT	NCO1	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT	CLC1OUT	CLKR	—	—	—
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1 ⁽³⁾ SCL2 ⁽³⁾	TX	CLC3OUT	—	—	—	—
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1 ⁽³⁾ SDA2 ⁽³⁾	—	CLC4OUT	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
 - 4: These pins are configured for I²C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

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TABLE 1-3: PIC16(L)F18345 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC3/ANC3/C1IN3-/C2IN3-/MDMIN ⁽¹⁾ /CCP2 ⁽¹⁾ /CLCIN1 ⁽¹⁾ /	RC3	TTL/ST	CMOS	General purpose I/O.
	ANC3	AN	—	ADC Channel C3 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	MDMIN	TTL/ST	—	Modular Source input.
	CCP2	TTL/ST	CMOS	Capture/Compare/PWM 2 input.
	CLCIN1	TTL/ST	—	Configurable Logic Cell 1 input.
RC4/ANC4	RC4	TTL/ST	CMOS	General purpose I/O.
	ANC4	AN	—	ADC Channel C4 input.
RC5/ANC5/MDCIN2 ⁽¹⁾ /CCP1 ⁽¹⁾	RC5	TTL/ST	CMOS	General purpose I/O.
	ANC5	AN	—	ADC Channel C5 input.
	MDCIN2	TTL/ST	—	Modular Carrier input 2.
	CCP1	TTL/ST	CMOS	Capture/Compare/PWM 1 input.
RC6/ANC6/SS1 ⁽¹⁾	RC6	TTL/ST	CMOS	General purpose I/O.
	ANC6	AN	—	ADC Channel C6 input.
	SS1	TTL/ST	—	Slave Select 1 input.
RC7/ANC7	RC7	TTL/ST	CMOS	General purpose I/O.
	ANC7	AN	—	ADC Channel C7 input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS= CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C = Schmitt Trigger input with I²C
HV = High Voltage XTAL = Crystal levels

- Note** 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers. See Register 13-2.
2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers. See Register 13-2.
3: These I²C functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18325	PIC16(L)F18345	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 31 — only accessible from Debug Executive, unless otherwise specified													
CPU CORE REGISTERS; see Table 4-2 for specifics													
F8Ch to FE3h	—	—	—	Unimplemented								—	—
FE4h ⁽²⁾	STATUS_SHAD			—	—	—	—	—	Z	DC	C	---- -xxx	---- -uuu
FE5h ⁽²⁾	WREG_SHAD			Working Register Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FE6h ⁽²⁾	BSR_SHAD			—	—	—	Bank Select Register Normal (Non-ICD) Shadow					---x xxxx	---u uuuu
FE7h ⁽²⁾	PCLATH_SHAD			—	Program Counter Latch High Register Normal (Non-ICD) Shadow							-xxx xxxx	-uuu uuuu
FE8h ⁽²⁾	FSR0L_SHAD			Indirect Data Memory Address 0 Low Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FE9h ⁽²⁾	FSR0H_SHAD			Indirect Data Memory Address 0 High Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FEAh ⁽²⁾	FSR1L_SHAD			Indirect Data Memory Address 1 Low Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FEBh ⁽²⁾	FSR1H_SHAD			Indirect Data Memory Address 1 High Pointer Normal (Non-ICD) Shadow								xxxx xxxx	uuuu uuuu
FECh	—	—		Unimplemented								—	—
FEDh ⁽²⁾	STKPTR			—	—	—	Current Stack pointer					---x xxxx	---1 1111
FEEh ⁽²⁾	TOSL			Top of Stack Low byte								xxxx xxxx	xxxx xxxx
FEFh ⁽²⁾	TOSH			—	Top of Stack High byte							-xxx xxxx	-xxx xxxx

Legend: x = unknown, u = unchanged, q = depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Only on PIC16F18325/18345.

Note 2: Register accessible from both User and ICD Debugger.

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TABLE 7-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON1	—	NOSC<2:0>			NDIV<3:0>				90
OSCCON2	—	COSC<2:0>			CDIV<3:0>				90
OSCCON3	CWSHOLD	SOSCPWR	SOSCBE	ORDY	NOSCR	—	—	—	91
OSCSTAT1	EXTOR	HFOR	—	LFOR	SOR	ADOR	—	PLLR	92
OSCEN	EXTOEN	HFOEN	—	LFOEN	SOSCEN	ADOEN	—	—	93
OSCFRQ	—	—	—	—	HFFRQ<3:0>				94
OSCTUNE	—	—	HFTUN<5:0>						95

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 7-4: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

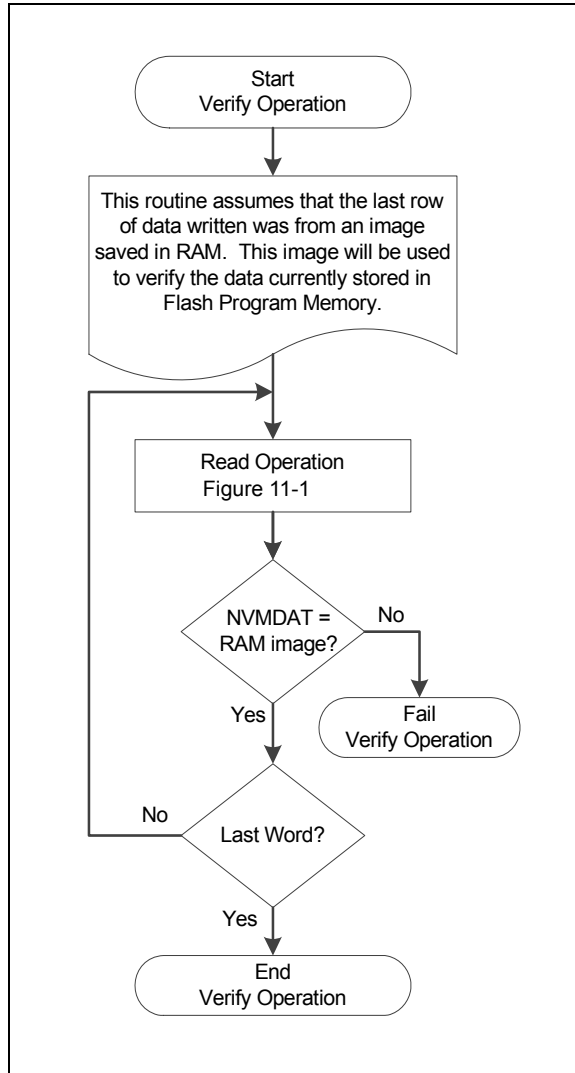
Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	—	CSWEN	—	—	CLKOUTEN	64
	7:0	—	RSTOSC2	RSTOSC1	RSTOSC0	—	FEXTOSC2	FEXTOSC1	FEXTOSC0	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

11.4.8 WRITE VERIFY

It is considered good programming practice to verify that program memory writes agree with the intended value. Since program memory is stored as a full row, then the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

FIGURE 11-7: PROGRAM FLASH MEMORY VERIFY FLOWCHART



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12.2.6 ANALOG CONTROL

The ANSELA register (Register 12-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

12.2.7 WEAK PULL-UP CONTROL

The WPUA register (Register 12-5) controls the individual weak pull-ups for each PORT pin.

PORTA pin RA3 includes the $\overline{\text{MCLR/VPP}}$ input. The $\overline{\text{MCLR}}$ input allows the device to be reset, and can be disabled by the MCLRE bit of Configuration Word 2. A weak pull-up is present on the RA3 port pin. This weak pull-up is enabled when $\overline{\text{MCLR}}$ is enabled (MCLRE = 1) or the WPUA3 bit is set. The weak pull-up is disabled when is disabled and the WPUA3 bit is clear.

12.2.8 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other output functions are selected with the peripheral pin select logic. See **Section 13.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

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REGISTER 12-3: LATA: PORTA DATA LATCH REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'
bit 5-4 **LATA<5:4>:** RA<5:4> Output Latch Value bits⁽¹⁾
bit 3 **Unimplemented:** Read as '0'
bit 2-0 **LATA<2:0>:** RA<2:0> Output Latch Value bits⁽¹⁾

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 12-4: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'
bit 5-4 **ANSA<5:4>:** Analog Select between Analog or Digital Function on pins RA<5:4>, respectively
1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.
bit 3 **Unimplemented:** Read as '0'
bit 2-0 **ANSA<2:0>:** Analog Select between Analog or Digital Function on pins RA<2:0>, respectively
1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

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REGISTER 12-7: SLRCONA: PORTA SLEW RATE CONTROL REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'
 bit 5-4 **SLRA<5:4>:** PORTA Slew Rate Enable bits
 For RA<5:4> pins, respectively
 1 = Port pin slew rate is limited
 0 = Port pin slews at maximum rate
 bit 3 **Unimplemented:** Read as '0'
 bit 2-0 **SLRA<2:0>:** PORTA Slew Rate Enable bits
 For RA<2:0> pins, respectively
 1 = Port pin slew rate is limited
 0 = Port pin slews at maximum rate

REGISTER 12-8: INLVLA: PORTA INPUT LEVEL CONTROL REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'
 bit 5-0 **INLVLA<5:0>:** PORTA Input Level Select bits
 For RA<5:0> pins, respectively
 1 = ST input used for PORT reads and interrupt-on-change
 0 = TTL input used for PORT reads and interrupt-on-change

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15.5 Register Definitions: Interrupt-on-Change Control

REGISTER 15-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **IOCAP<5:0>:** Interrupt-on-Change PORTA Positive Edge Enable bits1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCAF_x bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin

REGISTER 15-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'bit 5-0 **IOCAN<5:0>:** Interrupt-on-Change PORTA Negative Edge Enable bits1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAF_x bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin

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18.12 Register Definitions: Comparator Control

REGISTER 18-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	U-0	R/W-0/0	U-0	R/W-1/1	R/W-0/0	R/W-0/0
CxON	CxOUT	—	CxPOL	—	CxSP	CxHYS	CxSYNC
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7	CxON: Comparator Enable bit 1 = Comparator is enabled 0 = Comparator is disabled and consumes no active power
bit 6	CxOUT: Comparator Output bit <u>If CxPOL = 1 (inverted polarity):</u> 1 = CxVP < CxVN 0 = CxVP > CxVN <u>If CxPOL = 0 (non-inverted polarity):</u> 1 = CxVP > CxVN 0 = CxVP < CxVN
bit 5	Unimplemented: Read as '0'
bit 4	CxPOL: Comparator Output Polarity Select bit 1 = Comparator output is inverted 0 = Comparator output is not inverted
bit 3	Unimplemented: Read as '0'
bit 2	CxSP: Comparator Speed/Power Select bit 1 = Comparator operates in Normal-Power, High-Speed mode 0 = Reserved. (do not use)
bit 1	CxHYS: Comparator Hysteresis Enable bit 1 = Comparator hysteresis enabled 0 = Comparator hysteresis disabled
bit 0	CxSYNC: Comparator Output Synchronous Mode bit 1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source. 0 = Comparator output to Timer1 and I/O pin is asynchronous

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REGISTER 21-6: CLCxSEL3: GENERIC CLCx DATA 3 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LCxD4S<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'
 bit 5-0 **LCxD4S<5:0>**: CLCx Data 4 Input Selection bits
 See Table 21-1.

REGISTER 21-7: CLCxGLS0: GATE 0 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG1D4T	LCxG1D4N	LCxG1D3T	LCxG1D3N	LCxG1D2T	LCxG1D2N	LCxG1D1T	LCxG1D1N
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7 **LCxG1D4T**: Gate 0 Data 4 True (non-inverted) bit
 1 = CLCIN3 (true) is gated into CLCx Gate 0
 0 = CLCIN3 (true) is not gated into CLCx Gate 0
 bit 6 **LCxG1D4N**: Gate 0 Data 4 Negated (inverted) bit
 1 = CLCIN3 (inverted) is gated into CLCx Gate 0
 0 = CLCIN3 (inverted) is not gated into CLCx Gate 0
 bit 5 **LCxG1D3T**: Gate 0 Data 3 True (non-inverted) bit
 1 = CLCIN2 (true) is gated into CLCx Gate 0
 0 = CLCIN2 (true) is not gated into CLCx Gate 0
 bit 4 **LCxG1D3N**: Gate 0 Data 3 Negated (inverted) bit
 1 = CLCIN2 (inverted) is gated into CLCx Gate 0
 0 = CLCIN2 (inverted) is not gated into CLCx Gate 0
 bit 3 **LCxG1D2T**: Gate 0 Data 2 True (non-inverted) bit
 1 = CLCIN1 (true) is gated into CLCx Gate 0
 0 = CLCIN1 (true) is not gated into CLCx Gate 0
 bit 2 **LCxG1D2N**: Gate 0 Data 2 Negated (inverted) bit
 1 = CLCIN1 (inverted) is gated into CLCx Gate 0
 0 = CLCIN1 (inverted) is not gated into CLCx Gate 0
 bit 1 **LCxG1D1T**: Gate 0 Data 1 True (non-inverted) bit
 1 = CLCIN0 (true) is gated into CLCx Gate 0
 0 = CLCIN0 (true) is not gated into CLCx Gate 0
 bit 0 **LCxG1D1N**: Gate 0 Data 1 Negated (inverted) bit
 1 = CLCIN0 (inverted) is gated into CLCx Gate 0
 0 = CLCIN0 (inverted) is not gated into CLCx Gate 0

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REGISTER 22-6: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	—	—	ADRES<9:8>	
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-2 **Reserved:** Do not use.
bit 1-0 **ADRES<9:8>:** ADC Result Register bits
Upper two bits of 10-bit conversion result

REGISTER 22-7: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<7:0>							
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-0 **ADRES<7:0>:** ADC Result Register bits
Lower eight bits of 10-bit conversion result

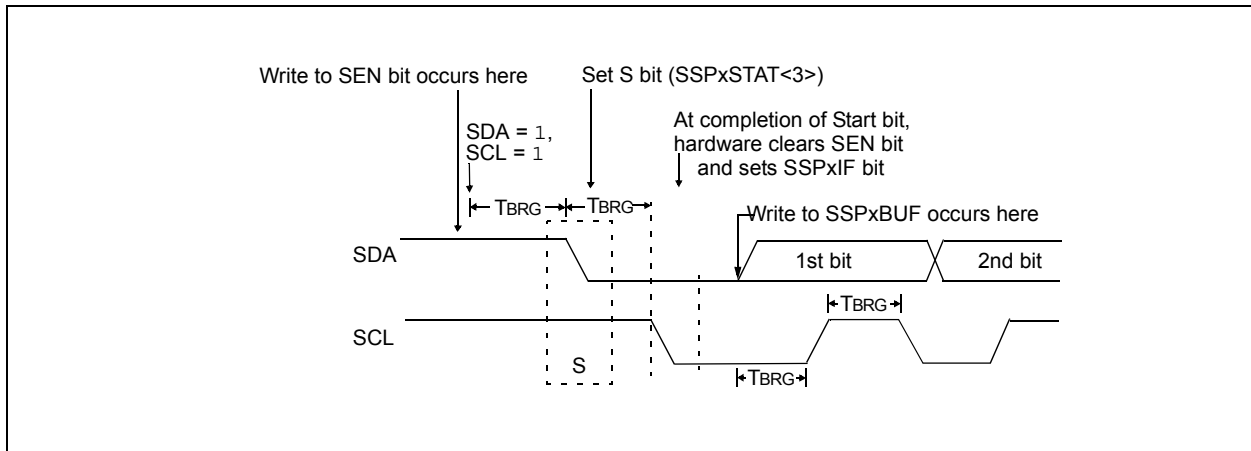
30.6.4 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition (Figure 30-26), the user sets the Start Enable bit, SEN bit of the SSPxCON2 register. If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the Start condition and causes the S bit of the SSPxSTAT register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPxCON2 register will be automatically cleared by hardware; the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note 1: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF, is set, the Start condition is aborted and the I²C module is reset into its idle state.

2: The Philips I²C specification states that a bus collision cannot occur on a Start.

FIGURE 30-26: FIRST START BIT TIMING



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REGISTER 31-4: RC1REG⁽¹⁾: RECEIVE DATA REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RC1REG<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **RC1REG<7:0>**: Lower eight bits of the received data; read-only; see also RX9D (Register 31-2)

Note 1: RC1REG (including the ninth bit) is double buffered, and data is available while new data is being received.

REGISTER 31-5: TX1REG⁽¹⁾: TRANSMIT DATA REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TX1REG<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **TX1REG<7:0>**: Lower eight bits of the received data; read-only; see also RX9D (Register 31-1)

Note 1: TX1REG (including the ninth bit) is double buffered, and can be written when previous data has started shifting.

REGISTER 31-6: SP1BRGL⁽¹⁾: BAUD RATE GENERATOR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SP1BRG<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **SP1BRG<7:0>**: Lower eight bits of the Baud Rate Generator

Note 1: Writing to SP1BRG resets the BRG counter.

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33.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- MCLR/VPP
- VDD
- VSS

In Program/Verify mode the program memory, data EEPROM, user IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the “PIC16(L)F183XX Memory Programming Specification” (DS40001738).

33.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on MCLR/VPP to VIH.

33.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Words is set to ‘1’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘0’. The LVP bit can only be reprogrammed to ‘0’ by using the High-Voltage Programming mode.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

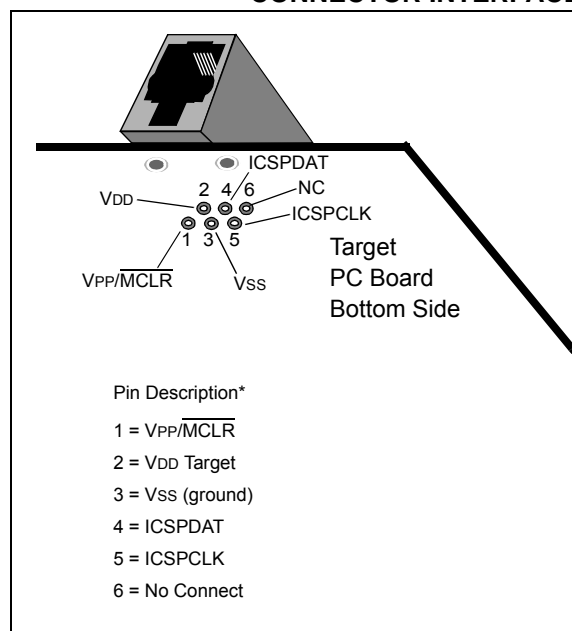
Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

If low-voltage programming is enabled (LVP = 1), the MCLR Reset function is automatically enabled and cannot be disabled. See Section 6.4 “MCLR” for more information.

33.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 33-1.

FIGURE 33-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 33-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 33-3 for more information.

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LSLF Logical Left Shift

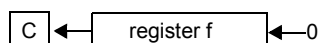
Syntax: [*label*] LSLF f {,d}

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f < 7) \rightarrow C$
 $(f < 6:0) \rightarrow \text{dest} < 7:1 >$
 $0 \rightarrow \text{dest} < 0 >$

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSB. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



LSRF Logical Right Shift

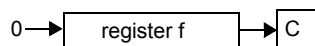
Syntax: [*label*] LSRF f {,d}

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $0 \rightarrow \text{dest} < 7 >$
 $(f < 7:1) \rightarrow \text{dest} < 6:0 >$,
 $(f < 0) \rightarrow C$,

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



MOVF Move f

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) \rightarrow (\text{dest})$

Status Affected: Z

Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example: MOVF FSR, 0

After Instruction
W = value in FSR register
Z = 1

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TABLE 35-4: I/O PORTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
D300	V _{IL}	Input Low Voltage					
		I/O PORT:					
		with TTL buffer	—	—	0.8	V	4.5V ≤ V _{DD} ≤ 5.5V
			—	—	0.15 V _{DD}	V	1.8V ≤ V _{DD} ≤ 4.5V
		with Schmitt Trigger buffer	—	—	0.2 V _{DD}	V	2.0V ≤ V _{DD} ≤ 5.5V
		with I ² C levels	—	—	0.3 V _{DD}	V	
D304		with SMBus levels	—	—	0.8	V	2.7V ≤ V _{DD} ≤ 5.5V
D305		MCLR	—	—	0.2 V _{DD}	V	
D320	V _{IH}	Input High Voltage					
		I/O PORT:					
		with TTL buffer	2.0	—	—	V	4.5V ≤ V _{DD} ≤ 5.5V
			0.25 V _{DD} + 0.8	—	—	V	1.8V ≤ V _{DD} ≤ 4.5V
		with Schmitt Trigger buffer	0.8 V _{DD}	—	—	V	2.0V ≤ V _{DD} ≤ 5.5V
		with I ² C levels	0.7 V _{DD}	—	—		
D324		with SMBus levels	2.1	—	—	V	2.7V ≤ V _{DD} ≤ 5.5V
D325		MCLR	0.7 V _{DD}	—	—	V	
D340	I _{IL}	Input Leakage Current⁽²⁾					
		I/O Ports	—	± 5	± 125	nA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, 85°C
			—	± 5	± 1000	nA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, 125°C
D342		MCLR ⁽²⁾	—	± 50	± 200	nA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, 85°C
D350	I _{PUR}	Weak Pull-up Current					
			25	120	200	μA	V _{DD} = 3.0V, V _{PIN} = V _{SS}
D360	V _{OL}	Output Low Voltage⁽⁴⁾					
		I/O ports	—	—	0.6	V	I _{OL} = 10.0 mA, V _{DD} = 3.0V
D370	V _{OH}	Output High Voltage⁽⁴⁾					
		I/O ports	V _{DD} - 0.7	—	—	V	I _{OH} = 6.0 mA, V _{DD} = 3.0V
D380	C _{IO}	All I/O pins	—	5	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

Note 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

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FIGURE 35-13: CAPTURE/COMPARE/PWM TIMINGS (CCP)

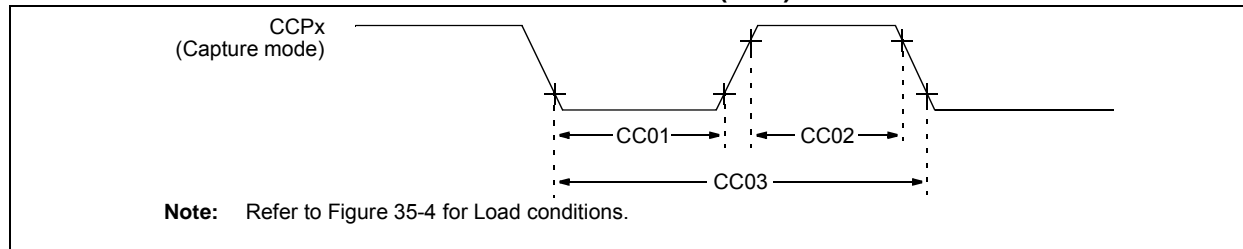


TABLE 35-18: CAPTURE/COMPARE/PWM CHARACTERISTICS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param. No.	Sym.	Characteristic		Min.	Typ.†	Max.	Units	Conditions
CC01*	TccL	CCPx Input Low Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCPx Input High Time	No Prescaler	$0.5T_{CY} + 20$	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCPx Input Period		$\frac{3T_{CY} + 40}{N}$	—	—	ns	N = prescale value

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (06/2015)

Initial release of the document.

Revision B (07/2015)

Updated the eXtreme Low-Power (XLP) Features section on page 1; Updated the Data Sheet Index in the Family Types table; Updated Sections 2.3, 3.2, 3.2.1 through 3.2.3, 3.5, 4.3.2, 5.2, 5.2.2, 5.2.3, 5.10, 6.1, 6.2.2, 6.2.2.3, 6.3, 6.4.4; 34.0 (Electrical Specifications); Removed note in Section 6.3.2; Updated Tables 1-2, 3-3, 5-1, 6-4, 19-1, 34-4, 34-7, Registers 4-1, 4-3, 4-4, 6-3, 6-4, and Figures 3-2, 34-5, 34-7; Removed Figure 3-8 (Indirect Addressing); Updated note 2 in Register 6-1 and Table 34-5; Updated notes in Register 6-2; Removed note 1 in Register 6-5 and note 2 in Register 6-2; Split table 6-1 in Tables 6-1 and 6-2; Changed data sheet status from Advance Information to Preliminary; Other minor corrections.

Revision C (10/2016)

Updated Family Types and Pin Allocation Tables in the Description chapter; Table 1-1, 1-2 and 1-3; updated Figure 3-1; Added Section 2.0 "Guidelines for Getting Started With PIC16(L)F183XX Microcontrollers"; Added Section 4.1.1.3. NVMREG Access and Section 4.5.4. Data EEPROM Memory; Updated Register 7-6; Updated Figure 8-2, and Registers 8-1, 8-2, 8-7, 8-8, and 8-10; Added Section 10.2.4 WDT Is Always Off; Removed Section 14.3 Disabling a Module; Updated Figure 15-1; Updated Figure 21-2; Updated Figure 22-1; Updated Figure 29-1.