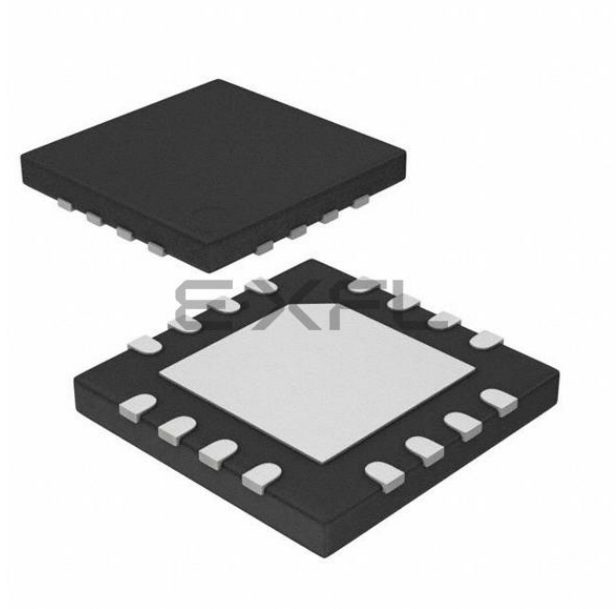


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UQFN Exposed Pad
Supplier Device Package	16-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18325-i-jq

TABLE 2: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)

I/O(2)	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR	Interrupt	Pull-up	Basic
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	—	IOC	Y	ICDDAT ICSPDAT
RA1	18	15	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	$\overline{SS2}$	—	—	—	IOC	Y	ICDCLK ICSPCLK
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CKI(1)	CCP3(1)	—	CWG1IN(1) CWG2IN(1)	—	—	CLCIN0(1)	—	IOC INT(1)	Y	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	$\overline{MCLR}$ VPP
RA4	3	20	ANA4	—	—	—	—	—	T1G(1) T3G(1) T5G(1) SOSCO	CCP4(1)	—	—	—	—	—	—	IOC	Y	CLKOUT OSC2
RA5	2	19	ANA5	—	—	—	—	—	T1CKI(1) T3CKI(1) T5CKI(1) SOSCIN SOSCI	—	—	—	—	—	—	—	IOC	Y	CLKIN OSC1
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	—	IOC	Y	—
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SDI2(1) SDA2(1,3,4)	RX(1)	CLCIN3(1)	—	IOC	Y	—
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	—	IOC	Y	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2(1) SCL2(1,3,4)	—	—	—	IOC	Y	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	IOC	Y	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: These pins are configured for I^2C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18325	PIC16(L)F18345	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 13													
CPU CORE REGISTERS; see Table 4-2 for specifics													
68Ch	—	—		Unimplemented								—	—
68Dh	—	—		Unimplemented								—	—
68Eh	—	—		Unimplemented								—	—
68Fh	—	—		Unimplemented								—	—
690h	—	—		Unimplemented								—	—
691h	CWG1CLKCON			—	—	—	—	—	—	—	CS	---- ---0	---- ---0
692h	CWG1DAT			—	—	—	—	DAT<3:0>				---- 0000	---- 0000
693h	CWG1DBR			—	—	DBR<5:0>						--00 0000	--00 0000
694h	CWG1DBF			—	—	DBF<5:0>						--00 0000	--00 0000
695h	CWG1CON0			EN	LD	—	—	—	MODE<2:0>			00-- -000	00-- -000
696h	CWG1CON1			—	—	IN	—	POLD	POLC	POLB	POLA	--x- 0000	--x- 0000
697h	CWG1AS0			SHUTDOWN	REN	LSBD<1:0>		LSAC<1:0>		—	—	0001 01--	0001 01--
698h	CWG1AS1			—	—	—	AS4E	AS3E	AS2E	AS1E	AS0E	---0 0000	---0 0000
699h	CWG1STR			OVRD	OVRC	OVRB	OVRA	STRD	STRC	STRB	STRA	0000 0000	0000 0000
69Ah to 69Fh	—	—		Unimplemented								—	—

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Only on PIC16F18325/18345.

2: Register accessible from both User and ICD Debugger.

TABLE 4-4: SPECIAL FUNCTION REGISTER SUMMARY BANKS 0-31 (CONTINUED)

Address	Name	PIC16(L)F18325	PIC16(L)F18345	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
Bank 30													
CPU CORE REGISTERS; see Table 4-2 for specifics													
F20h	CLC2GLS0			LC2G1D4T	LC2G1D4N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	xxxx xxxx	uuuu uuuu
F21h	CLC2GLS1			LC2G2D4T	LC2G2D4N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	xxxx xxxx	uuuu uuuu
F22h	CLC2GLS2			LC2G3D4T	LC2G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	xxxx xxxx	uuuu uuuu
F23h	CLC2GLS3			LC2G4D4T	LC2G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	xxxx xxxx	uuuu uuuu
F24h	CLC3CON			LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			0-00 0000	0-00 0000
F25h	CLC3POL			LC3POL	—	—	—	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	0--- xxxx	0--- uuuu
F26h	CLC3SEL0			—	—	LC3D1S<5:0>						--xx xxxx	--uu uuuu
F27h	CLC3SEL1			—	—	LC3D2S<5:0>						--xx xxxx	--uu uuuu
F28h	CLC3SEL2			—	—	LC3D3S<5:0>						--xx xxxx	--uu uuuu
F29h	CLC3SEL3			—	—	LC3D4S<5:0>						--xx xxxx	--uu uuuu
F2Ah	CLC3GLS0			LC3G1D4T	LC3G1D4N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	xxxx xxxx	uuuu uuuu
F2Bh	CLC3GLS1			LC3G2D4T	LC3G2D4N	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	xxxx xxxx	uuuu uuuu
F2Ch	CLC3GLS2			LC3G3D4T	LC3G3D4N	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	xxxx xxxx	uuuu uuuu
F2Dh	CLC3GLS3			LC3G4D4T	LC3G4D4N	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	xxxx xxxx	uuuu uuuu
F2Eh	CLC4CON			LC4EN	—	LC4OUT	LC4INTP	LC4INTN	LC4MODE<2:0>			0-00 0000	0-00 0000
F2Fh	CLC4POL			LC4POL	—	—	—	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	0--- xxxx	0--- uuuu
F30h	CLC4SEL0			—	—	LC4D1S<5:0>						--xx xxxx	--uu uuuu
F31h	CLC4SEL1			—	—	LC4D2S<5:0>						--xx xxxx	--uu uuuu
F32h	CLC4SEL2			—	—	LC4D3S<5:0>						--xx xxxx	--uu uuuu
F33h	CLC4SEL3			—	—	LC4D4S<5:0>						--xx xxxx	--uu uuuu
F34h	CLC4GLS0			LC4G1D4T	LC4G1D4N	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	xxxx xxxx	uuuu uuuu
F35h	CLC4GLS1			LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	xxxx xxxx	uuuu uuuu
F36h	CLC4GLS2			LC4G3D4T	LC4G3D4N	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	xxxx xxxx	uuuu uuuu
F37h	CLC4GLS3			LC4G4D4T	LC4G4D4N	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, q =depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations unimplemented, read as '0'.

Note 1: Only on PIC16F18325/18345.

2: Register accessible from both User and ICD Debugger.

REGISTER 8-8: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W/HS-0/0	R/W/HS-0/0	R-0	R/HS/HC-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	BCL1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware set

bit 7 **TMR1GIF**: Timer1 Gate Interrupt Flag bit
1 = The Timer1 gate has gone inactive (the gate is closed).
0 = The Timer1 gate has not gone inactive.

bit 6 **ADIF:** Analog-to-Digital Converter (ADC) Interrupt Flag bit
1 = The A/D conversion completed
0 = The A/D conversion is not completed

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit (read-only)
1 = The EUSART1 receive buffer is not empty
0 = The EUSART1 receive buffer is empty

bit 4 **TXIF**: EUSART Transmit Interrupt Flag bit (read-only)
1 = The EUSART1 receive buffer is empty
0 = The EUSART1 receive buffer is not empty

bit 3 **SSP1IF**: Synchronous Serial Port (MSSP) Interrupt Flag bit
1 = The Transmission/Reception/Bus Condition is complete (must be cleared in software)
0 = Waiting for the Transmission/Reception/Bus Condition in progress

bit 2 **BCL1IF:** MSSP Bus Collision Interrupt Flag bit
1 = A bus collision was detected (must be cleared in software)
0 = No bus collision was detected

bit 1 **TMR2IF:** Timer2 to PR2 Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = TMR1 overflow occurred (must be cleared in software)
0 = No TMR1 overflow occurred

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

13.0 PERIPHERAL PIN SELECT (PPS) MODULE

The Peripheral Pin Select (PPS) module connects peripheral inputs and outputs to the device I/O pins. Only digital signals are included in the selections. All analog inputs and outputs remain fixed to their assigned pins. Input and output selections are independent as shown in the simplified block diagram Figure 13-1.

13.1 PPS Inputs

Each peripheral has a PPS register with which the inputs to the peripheral are selected. Inputs include the device pins.

Although every peripheral has its own PPS input selection register, the selections are identical for every peripheral as shown in Register 13-1.

Note:	The notation “xxx” in the register name is a place holder for the peripheral identifier. For example, CLC1PPS.

13.2 PPS Outputs

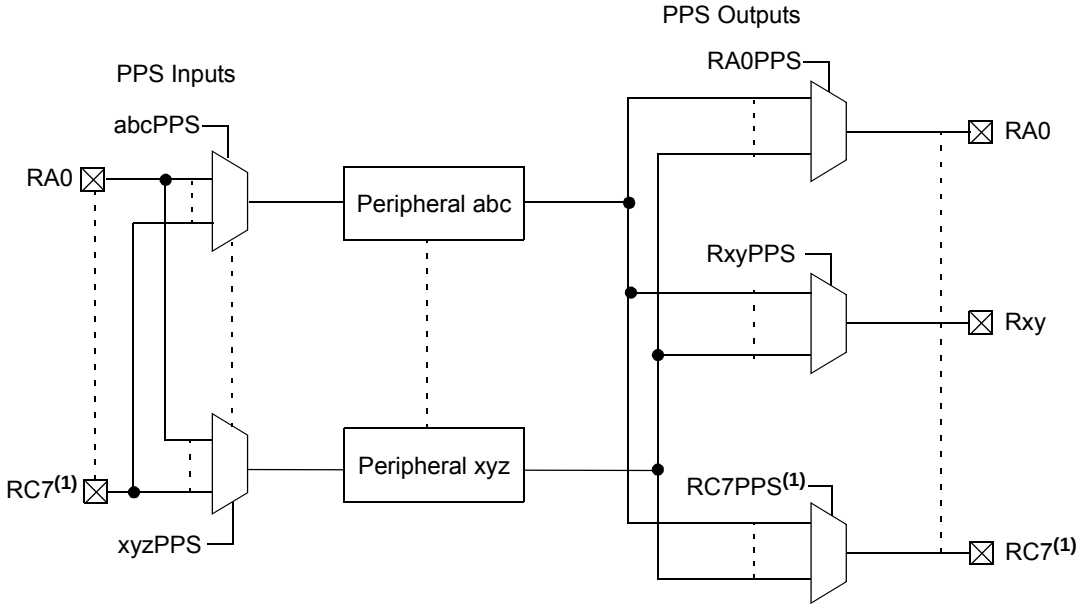
Each I/O pin has a PPS register with which the pin output source is selected. With few exceptions, the port TRIS control associated with that pin retains control over the pin output driver. Peripherals that control the pin output driver as part of the peripheral operation will override the TRIS control as needed. These peripherals are:

- EUSART1 (synchronous operation)
- MSSP (I^2C)

Although every pin has its own PPS peripheral selection register, the selections are identical for every pin as shown in Register 13-2.

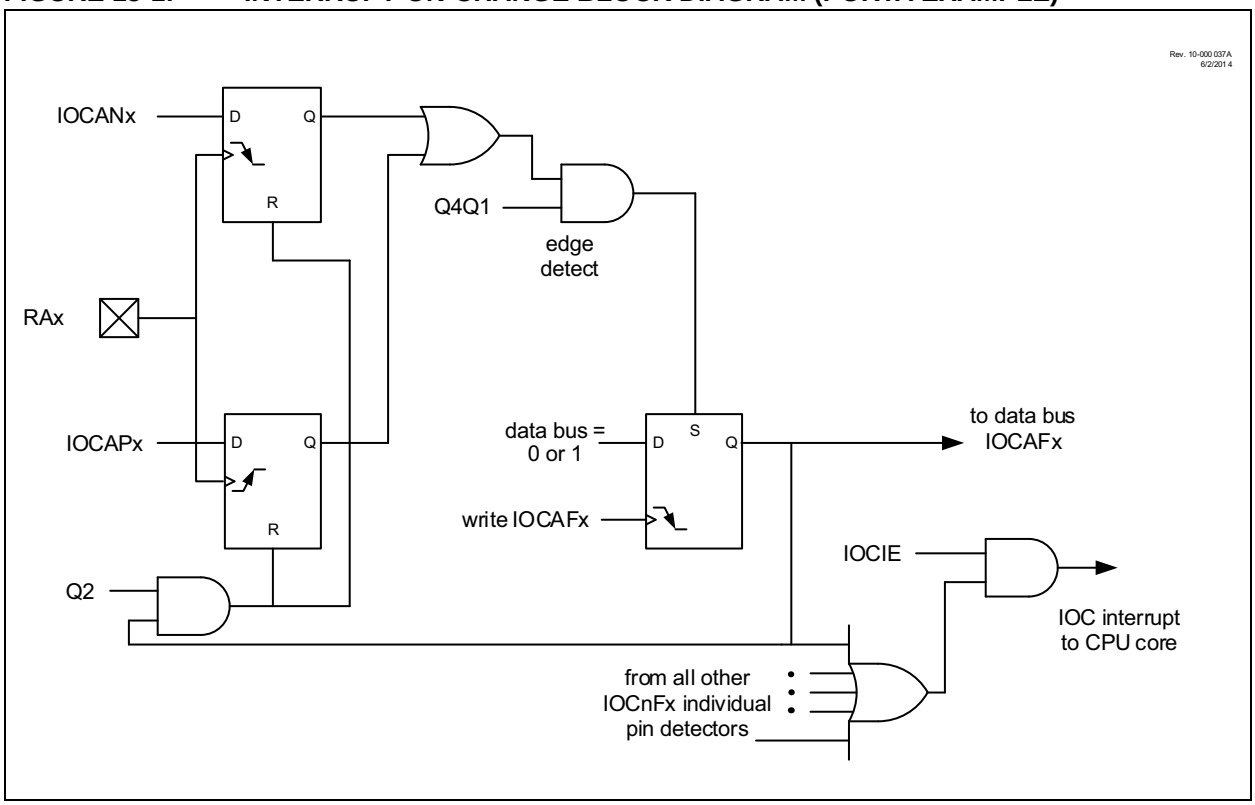
Note:	The notation “Rxy” is a place holder for the pin identifier. For example, RA0PPS.

FIGURE 13-1: SIMPLIFIED PPS BLOCK DIAGRAM



Note 1: RB<7:4> and RC<7:6> are available on PIC16(L)F18345 only.

FIGURE 15-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)



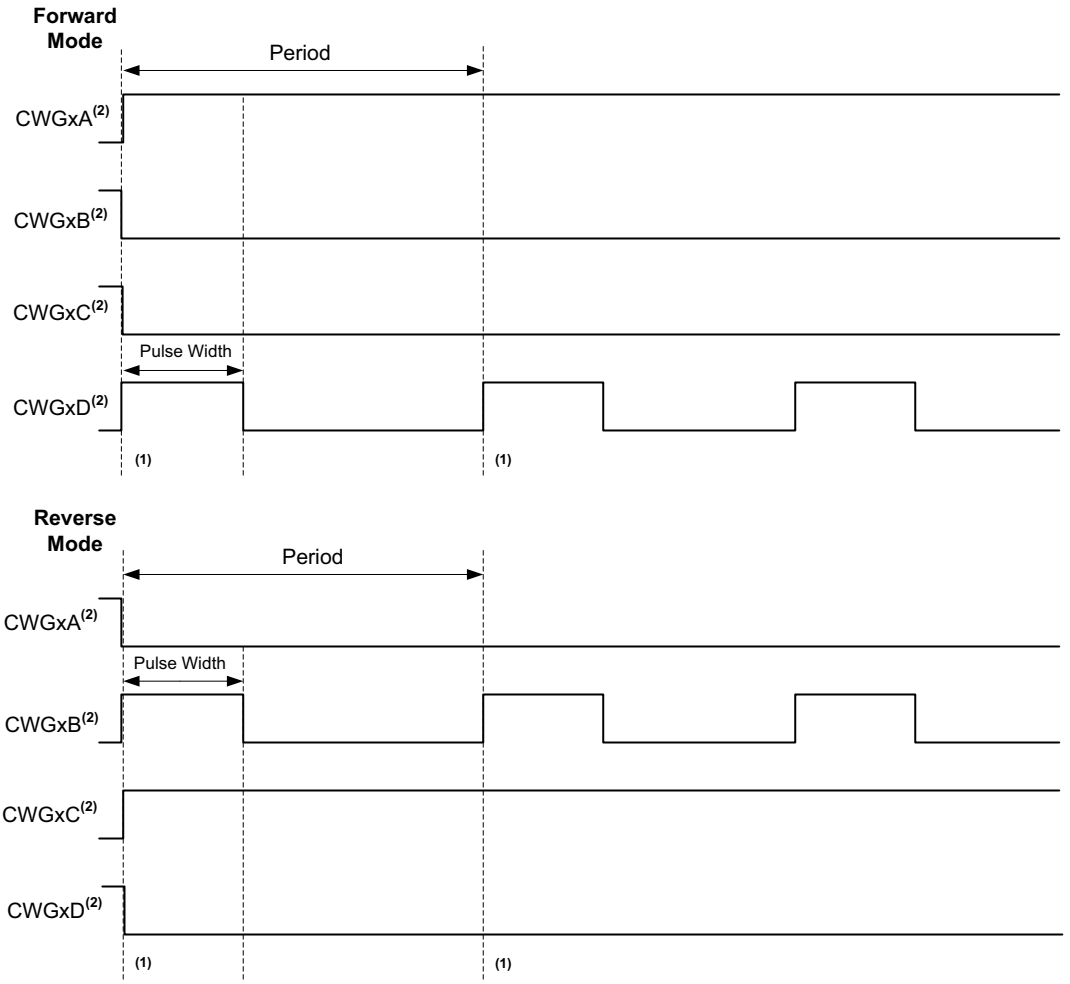
20.2.4.1 Full-Bridge Forward Mode

In Full-Bridge Forward mode (MODE<2:0> = 010), CWGxA is driven to its active state and CWGxD is modulated while CWGxB and CWGxC are driven to their inactive state, as illustrated at the top of Figure 20-6.

20.2.4.2 Full-Bridge Reverse Mode

In Full-Bridge Reverse mode (MODE<2:0> = 011), CWGxC is driven to its active state and CWGxB is modulated while CWGxA and CWGxD are driven to their inactive state, as illustrated at the bottom of Figure 20-6.

FIGURE 20-6: EXAMPLE OF FULL-BRIDGE OUTPUT



Note 1: A rising CWG data input creates a rising event on the modulated output.

2: Output signals shown as active-high; all POLy bits are clear.

20.2.4.3 Direction Change in Full-Bridge Mode

In Full-Bridge mode, changing MODE<2:0> controls the forward/reverse direction. Changes to MODE<2:0> change to the new direction on the next rising edge of the modulated input.

A direction change is initiated in software by changing the MODE<2:0> bits of the WGxCON0 register. The sequence is illustrated in Figure 20-7.

- The associated active output CWGxA and the inactive output CWGxC are switched to drive in the opposite direction.
- The previously modulated output CWGxD is switched to the inactive state, and the previously inactive output CWGxB begins to modulate.
- CWG modulation resumes after the direction-switch dead band has elapsed.

TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH NCO1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
TRISA	—	—	TRISA5	TRISA4	—(2)	TRISA2	TRISA1	TRISA0	143
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	144
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	149
ANSELB(1)	ANSB7	ANSB6	ANSB5	ANSB4	—	—	—	—	150
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	156
ANSELC	ANSC7(1)	ANSC6(1)	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	157
PIR2	TMR6IF	C2IF	C1IF	NVMIF	SSP2IF	BCL2IF	TMR4IF	NCO1IF	109
PIE2	TMR6IE	C2IE	C1IE	NVMIE	SSP2IE	BCL2IE	TMR4IE	NCO1IE	104
INTCON	GIE	PEIE	—	—	—	—	—	INTEDG	101
NCO1CON	N1EN	—	N1OUT	N1POL	—	—	—	N1PFM	256
NCO1CLK	N1PWS<2:0>			—	—	—	N1CKS<1:0>		257
NCO1ACCL	NCO1ACC <7:0>								257
NCO1ACCH	NCO1ACC <15:8>								258
NCO1ACCU	—	—	—	—	NCO1ACC <19:16>				258
NCO1INCL	NCO1INC<7:0>								258
NCO1INCH	NCO1INC<15:8>								259
NCO1INCU	—	—	—	—	NCO1INC<19:16>				259
CWG1DAT	—	—	—	—	DAT<3:0>				215
MDSRC	—	—	—	—	MDMS<3:0>				272
MDCARH	—	MDCHPOL	MDCHSYNC	—	MDCH<3:0>				273
MDCARL	—	MDCLPOL	MDCLSYNC	—	MDCL<3:0>				274
CCPxCAP	—	—	—	—	CCPxCTS<3:0>				309

Legend: – = unimplemented read as '0'. Shaded cells are not used for NCO1 module.

Note 1: PIC16(L)F18345 only.

2: Unimplemented, read as '1'.

28.0 TIMER2/4/6 MODULE

Timer2/4/6 modules are 8-bit timers that incorporate the following features:

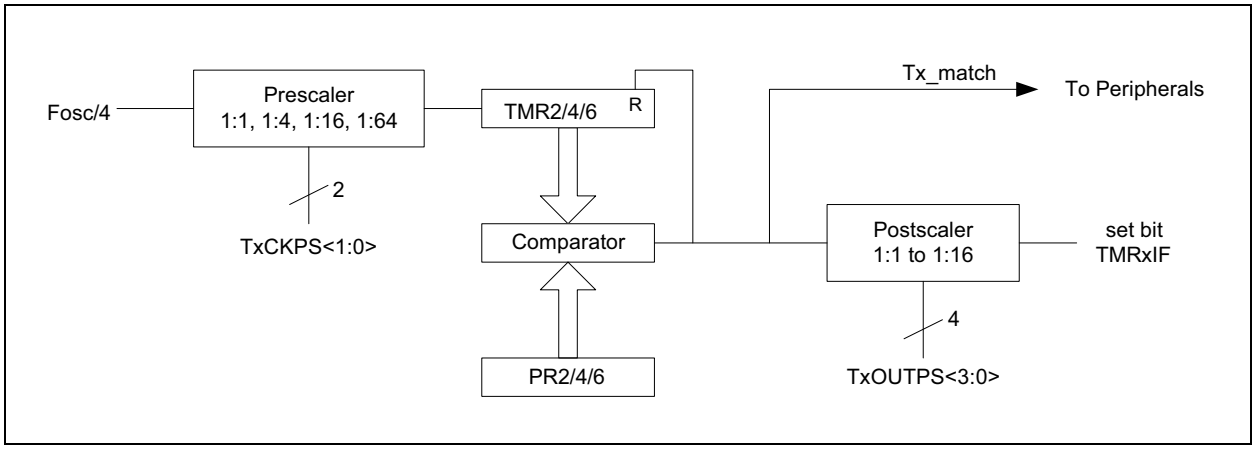
- 8-bit Timer and Period registers (TMR2/4/6 and PR2/4/6, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16, and 1:64)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2/4/6 match with PR2/4/6
- Optional use as the shift clock for the MSSPx module

See Figure 28-1 for a block diagram of Timer2/4/6.

Note 1: In devices with more than one Timer module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the T2CON and T4CON control the same operational aspects of two completely different Timer modules.

2: Throughout this section, generic references to Timer2 module in any of its operating modes may be interpreted as being equally applicable to Timerx module. Register names, module signals, I/O pins and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

FIGURE 28-1: TIMER2/4/6 BLOCK DIAGRAM



29.0 CAPTURE/COMPARE/PWM MODULES

The Capture/Compare/PWM module is a peripheral that allows the user to time and control different events and to generate Pulse-Width Modulation (PWM) signals. In Capture mode, the peripheral allows the timing of the duration of an event. The Compare mode allows the user to trigger an external event when a predetermined amount of time has expired. The PWM mode can generate Pulse-Width Modulated signals of varying frequency and duty cycle.

This family of devices contains four standard Capture/Compare/PWM modules (CCP1, CCP2, CCP3 and CCP4).

The Capture and Compare functions are identical for all CCP modules.

29.1 CCP/PWM Clock Selection

The PIC16(L)F18325/18345 devices allow each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2, Timer4, and Timer6), PWM mode on the CCP and PWM modules can use any of these timers.

The CCPTMRS register is used to select which timer is used.

Note 1:	In devices with more than one CCP module, it is very important to pay close attention to the register names used. A number placed after the module acronym is used to distinguish between separate modules. For example, the CCP1CON and CCP2CON control the same operational aspects of two completely different CCP modules.
2:	Throughout this section, generic references to a CCP module in any of its operating modes may be interpreted as being equally applicable to CCPx module. Register names, module signals, I/O pins, and bit names may use the generic designator 'x' to indicate the use of a numeral to distinguish a particular module, when required.

29.2 Capture Mode

Capture mode makes use of either the 16-bit Timer0 or Timer1 resource. When an event occurs on the capture source, the 16-bit CCPRxH:CCPRxL register pair captures and stores the 16-bit value of the TMR0H:TMR0L or TMR1H:TMR1L register pair, respectively. An event is defined as one of the following and is configured by the CCPxMODE<3:0> bits of the CCPxCON register:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

When a capture is made, the Interrupt Request Flag bit CCPxIF of the PIR4 register is set. The interrupt flag must be cleared in software. If another capture occurs before the value in the CCPRxH, CCPRxL register pair is read, the old captured value is overwritten by the new captured value.

Figure 29-1 shows a simplified diagram of the capture operation.

29.2.1 CAPTURE SOURCES

In Capture mode, the CCPx pin should be configured as an input by setting the associated TRIS control bit.

Note:	If the CCPx pin is configured as an output, a write to the port can cause a Capture condition.

The capture source is selected by configuring the CCPxCTS<3:0> bits of the CCPxCAP register. The following sources can be selected:

- CCPxPPS input
- C1_output
- C2_output
- NCO_output
- IOC_interrupt
- LC1_output
- LC2_output
- LC3_output
- LC4_output

30.5.8 GENERAL CALL ADDRESS SUPPORT

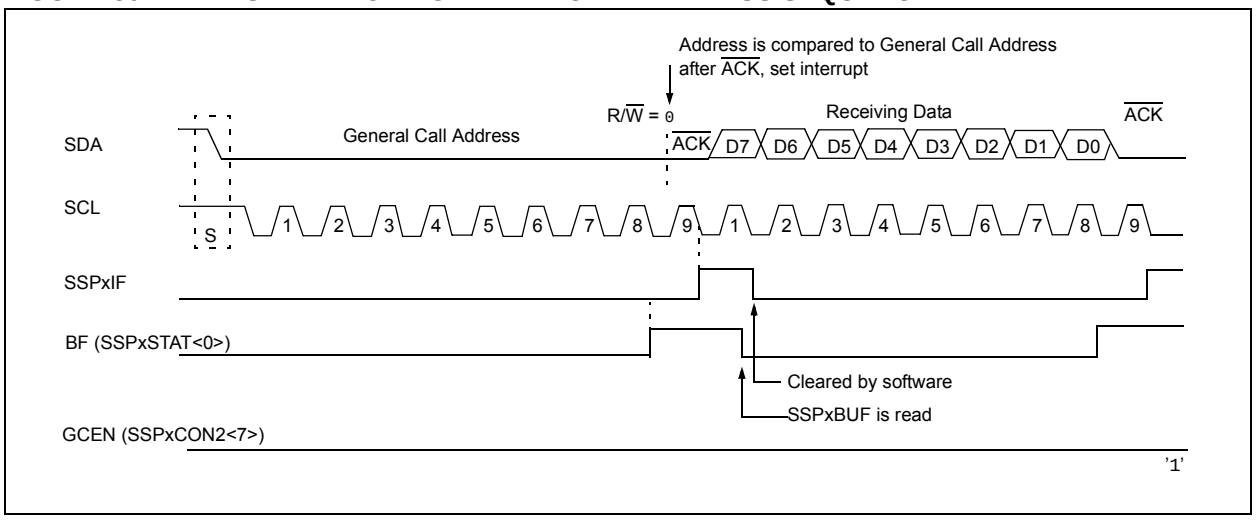
The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically $\overline{ACK}$ the reception of this address regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros with the R/$\overline{W}$ bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 30-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the eighth falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 30-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE



30.5.9 SSP MASK REGISTER

An SSP Mask (SSPMSK) register (Register 30-5) is available in I^2C Slave mode as a mask for the value held in the SSPxSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

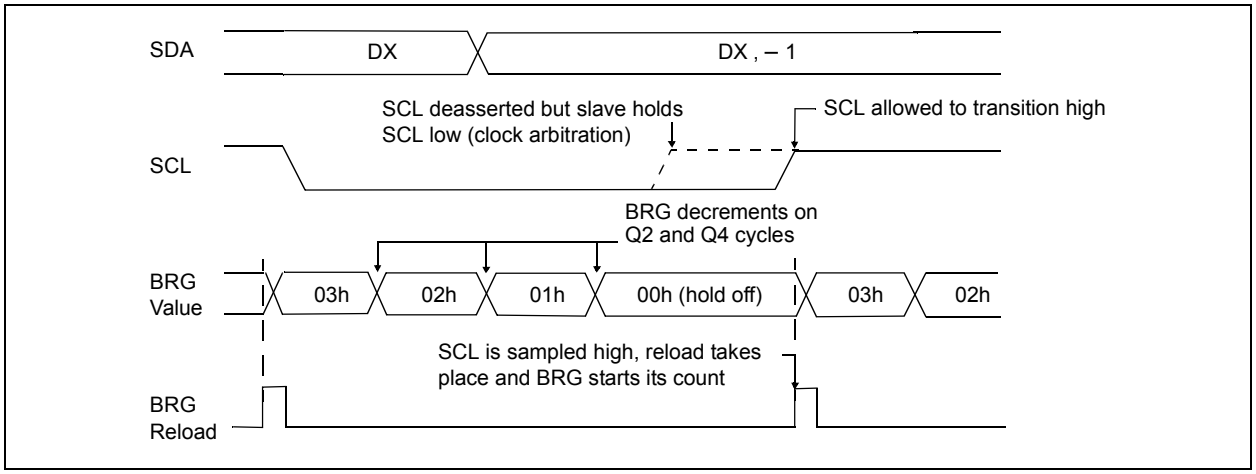
The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

30.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 30-25).

FIGURE 30-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



30.6.3 WCOL STATUS FLAG

If the user writes the SSPxBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPxBUF was attempted while the module was not idle.

Note:	Because queuing of events is not allowed, writing to the lower five bits of SSPxCON2 is disabled until the Start condition is complete.

30.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 30-33).

b) SCL is sampled low before SDA is asserted low (Figure 30-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the Start condition is aborted,
- the BCL1IF flag is set and
- the MSSPx module is reset to its Idle state (Figure 30-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 30-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note:	The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

FIGURE 30-33: BUS COLLISION DURING START CONDITION (SDA ONLY)

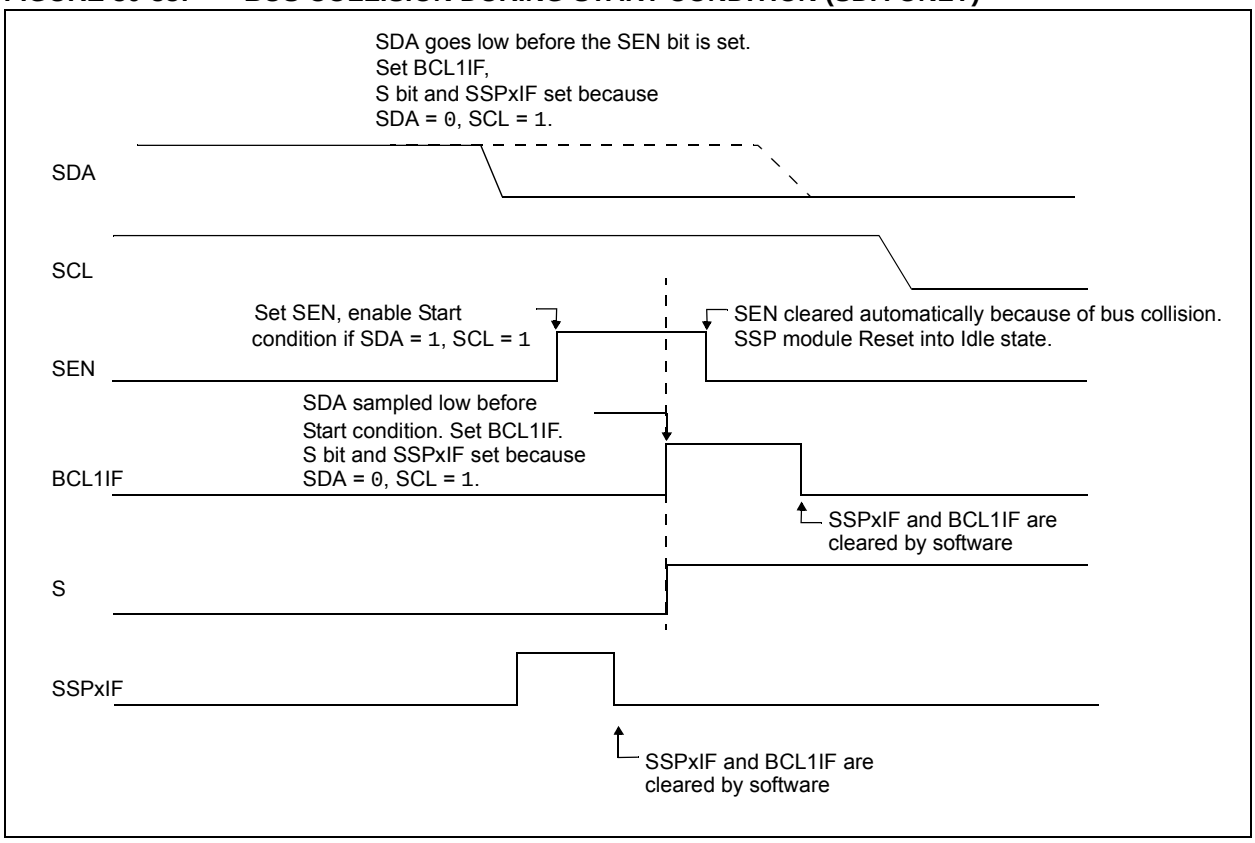


TABLE 30-2: MSSP CLOCK RATE W/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in Table 35-4 to ensure the system is designed to support IOL requirements.

REGISTER 30-3: SSPxCON2: SSPx CONTROL REGISTER 2 (I^2C MODE ONLY)(1)

R/W-0/0	R/HS/HC-0	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0	R/S/HC-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

bit 7 **GCEN:** General Call Enable bit (in I^2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 **ACKDT:** Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3 **RCEN:** Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2 **PEN:** Stop Condition Enable bit (in I^2C Master mode only)
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit (in I^2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the idle state, these bits may not be set (no spooling) and the SSPBUF may not be written.

31.1 EUSART1 Asynchronous Mode

The EUSART1 transmits and receives data using the standard non-return-to-zero (NRZ) format. NRZ is implemented with two levels: a VOH Mark state which represents a '1' data bit, and a VOL Space state which represents a '0' data bit. NRZ refers to the fact that consecutively transmitted data bits of the same value stay at the output level of that bit without returning to a neutral level between each bit transmission. An NRZ transmission port idles in the Mark state. Each character transmission consists of one Start bit followed by eight or nine data bits and is always terminated by one or more Stop bits. The Start bit is always a space and the Stop bits are always marks. The most common data format is eight bits. Each transmitted bit persists for a period of 1/(Baud Rate). An on-chip dedicated 8-bit/16-bit Baud Rate Generator is used to derive standard baud rate frequencies from the system oscillator. See Table 31-3 for examples of baud rate configurations.

The EUSART1 transmits and receives the LSb first. The EUSART1's transmitter and receiver are functionally independent, but share the same data format and baud rate. Parity is not supported by the hardware, but can be implemented in software and stored as the ninth data bit.

31.1.1 EUSART1 ASYNCHRONOUS TRANSMITTER

The EUSART1 transmitter block diagram is shown in Figure 31-1. The heart of the transmitter is the serial Transmit Shift Register (TSR), which is not directly accessible by software. The TSR obtains its data from the transmit buffer, which is the TX1REG register.

31.1.1.1 Enabling the Transmitter

The EUSART1 transmitter is enabled for asynchronous operations by configuring the following three control bits:

- TXEN = 1
- SYNC = 0
- SPEN = 1

All other EUSART1 control bits are assumed to be in their default state.

Setting the TXEN bit of the TX1STA register enables the transmitter circuitry of the EUSART1. Clearing the SYNC bit of the TX1STA register configures the EUSART1 for asynchronous operation. Setting the SPEN bit of the RC1STA register enables the EUSART1 and automatically configures the TX/CK I/O pin as an output. If the TX/CK pin is shared with an analog peripheral, the analog I/O function must be disabled by clearing the corresponding ANSEL bit.

Note:	The TXIF Transmitter Interrupt flag is set when the TXEN enable bit is set.

31.1.1.2 Transmitting Data

A transmission is initiated by writing a character to the TX1REG register. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TX1REG is immediately transferred to the TSR register. If the TSR still contains all or part of a previous character, the new character data is held in the TX1REG until the Stop bit of the previous character has been transmitted. The pending character in the TX1REG is then transferred to the TSR in one TCY immediately following the Stop bit transmission. The transmission of the Start bit, data bits and Stop bit sequence commences immediately following the transfer of the data to the TSR from the TX1REG.

31.1.1.3 Transmit Data Polarity

The polarity of the transmit data can be controlled with the SCKP bit of the BAUD1CON register. The default state of this bit is '0' which selects high true transmit idle and data bits. Setting the SCKP bit to '1' will invert the transmit data resulting in low true idle and data bits. The SCKP bit controls transmit data polarity in Asynchronous mode only. In Synchronous mode, the SCKP bit has a different function. See **Section 31.4.1.2 "Clock Polarity"**.

31.1.1.4 Transmit Interrupt Flag

The TXIF interrupt flag bit of the PIR1 register is set whenever the EUSART1 transmitter is enabled and no character is being held for transmission in the TX1REG. In other words, the TXIF bit is only clear when the TSR is busy with a character and a new character has been queued for transmission in the TX1REG. The TXIF flag bit is not cleared immediately upon writing TX1REG. TXIF becomes valid in the second instruction cycle following the write execution. Polling TXIF immediately following the TX1REG write will return invalid results. The TXIF bit is read-only, it cannot be set or cleared by software.

The TXIF interrupt can be enabled by setting the TXIE interrupt enable bit of the PIE1 register. However, the TXIF flag bit will be set whenever the TX1REG is empty, regardless of the state of TXIE enable bit.

To use interrupts when transmitting data, set the TXIE bit only when there is more data to send. Clear the TXIE interrupt enable bit upon writing the last character of the transmission to the TX1REG.

TABLE 35-9: PLL CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
PLL01	FPLLIN	PLL Input Frequency Range	4	—	8	MHz	
PLL02	FPLLOUT	PLL Output Frequency Range	16	—	32	MHz	
PLL03	TPLLST	PLL Lock Time from Start-up	—	200	—	μs	
PLL04	FPLLJIT	PLL Output Frequency Stability (Jitter)	-0.25	—	0.25	%	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 35-7: CLKOUT AND I/O TIMING

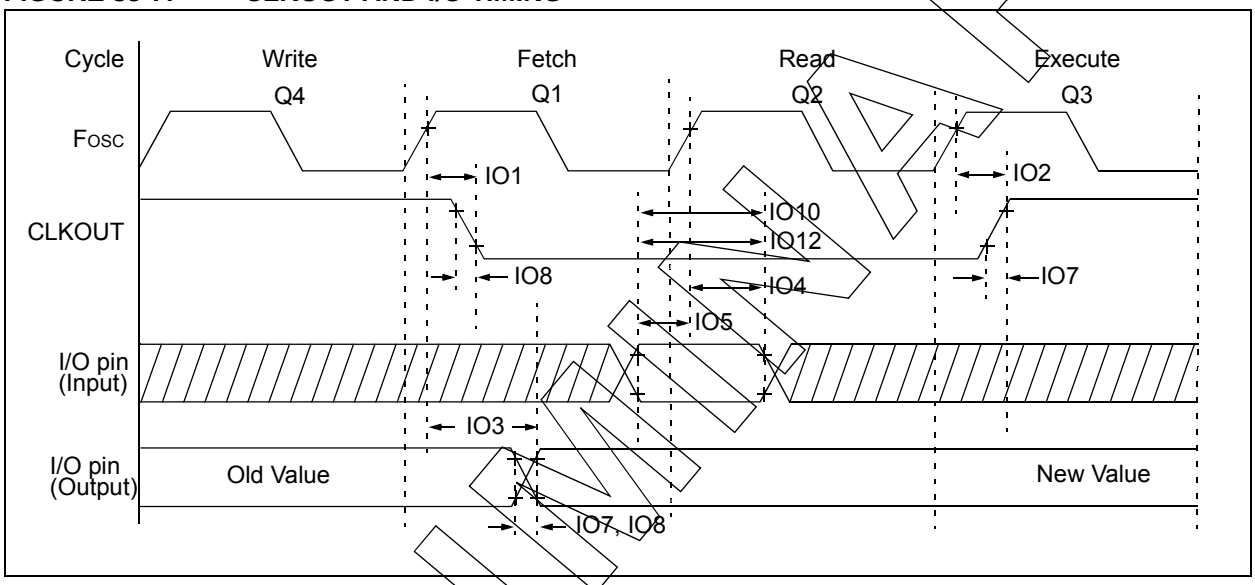


TABLE 35-14: COMPARATOR SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C See **Section 36.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM01	V_{IOFF}	Input Offset Voltage	—	—	±40	mV	V_{ICM} = V_{DD}/2
CM02	V_{ICM}	Input Common Mode Voltage	GND	—	V_{DD}	V	
CM03	CMRR	Common Mode Input Rejection Ratio	—	50	—	dB	
CM04	C_{HYST}	Comparator Hysteresis	15	25	35	mV	
CM05	T_{RESP}(1)	Response Time, Rising Edge	—	300	600	ns	
		Response Time, Falling Edge	—	220	500	ns	
CM06*	T_{MCV2VO}(2)	Mode Change to Valid Output	—	—	10	us	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at V_{DD}/2, while the other input transitions from V_{SS} to V_{DD}.

2: A mode change includes changing any of the control register values, including module enable.

TABLE 35-15: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated) V_{DD} = 3.0V, T_A = 25°C							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.†**	**Max.**	**Units**	**Comments**
DSB01	V_{LSB}	Step Size	—	V_{DD}/32	—	V	
DSB01	V_{ACC}	Absolute Accuracy	—	—	± 0.5	LSb	
DSB03*	R_{UNIT}	Unit Resistor Value	—	6000	—	Ω	
DSB04*	T_{ST}	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Settling time measured while DACR<4:0> transitions from '00000' to '01111'.

TABLE 35-16: FIXED VOLTAGE REFERENCE (FVR) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
FVR01	V_{FVR1}	1x Gain (1.024V nominal)	-4	—	4	%	V_{DD} ≥ 2.5V, -40°C to 85°C
FVR02	V_{FVR2}	2x Gain (2.048V nominal)	-4	—	4	%	V_{DD} ≥ 2.5V, -40°C to 85°C
FVR03	V_{FVR4}	4x Gain (4.096V nominal)	-5	—	5	%	V_{DD} ≥ 4.75V, -40°C to 85°C
FVR04	T_{FVRST}	FVR Start-up Time	—	—	—	µs	

TABLE 35-24: I²C BUS DATA CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
SP100*	THIGH	Clock high time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP101*	TLOW	Clock low time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5TCY	—		
SP102*	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL fall time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
SP107*	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
SP111	CB	Bus capacitive loading		—	400	pF	

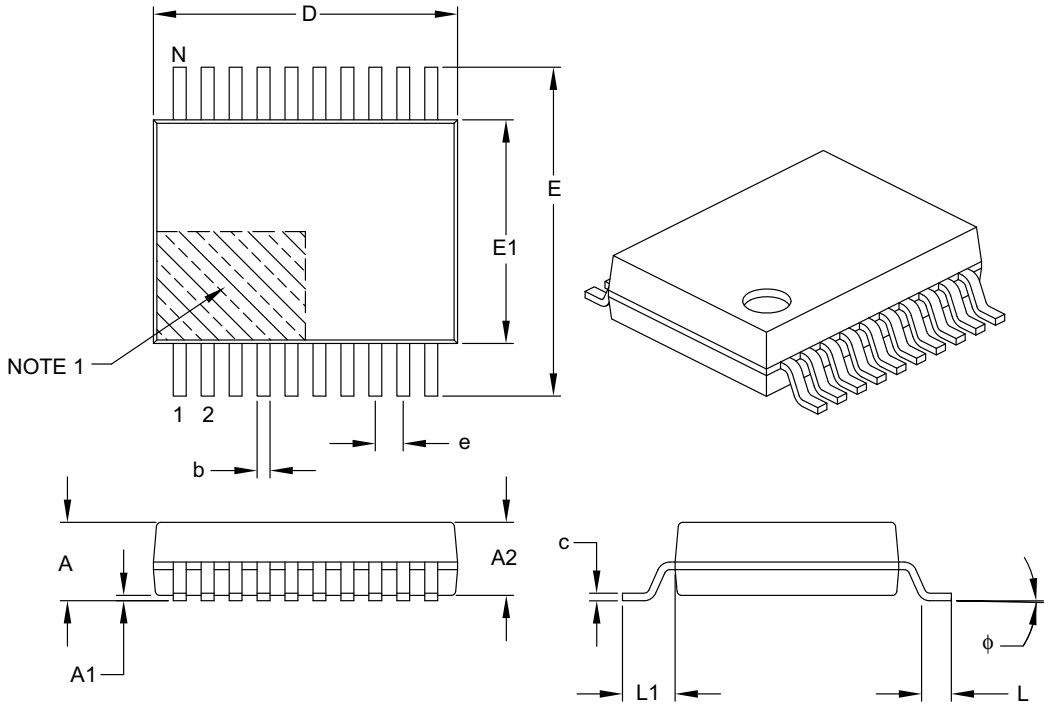
* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

