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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XF

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18325t-i-st

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



4.2.2.1 STATUS Register

The STATUS register, shown in Register 4-1, contains:

- The arithmetic status of the ALU
- · The Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

REGISTER 4-1: STATUS: STATUS REGISTER

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to Section 34.0 "Instruction Set Summary").

Note 1:	The C and DC bits operate as Borrow
	and Digit Borrow out bits, respectively, in
	subtraction.

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
_	_	_	TO	PD	Z	DC ⁽¹⁾	C ⁽¹⁾
bit 7	•						bit 0
Legend:							
R = Readable I	bit	W = Writable	bit	U = Unimpler	mented bit, read	l as '0'	
u = Bit is uncha	anged	x = Bit is unkn	iown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared	q = Value der	pends on condit	ion	

bit 7-5	Unimplemented: Read as '0'
bit 4	TO: Time-Out bit
	1 = After power-up, CLRWDT instruction or SLEEP instruction 0 = A WDT Time-out occurred
bit 3	PD: Power-Down bit
	 1 = After power-up or by the CLRWDT instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit
	 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	 DC: Digit Carry/Digit Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)⁽¹⁾ 1 = A carry-out from the 4th low-order bit of the result occurred 0 = No carry-out from the 4th low-order bit of the result
bit 0	C : Carry/Borrow bit ⁽¹⁾ (ADDWF, ADDLW, SUBLW, SUBWF instructions) ⁽¹⁾ 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

R-q/q	R-q/q	U-0	R-q/q	R-q/q	R-q/q	U-0	R-q/q
EXTOR	HFOR	—	LFOR	SOR	ADOR	—	PLLR
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimple	mented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BC	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is cle	ared				
q = Reset valu	e is determine	d by hardware					
bit 7	EXTOR: EXT	OSC (external) Oscillator Re	ady			
	1 = The osc	illator is ready	to be used				
	0 = The osc	illator is not en	abled, or is no	t yet ready to t	be used.		
bit 6	HFOR: HFIN	TOSC Oscillato	or Ready				
	0 = The osc	illator is not en	abled, or is no	t vet readv to b	be used.		
bit 5	Unimplemen	ted: Read as '	0'	- , , ,			
bit 4	LFOR: LFINT	OSC Oscillato	r Readv				
	1 = The osc	illator is ready	to be used				
	0 = The osc	cillator is not er	nabled, or is no	ot yet ready to	be used.		
bit 3	SOR: Second	lary Oscillator	Ready				
	1 = The osc	illator is ready	to be used	t vot roodv to	hawaad		
h # 0		Consiliator S not er	abled, or is no	of yet ready to	be used.		
DIL 2	1 = The osc	illator is ready	to be used				
	0 = The osc	cillator is not er	abled, or is no	ot yet ready to	be used		
bit 1	Unimplemen	ted: Read as '	0'	- •			
bit 0	PLLR: PLL is	ready					
	1 = The PLL	is ready to be	used				
	0 = The PLL	is not enable	d, the required	input source is	s not ready, or t	he PLL is not r	eady.

REGISTER 7-4: OSCSTAT1: OSCILLATOR STATUS REGISTER 1

U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
—	—	—	—		HFFR	Q<3:0>	
bit 7							bit 0
Logondi							

REGISTER 7-6: OSCFRQ: HFINTOSC FREQUENCY SELECTION REGISTER

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 Unimplemented: Read as '0'.

bit 3-0 HFFRQ<3:0>: HFINTOSC Frequency Selection bits

HFFRQ<3:0>	Nominal Freq. (MHz) (NOSC = 110)	2xPLL Freq. (MHz) (NOSC = 000)
0000	1	
0001	2	Peserved
0010	Reserved	Reserved
0011	4	
0100	8	16
0101	12	24
0110	16	32
0111	32	Peserved
1xxx	32	I COOLINEO

EXAMPLE 11-3: ERASING ONE ROW OF PROGRAM FLASH MEMORY

; This sample row erase routine assumes the following: ; 1.A valid address within the erase row is loaded in variables ADDRH:ADDRL ; 2.ADDRH and ADDRL are located in common RAM (locations 0x70 - 0x7F)

BANKSEL	NVMADRL	
MOVF	ADDRL,W	
MOVWF	NVMADRL	; Load lower 8 bits of erase address boundary
MOVF	ADDRH,W	
MOVWF	NVMADRH	; Load upper 6 bits of erase address boundary
BCF	NVMCON1,NVMREGS	; Choose Program Flash Memory area
BSF	NVMCON1, FREE	; Specify an erase operation
BSF	NVMCON1,WREN	; Enable writes
BCF	INTCON,GIE	; Disable interrupts during unlock sequence
;	RE	QUIRED UNLOCK SEQUENCE:
MOLT II	E E b	· I and EEb to got woody for unlock company
MOVLW	5511	, Load 55h to get ready for unlock sequence
MOVWF		
	NVMCON2	; First step is to load 55h into NVMCON2
MOVLW	NVMCON2 AAh	; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W
MOVLW MOVWF	NVMCON2 AAh NVMCON2	; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W ; Third step is to load AAh into NVMCON2
MOVLW MOVWF BSF	NVMCON2 AAh NVMCON2 NVMCON1,WR	<pre>; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W ; Third step is to load AAh into NVMCON2 ; Final step is to set WR bit</pre>
MOVLW MOVWF BSF ;	NVMCON2 AAh NVMCON2 NVMCON1,WR	; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W ; Third step is to load AAh into NVMCON2 ; Final step is to set WR bit
MOVLW MOVWF BSF ;	NVMCON2 AAh NVMCON2 NVMCON1,WR INTCON,GIE	<pre>; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W ; Third step is to load AAh into NVMCON2 ; Final step is to set WR bit</pre>
MOVLW MOVWF BSF ; BSF BCF	NVMCON2 AAh NVMCON2 NVMCON1,WR INTCON,GIE NVMCON1,WREN	<pre>; First step is to load 55h into NVMCON2 ; Second step is to load AAh into W ; Third step is to load AAh into NVMCON2 ; Final step is to set WR bit</pre>

TABLE 11-2: NVM ORGANIZATION AND ACCESS INFORMATION

Master Values			NVMREG Access			FSR Access	
Memory Function	Program Counter (PC), ICSP™ Address	Memory Type	NVMREGS bit (NVMCON1)	NVMADR <14:0>	Allowed Operations	FSR Address	FSR Programming Address
Reset Vector	0000h		0	0000h		8000h	
User Memory	0001h	Program	0	0001h		8001h	
	0003h	Flash		0003h	READ	8003h	
INT Vector	0004h	Memory	0	0004h	WRITE	8004h	READ-ONET
User Memory	0005h		0	0005h		8005h	1
	17FFh			17FFh		FFFFh	
User ID		Program	1	0000h			
		Flash Memory		0003h	READ		
Reserved		_	—	0004h	_		
Rev ID			1	0005h		No	Access
Device ID	No PC Address	_	1	0006h		110	100000
CONFIG1		Program	1	0007h			
CONFIG2		Memory	1	0008h	READ		
CONFIG3			1	0009h			
CONFIG4				000Ah			
User Memory		EEPROM	1	7000h	READ	7000h	READ-ONLY
				70FFh	WRITE	70FFh	

12.6 PORTC Registers

12.6.1 DATA REGISTER

PORTC is a bidirectional port that is either 6-bit wide (PIC16(L)F18325) or 8-bit wide (PIC16(L)F18345). The corresponding data direction register is TRISC (Register 12-18). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 12-1 shows how to initialize an I/O port.

Reading the PORTC register (Register 12-17) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATC).

The PORT data latch LATC (Register 12-19) holds the output port data, and contains the latest value of a LATC or PORTC write.

12.6.2 DIRECTION CONTROL

The TRISC register (Register 12-18) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

12.6.3 INPUT THRESHOLD CONTROL

The INLVLC register (Register 12-24) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 35-4 for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

12.6.4 OPEN-DRAIN CONTROL

The ODCONC register (Register 12-22) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONC bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONC bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

Note: It is not necessary to set open-drain control when using the pin for I²C; the I²C module controls the pin and makes the pin open-drain.

12.6.5 SLEW RATE CONTROL

The SLRCONC register (Register 12-23) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONC bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONC bit is cleared, The corresponding port pin drive slews at the maximum rate available.

12.6.6 ANALOG CONTROL

The ANSELC register (Register 12-20) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELC bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELC bits has no effect on digital output functions. A pin with TRIS clear and ANSELC set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELC bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

12.6.7 WEAK PULL-UP CONTROL

The WPUC register (Register 12-21) controls the individual weak pull-ups for each PORT pin.

12.6.8 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the peripheral pin select logic. See **Section 13.0** "**Peripheral Pin Select (PPS) Module**" for more information.

Analog output functions, such as ADC and comparator inputs, are not shown in the peripheral pin select lists. Digital output functions may continue to control the pin when it is in Analog mode.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	—		-	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable I	bit	U = Unimpler	mented bit, read	as '0'	
u = Bit is unchanged x = Bit is unknown			-n/n = Value at POR and BOR/Value at all other Resets				
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 15-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER⁽¹⁾

bit 7-4	IOCBN<7:4>: Interrupt-on-Change PORTB Negative Edge Enable bits 1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAFx bit and IOCIF flag will
	be set upon detecting an edge.
	0 = Interrupt-on-Change disabled for the associated pin
bit 3-0	Unimplemented: Read as '0'

Note 1: PIC16(L)F18345 only.

REGISTER 15-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER⁽¹⁾

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	_	—	—	—
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-4 **IOCBF<7:4>:** Interrupt-on-Change PORTB Flag bits 1 = An enabled change was detected on the associated pin

Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.

0 = No change was detected, or the user cleared the detected change.

bit 3-0 Unimplemented: Read as '0'

Note 1: PIC16(L)F18345 only.

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CxINTP	CxINTN		CxPCH<2:0>		CxNCH<2:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value	at POR and BC	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is cle	ared				
bit 7	CxINTP: Con 1 = The CxIF 0 = No intern	nparator Interru interrupt flag v upt flag will be	ipt on Positive will be set upo set on a positi	e Going Edge E n a positive go ive going edge	nable bits ing edge of the of the CxOUT I	CxOUT bit bit	
bit 6	CxINTN: Comparator Interrupt on Negative Going Edge Enable bits 1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit						
bit 5-3	CxPCH<2:0>: Comparator Positive Input Channel Select bits 111 = CxVP connects to Vss 110 = CxVP connects to FVR Buffer 2 101 = CxVP connects to DAC output 100 = CxVP unconnected 011 = CxVP unconnected 010 = CxVP unconnected 010 = CxVP unconnected 001 = CxVP unconnected 001 = CxVP unconnected 001 = CxVP unconnected 001 = CxVP connects to CxIN0+ pin						
bit 2-0	CxNCH<2:0>: Comparator Negative Input Channel Select bits 111 = CxVN connects to Vss 110 = CxVN connects to FVR Buffer 2 101 = CxVN unconnected 100 = CxVN unconnected 011 = CxVN connects to CxIN3- pin 010 = CxVN connects to CxIN2- pin 001 = CxVN connects to CxIN1- pin 000 = CxVN connects to CxIN0- pin						

REGISTER 18-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

19.2 Register Definitions: PWM Control

NEOIOTEN I	J ⁻ 1 . 1 WWA			LOIDIEN			
R/W-0/0	U-0	R-0	R/W-0/0	U-0	U-0	U-0	U-0
PWMxEN	—	PWMxOUT	PWMxPOL	—	—	_	—
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
u = Bit is unchanged x = Bit is unknown		nown	-n/n = Value a	at POR and BC	R/Value at all	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	PWMxEN: PV	VM Module En	able bit				
	1 = PWM mo	dule is enable	d				
	0 = PWM mc	dule is disable	d				
bit 6	Unimplemen	ted: Read as '	0'				
bit 5	PWMxOUT: F	PWM Module C	output Level wh	nen bit is read.			
bit 4	PWMxPOL: PWMx Output Polarity Select bit						
	1 = PWM output is active-low.						
	0 = PWM out	tput is active-hi	gh.				
bit 3-0	Unimplemen	ted: Read as '	0'				

REGISTER 19-1: PWMxCON: PWM CONTROL REGISTER

REGISTER 19-2: PWMxDCH: PWM DUTY CYCLE HIGH BITS

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PWMxDC<9:2>							
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PWMxDC<9:2>:** PWM Duty Cycle Most Significant bits

These bits are the MSbs of the PWM duty cycle. The two LSbs are found in PWMxDCL Register.

REGISTER 19-3: PWMxDCL: PWM DUTY CYCLE LOW BITS

R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	U-0	U-0
PWMxD)C<1:0>	—	—	—	—	—	—
bit 7 bit 0							

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **PWMxDC<1:0>:** PWM Duty Cycle Least Significant bits These bits are the LSbs of the PWM duty cycle. The MSbs are found in PWMxDCH Register.

bit 5-0 Unimplemented: Read as '0'

Full-Bridge Reverse Mode

In Full-Bridge Reverse mode (MODE<2:0> = 011),

CWGxC is driven to its active state and CWGxB is modulated while CWGxA and CWGxD are driven to

their inactive state, as illustrated at the bottom of

20.2.4.2

Figure 20-6.

20.2.4.1 Full-Bridge Forward Mode

In Full-Bridge Forward mode (MODE<2:0> = 010), CWGxA is driven to its active state and CWGxD is modulated while CWGxB and CWGxC are driven to their inactive state, as illustrated at the top of Figure 20-6.

FIGURE 20-6: EXAMPLE OF FULL-BRIDGE OUTPUT



20.2.4.3 Direction Change in Full-Bridge Mode

In Full-Bridge mode, changing MODE<2:0> controls the forward/reverse direction. Changes to MODE<2:0> change to the new direction on the next rising edge of the modulated input.

A direction change is initiated in software by changing the MODE<2:0> bits of the WGxCON0 register. The sequence is illustrated in Figure 20-7.

- The associated active output CWGxA and the inactive output CWGxC are switched to drive in the opposite direction.
- The previously modulated output CWGxD is switched to the inactive state, and the previously inactive output CWGxB begins to modulate.
- CWG modulation resumes after the direction-switch dead band has elapsed.

REGISTER 21-11:	CLCDATA: CLC DATA OUTPUT
-----------------	--------------------------

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	_	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

- bit 3 MLC4OUT: Mirror copy of LC4OUT bit
- bit 2 MLC3OUT: Mirror copy of LC3OUT bit
- bit 1 MLC2OUT: Mirror copy of LC2OUT bit
- bit 0 MLC1OUT: Mirror copy of LC1OUT bit

TABLE 21-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

Name	Bit7	Bit6	Bit5	Bit4	Blt3	Bit2	Bit1	Bit0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	—	ANSA2	ANSA1	ANSA0	144
TRISA	—	—	TRISA5	TRISA4	_(2)	TRISA2	TRISA1	TRISA0	143
ANSELB ⁽¹⁾	ANSB7	ANSB6	ANSB5	ANSB4	—	—		—	150
TRISB ⁽¹⁾	TRISB7	TRISB6	TRISB5	TRISB4	—	—	_	—	149
ANSELC	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	ANSC5	ANSC4	ANSC3	ANSC2	ANSC1	ANSC0	157
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	156
INTCON	GIE	PEIE	—	—	—	—	-	INTEDG	101
PIR3	OSFIF	CSWIF	TMR3GIF	TMR3IF	CLC4IF	CLC3IF	CLC2IF	CLC1IF	110
PIE3	OSFIE	CSWIE	TMR3GIE	TMR3IE	CLC4IE	CLC3IE	CLC2IE	CLC1IE	105
CLC1CON	LC1EN	—	LC10UT	LC1INTP	LC1INTN	LC1MODE<2:0>			227
CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	228
CLC1SEL0	—	—		LC1D1S<5:0>					
CLC1SEL1	—	—		LC1D2S<5:0>					
CLC1SEL2	—	—			LC1D3	3S<5:0>			229
CLC1SEL3	—	—			LC1D4	4S<5:0>			230
CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	230
CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	231
CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	232
CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	233
CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	L	C2MODE<2:0	>	227
CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	228
CLC2SEL0	—	_			LC2D1	IS<5:0>			229
CLC2SEL1	—	—			LC2D2	2S<5:0>			229
CLC2SEL2	—	—			LC2D3	3S<5:0>			229
CLC2SEL3	—	—			LC2D4	IS<5:0>			230

Legend: — = Unimplemented, read as '0'. Shaded cells are unused by the CLC module.

U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
—	—	—			DAC1R<4:0>			
bit 7 bi								
Legend:								
R = Readable	bit	W = Writable	bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unkno			iown	-n/n = Value a	at POR and BO	R/Value at all c	ther Resets	

REGISTER 24-2: DACCON1: VOLTAGE REFERENCE CONTROL REGISTER 1

bit 7-5 **Unimplemented:** Read as '0'

1' = Bit is set

bit 4-0 DAC1R<4:0>: DAC1 Voltage Output Select bits VOUT = (VSRC+ - VSRC-)*(DAC1R<4:0>/32) + VSRC

'0' = Bit is cleared

TABLE 24-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC1 MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
DACCON0	DAC1EN	—	DAC10E		DAC1PS	SS<1:0>	—	DAC1NSS	263
DACCON1	—	—	—	DAC1R<4:0>				264	
CMxCON1	CxINTP	CxINTN	C>	CxPCH<2:0> CxNCH<2:0>				191	
ADCON0			CHS<	CHS<5:0> GO/DONE ADON					

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used with the DAC module.

29.4.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

- Use the desired output pin RxyPPS control to select CCPx as the source and disable the CCPx pin output driver by setting the associated TRIS bit.
- 2. Load the PR2 register with the PWM period value.
- Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
- 4. Load the CCPRxL register and the CCPRxH register bits, with the PWM duty cycle value and configure the CCPxFMT bit of the CCPxCON register to set the proper register alignment.
- 5. Configure and start Timer2, 4 or 6.
 - Clear the TMR2/4/6IF interrupt flag bits of the PIR4 register. See Note below.
 - Configure the T2/4/6CKPS bits of the T2/4/6CON register with the Timer prescale value.
 - Enable the Timer by setting the TMR2/4/6ON bit of the T2/4/6CON register.
- 6. Enable PWM output pin:
 - Wait until the Timer overflows and the TMR2/4/6IF bits of the PIR4 register is set. See Note below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.
- **Note:** In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

29.4.3 TIMER2/4/6 TIMER RESOURCE

The PWM standard mode makes use of the 8-bit Timer2/4/6 timer resources to specify the PWM period.

29.4.4 PWM PERIOD

The PWM period is specified by the PRx register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 29-1.

EQUATION 29-1: PWM PERIOD

 $PWM Period = [(PR2x) + 1] \bullet 4 \bullet Tosc \bullet$

(TMR2/4/6 Prescale Value)

Note: Tosc = 1/Fosc

When TMR2/4/6 is equal to PR2/4/6, the following three events occur on the next increment cycle:

- · TMR2/4/6 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is transferred from the CCPRxL/H register pair into a 10-bit buffer.

Note: The Timer postscaler (see Section 28.1 "Timer2 Operation") is not used in the determination of the PWM frequency.

29.4.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to the CCPRxH:CCPRxL register pair. The alignment of the 10-bit value is determined by the CCPRxFMT bit of the CCPxCON register (see Figure 29-5). The CCPRxH:CCPRxL register pair can be written to at any time; however, the duty cycle value is not latched into the 10-bit buffer until after a match between PR2/4/6 and TMR2/4/6.

Equation 29-2 is used to calculate the PWM pulse width.

Equation 29-3 is used to calculate the PWM duty cycle ratio.

FIGURE 29-5: PWM 10-BIT ALIGNMENT BLOCK DIAGRAM





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Preliminary

30.6.7 I²C MASTER MODE RECEPTION

Master mode reception (Figure 30-29) is enabled by programming the Receive Enable bit, RCEN bit of the SSPxCON2 register.

Note:	The MSSPx module must be in an Idle
	state before the RCEN bit is set or the
	RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPxSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPxSR are loaded into the SSPxBUF, the BF flag bit is set, the SSPxIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSPx is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPxCON2 register.

30.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPxBUF from SSPxSR. It is cleared when the SSPxBUF register is read.

30.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPxSR and the BF flag bit is already set from a previous reception.

30.6.7.3 WCOL Status Flag

If the user writes the SSPxBUF when a receive is already in progress (i.e., SSPxSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

30.6.7.4 Typical Receive Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSPxCON2 register.
- 2. SSPxIF is set by hardware on completion of the Start.
- 3. SSPxIF is cleared by software.
- 4. User writes SSPxBUF with the slave address to transmit and the R/W bit set.
- 5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPxBUF is written to.
- 6. The MSSPx module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSPxCON2 register.
- The MSSPx module generates an interrupt at the end of the ninth clock cycle by setting the SSPxIF bit.
- 8. User sets the RCEN bit of the SSPxCON2 register and the master clocks in a byte from the slave.
- 9. After the eighth falling edge of SCL, SSPxIF and BF are set.
- 10. Master clears SSPxIF and reads the received byte from SSPxBUF, clears BF.
- 11. Master sets ACK value sent to slave in ACKDT bit of the SSPxCON2 register and initiates the ACK by setting the ACKEN bit.
- 12. Master's ACK is clocked out to the slave and SSPxIF is set.
- 13. User clears SSPIF.
- 14. Steps 8-13 are repeated for each received byte from the slave.
- 15. Master sends a not ACK or Stop to end communication.

30.6.13.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- a) SDA or SCL are sampled low at the beginning of the Start condition (Figure 30-33).
- b) SCL is sampled low before SDA is asserted low (Figure 30-34).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- · the Start condition is aborted,
- the BCL1IF flag is set and
- the MSSPx module is reset to its Idle state (Figure 30-33).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded and counts down. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 30-35). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to zero; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.





RETLW	Return with literal in W				
Syntax:	[<i>label</i>] RETLW k				
Operands:	$0 \le k \le 255$				
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC				
Status Affected:	None				
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.				
Words:	1				
Cycles:	2				
Example:	CALL TABLE;W contains table ;offset value ;W now has table value				
TABLE	• • ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • • RETLW kn ; End of table				
	Before Instruction				

• RETLW	kn	;	End of table
Before In	struc W	tio =	n : 0x07
After Inst	ructic W	on =	value of k8

RETURN **Return from Subroutine**

Syntax:	[label] RETURN
Operands:	None
Operation:	$TOS \rightarrow PC$
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

RLF	Rotate Left f through Carry						
Syntax:	[<i>label</i>] RLF f,d						
Operands:	$0 \le f \le 127$ $d \in [0,1]$						
Operation:	See description below						
Status Affected:	С						
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.						
Words:	1						
Cycles:	1						
Example:	RLF REG1,0						
	Before Instruction						
	REG1 = 1110 0110						
	C = 0						
	After Instruction						
	REG1 = 1110 0110						
	$W = 1100 \ 1100$						
	C = 1						
RRF	Rotate Right f through Carry						

Syntax:	[<i>label</i>] RRF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	See description below
Status Affected:	С
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



Package Marking Information (Continued)



14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VI	EW	С

	Units	MILLIMETERS				
Dimension Lin	nits	MIN	NOM	MAX		
Number of Pins	N	14				
Pitch	е		1.27 BSC			
Overall Height	А	-	-	1.75		
Molded Package Thickness	A2	1.25	-	-		
Standoff §	A1	0.10	-	0.25		
Overall Width	Е	6.00 BSC				
Molded Package Width	E1	3.90 BSC				
Overall Length	D	8.65 BSC				
Chamfer (Optional)	h	0.25	-	0.50		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.04 REF				
Lead Angle	Θ	0°	-	-		
Foot Angle	φ	0°	-	8°		
Lead Thickness	С	0.10	-	0.25		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5°	_	15°		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic
- 3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.
- 5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A