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Details

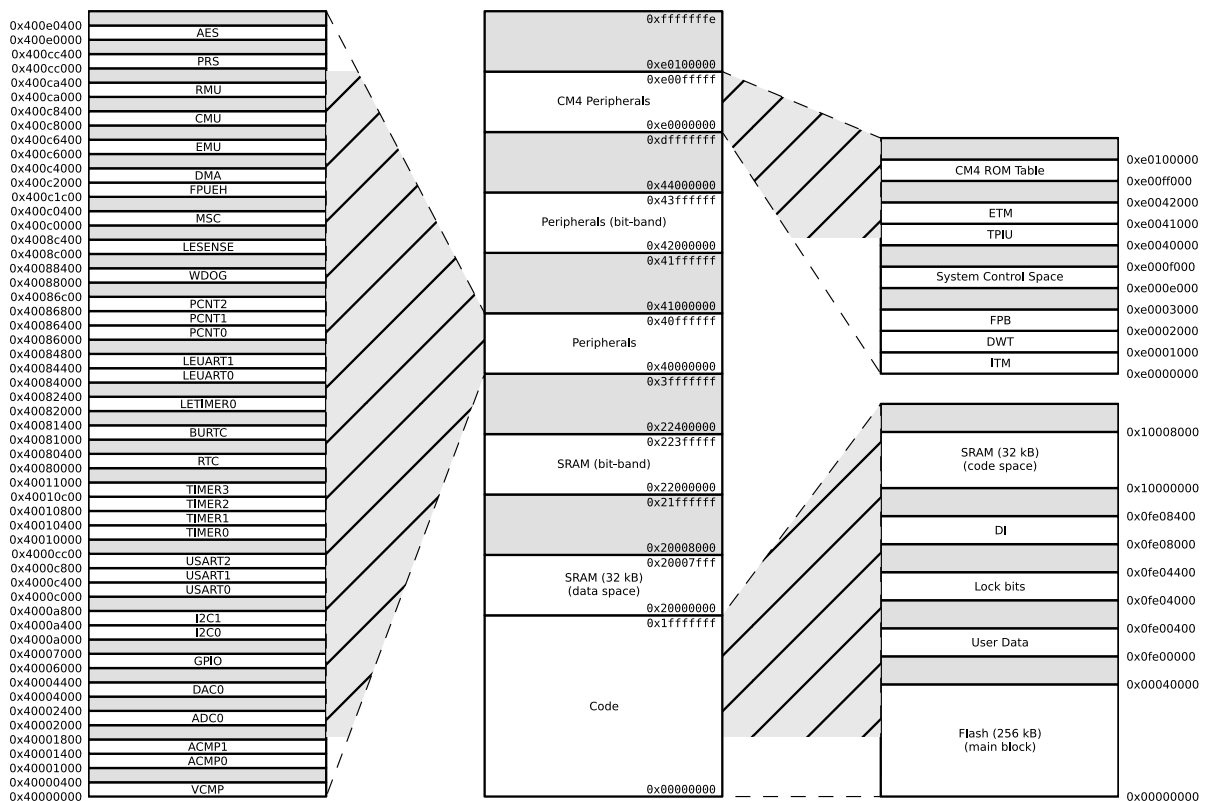
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg232f64-qfp64t

Module	Configuration	Pin Connections
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP		
AES	Full configuration	NA
GPIO	53 pins	Available pins are shown in Table 4.3 (p. 60)

2.3 Memory Map

The EFM32WG232 memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG232 Memory Map with largest RAM and Flash sizes



3.3.2 Environmental

Table 3.3. Environmental

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V _{ESDHBM}	ESD (Human Body Model HBM)	T _{AMB} =25°C			2000	V
V _{ESDCDM}	ESD (Charged Device Model, CDM)	T _{AMB} =25°C			750	V

Latch-up sensitivity passed: $\pm 100 \text{ mA}/1.5 \times V_{\text{SUPPLY}}(\text{max})$ according to JEDEC JESD 78 method Class II, 85°C.

3.4 Current Consumption

Table 3.4. Current Consumption

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I _{EM0}	EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		225	236	μA/ MHz
		48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		225		μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		226	238	μA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		227		μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		228	240	μA/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		229		μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		230	243	μA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		231		μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		232	245	μA/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		233		μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C		238	250	μA/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C		238		μA/ MHz

Figure 3.3. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz

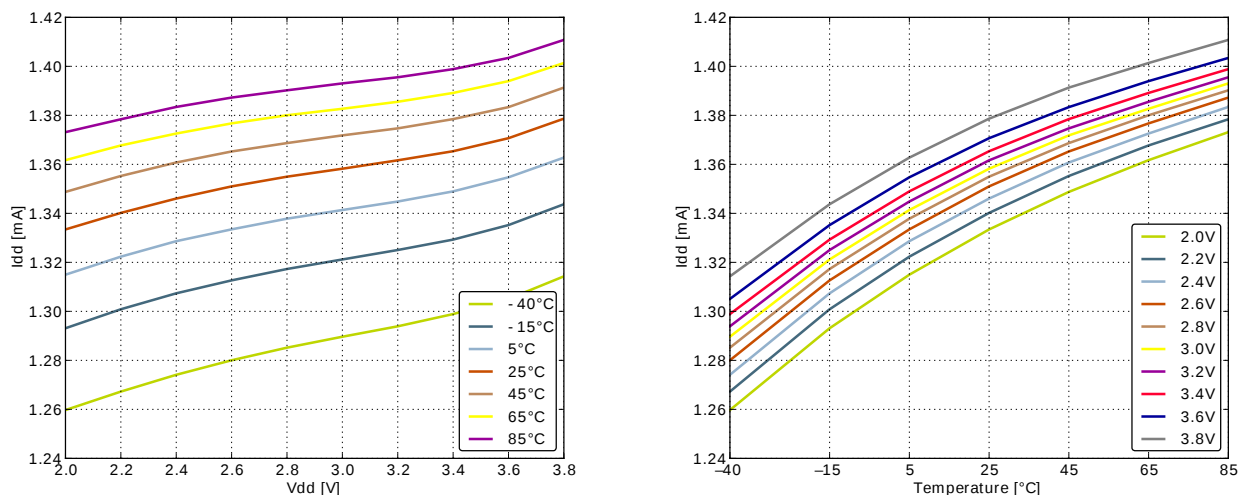


Figure 3.4. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz

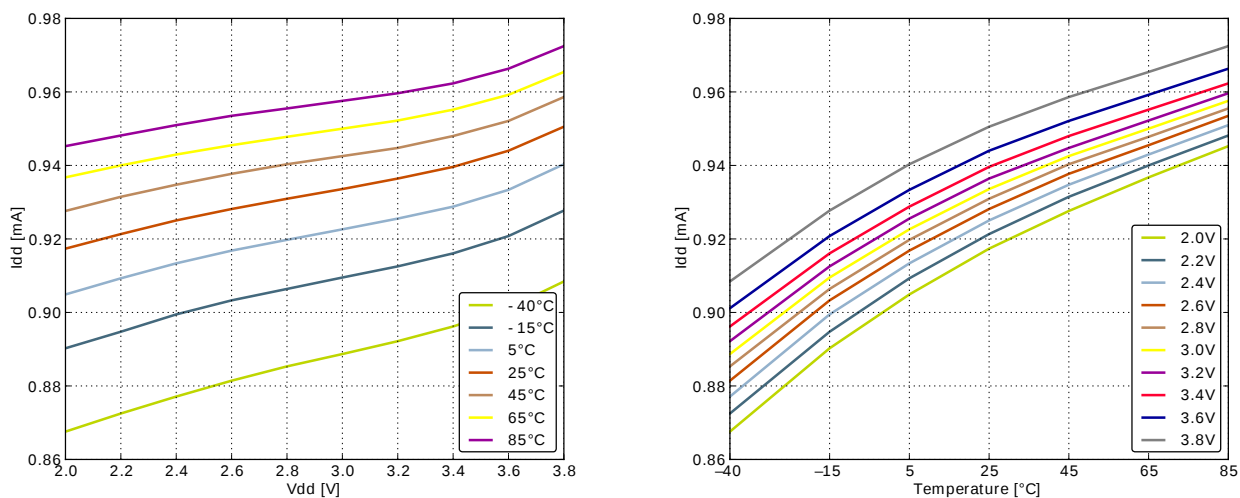


Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz

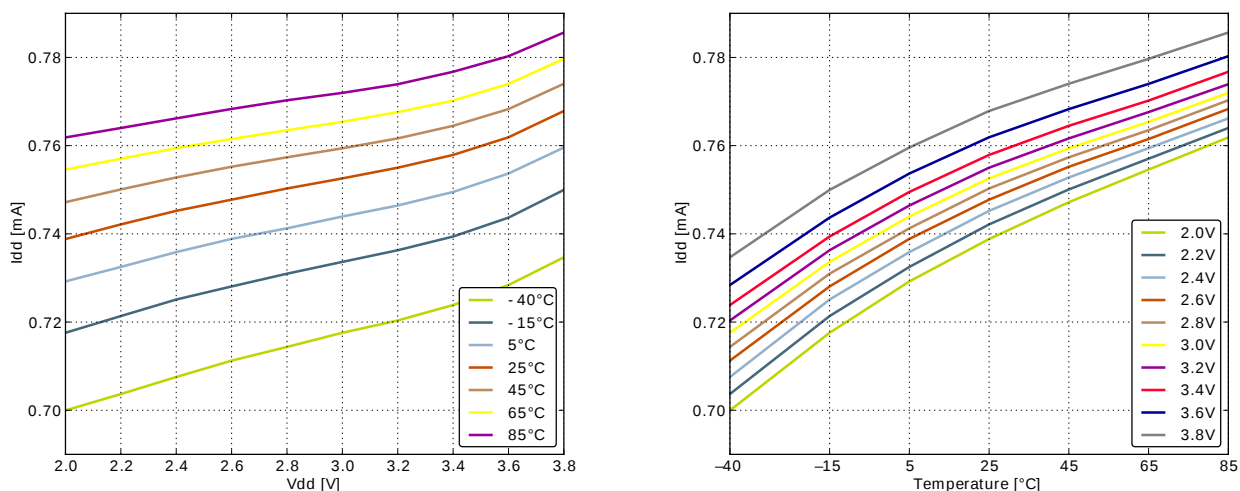


Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz

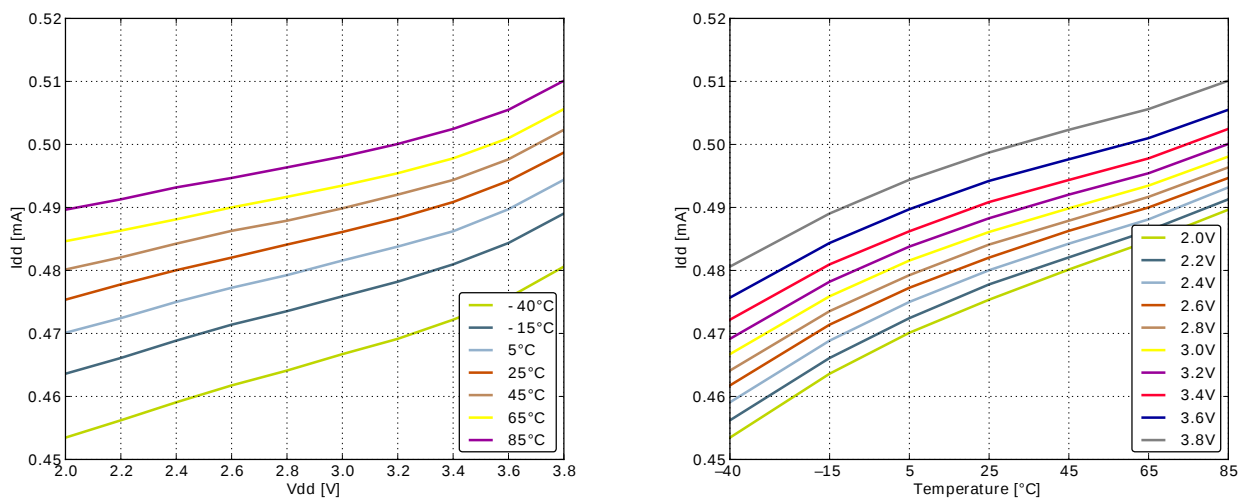
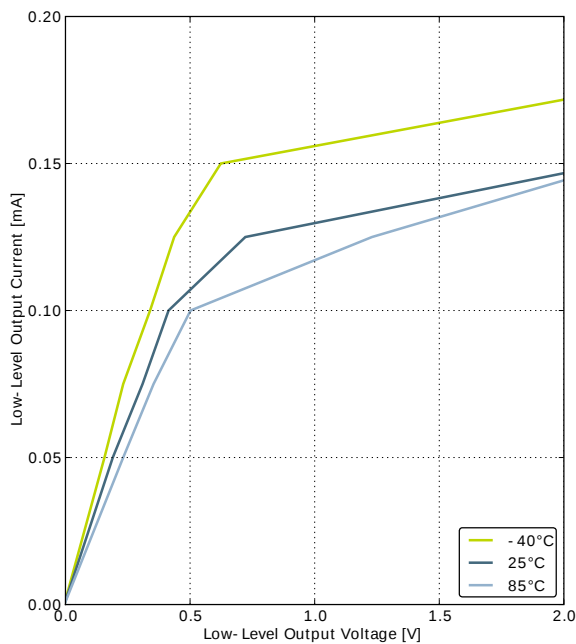
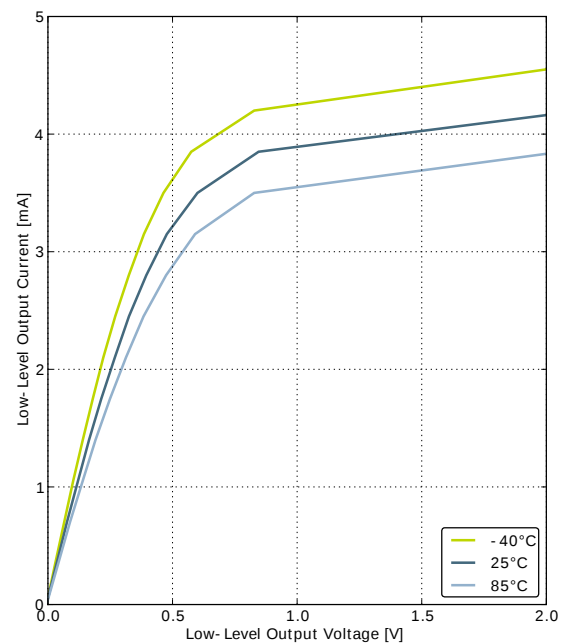


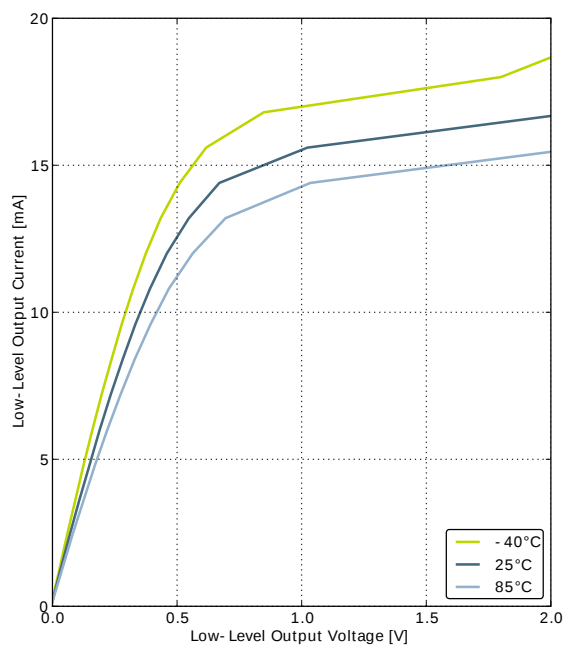
Figure 3.11. Typical Low-Level Output Current, 2V Supply Voltage



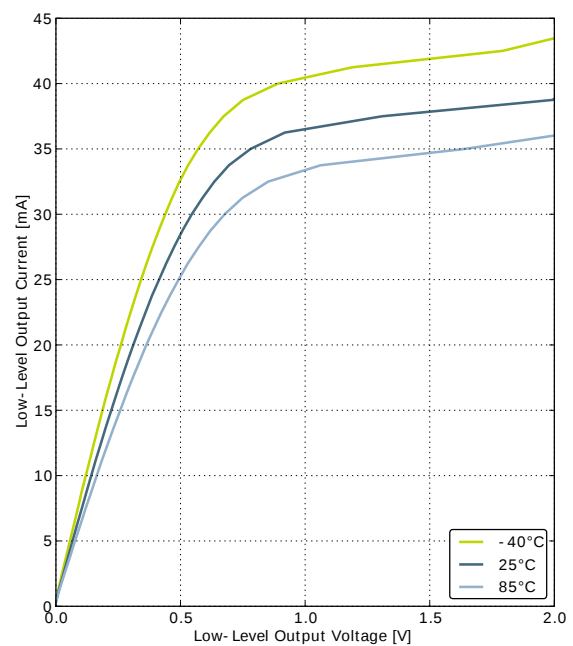
GPIO_Px_CTRL DRIVEMODE = LOWEST



GPIO_Px_CTRL DRIVEMODE = LOW

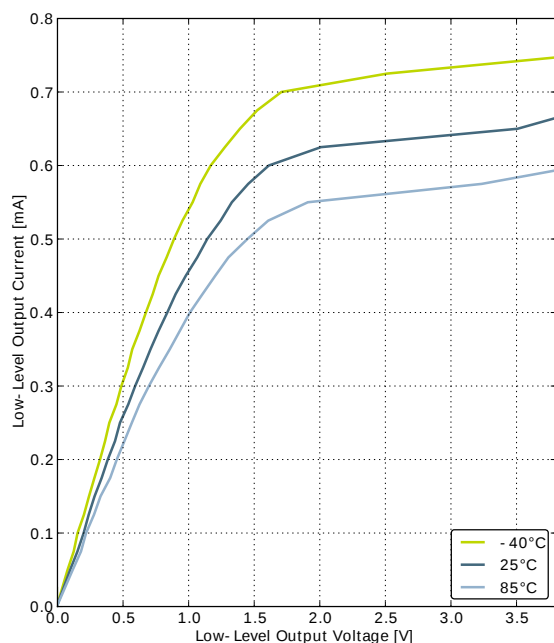


GPIO_Px_CTRL DRIVEMODE = STANDARD

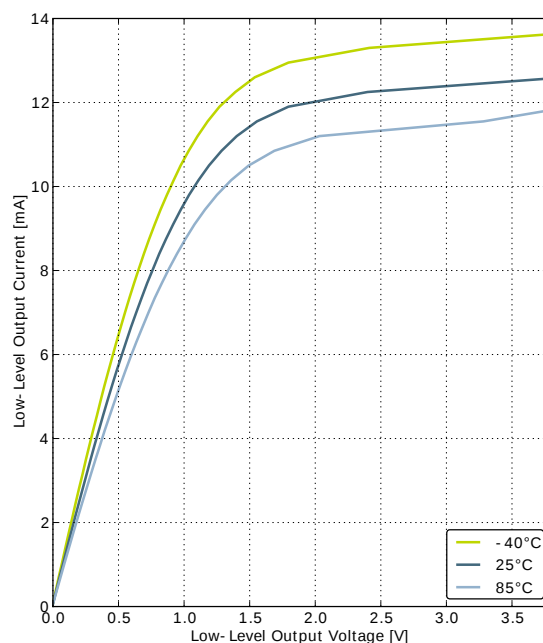


GPIO_Px_CTRL DRIVEMODE = HIGH

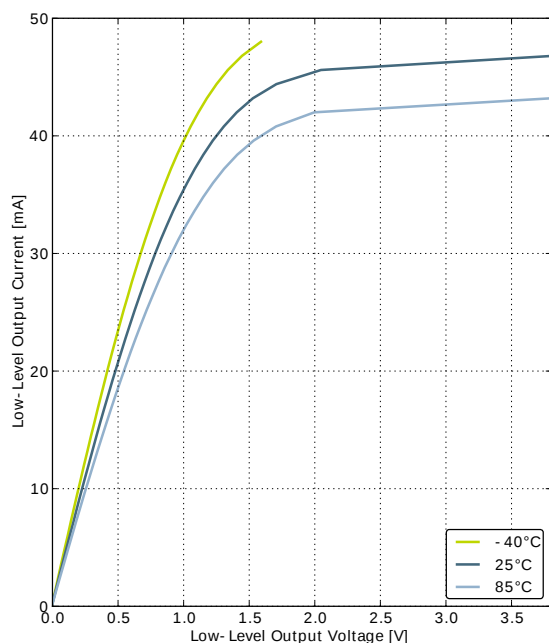
Figure 3.15. Typical Low-Level Output Current, 3.8V Supply Voltage



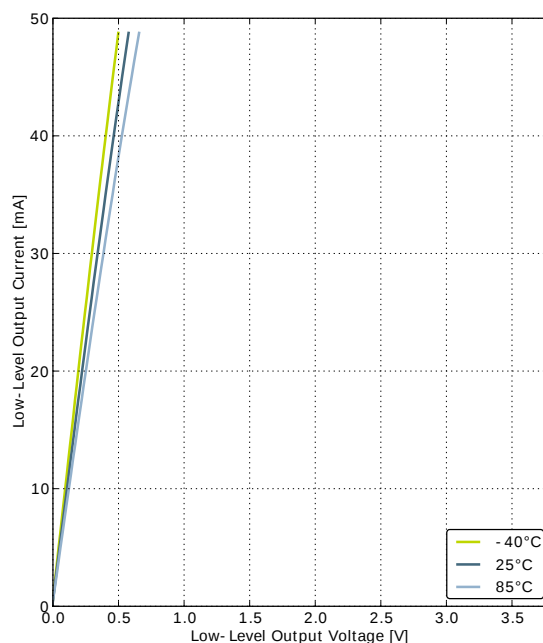
GPIO_Px_CTRL DRIVEMODE = LOWEST



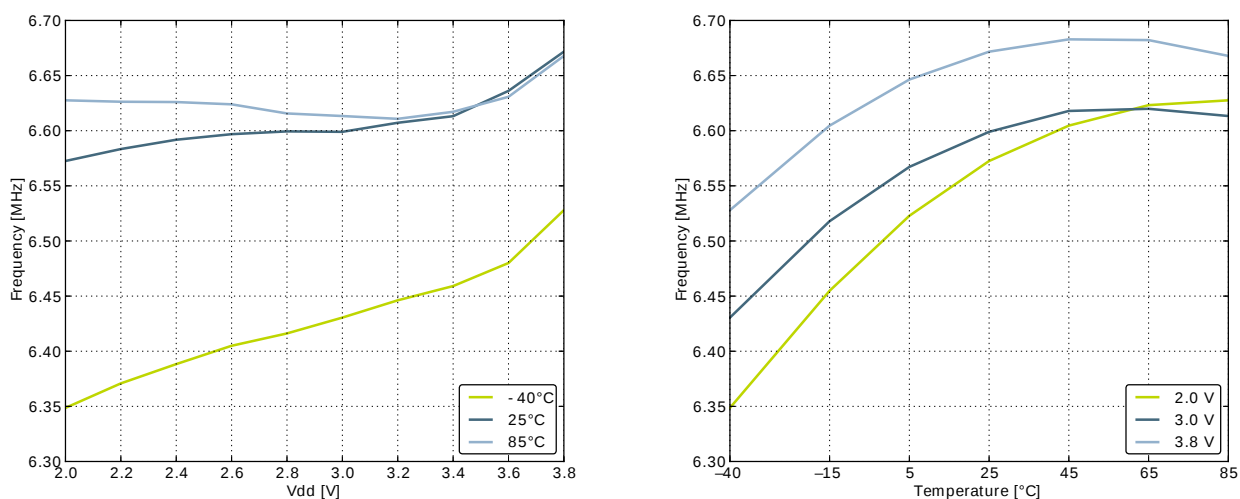
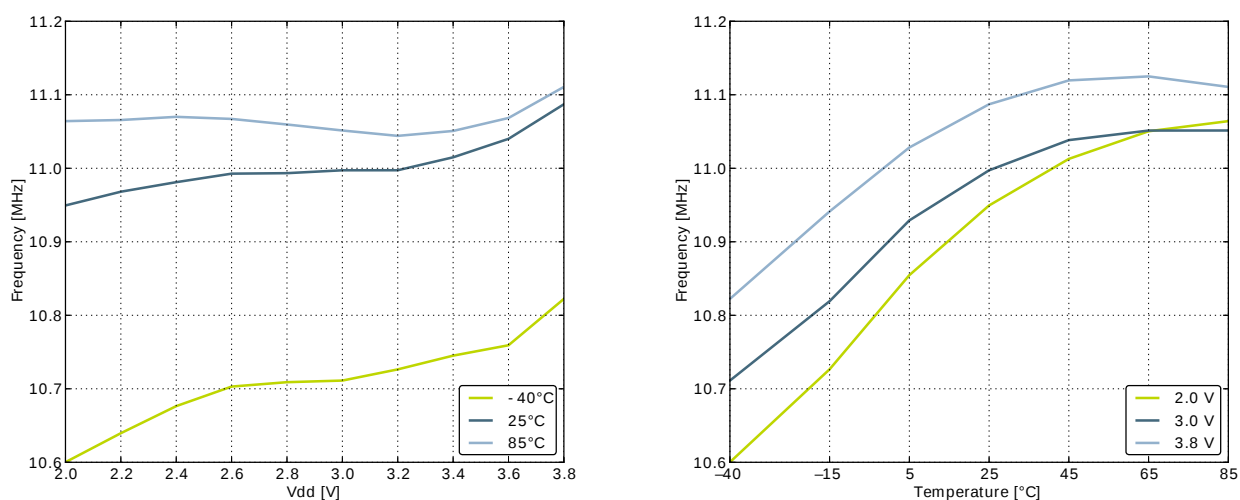
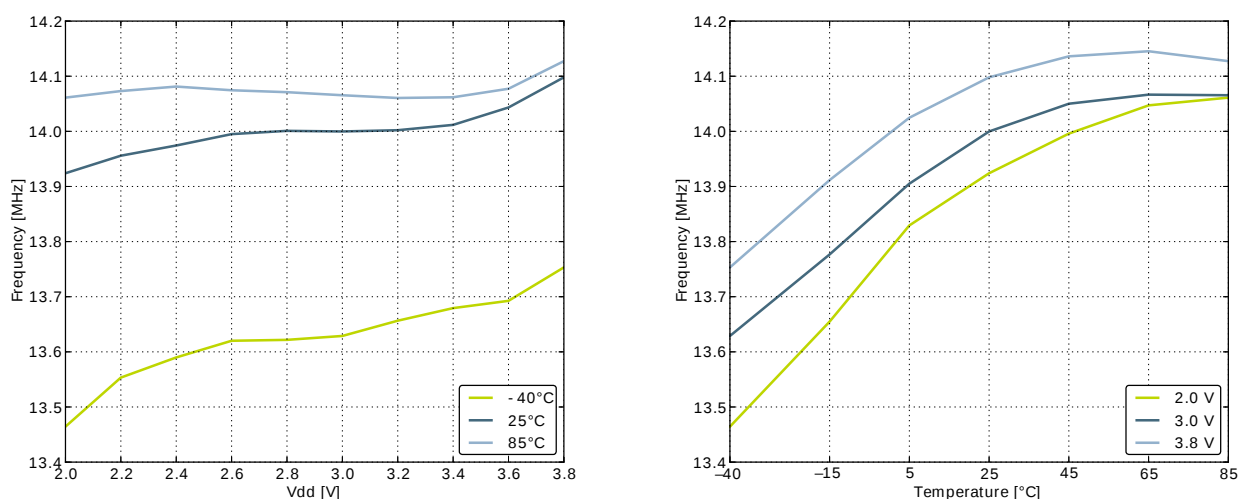
GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD



GPIO_Px_CTRL DRIVEMODE = HIGH

Figure 3.19. Calibrated HFRCO 7 MHz Band Frequency vs Supply Voltage and Temperature**Figure 3.20. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature****Figure 3.21. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	and ADC core in NORMAL mode					
	Startup time of reference generator and ADC core in KEEPADCWARM mode			1		μs
SNR _{ADC}	Signal to Noise Ratio (SNR)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		59		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		65		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB
		1 MSamples/s, 12 bit, differential, internal 2.5V reference		65		dB
		1 MSamples/s, 12 bit, differential, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V _{DD} reference		67		dB
		1 MSamples/s, 12 bit, differential, 2xV _{DD} reference		69		dB
		200 kSamples/s, 12 bit, single ended, internal 1.25V reference		62		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		63		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		67		dB
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differential, V _{DD} reference	63	66		dB
		200 kSamples/s, 12 bit, differential, 2xV _{DD} reference		70		dB
SINAD _{ADC}	Signal-to-Noise And Distortion-ratio (SINAD)	1 MSamples/s, 12 bit, single ended, internal 1.25V reference		58		dB
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		62		dB
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		64		dB
		1 MSamples/s, 12 bit, differential, internal 1.25V reference		60		dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		200 kSamples/s, 12 bit, differential, internal 1.25V reference		79		dBc
		200 kSamples/s, 12 bit, differential, internal 2.5V reference		79		dBc
		200 kSamples/s, 12 bit, differential, 5V reference		78		dBc
		200 kSamples/s, 12 bit, differential, V _{DD} reference	68	79		dBc
		200 kSamples/s, 12 bit, differential, 2xV _{DD} reference		79		dBc
V _{ADCOFFSET}	Offset voltage	After calibration, single ended	-3.5	0.3	3	mV
		After calibration, differential		0.3		mV
TGRAD _{ADCTH}	Thermometer output gradient			-1.92		mV/°C
				-6.3		ADC Codes/°C
DNL _{ADC}	Differential non-linearity (DNL)		-1	±0.7	4	LSB
INL _{ADC}	Integral non-linearity (INL), End point method			±1.2	±3	LSB
MC _{ADC}	No missing codes		11.999 ¹	12		bits
GAIN _{ED}	Gain error drift	1.25V reference		0.01 ²	0.033 ³	%/°C
		2.5V reference		0.01 ²	0.03 ³	%/°C
OFFSET _{ED}	Offset error drift	1.25V reference		0.2 ²	0.7 ³	LSB/°C
		2.5V reference		0.2 ²	0.62 ³	LSB/°C

¹On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

²Typical numbers given by $\text{abs}(\text{Mean}) / (85 - 25)$.

³Max number given by $(\text{abs}(\text{Mean}) + 3 \times \text{stddev}) / (85 - 25)$.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.24 (p. 36) and Figure 3.25 (p. 36) , respectively.

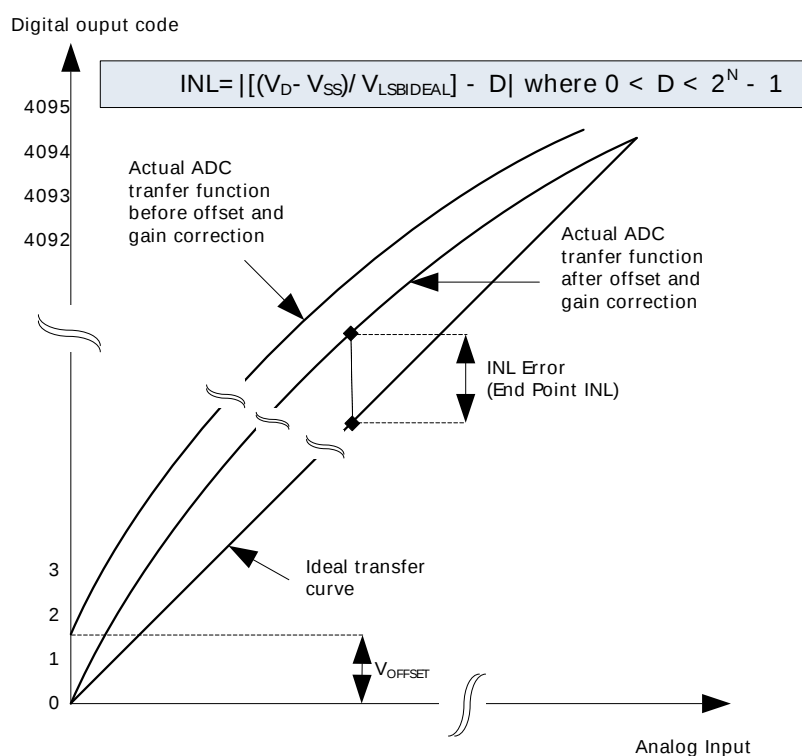
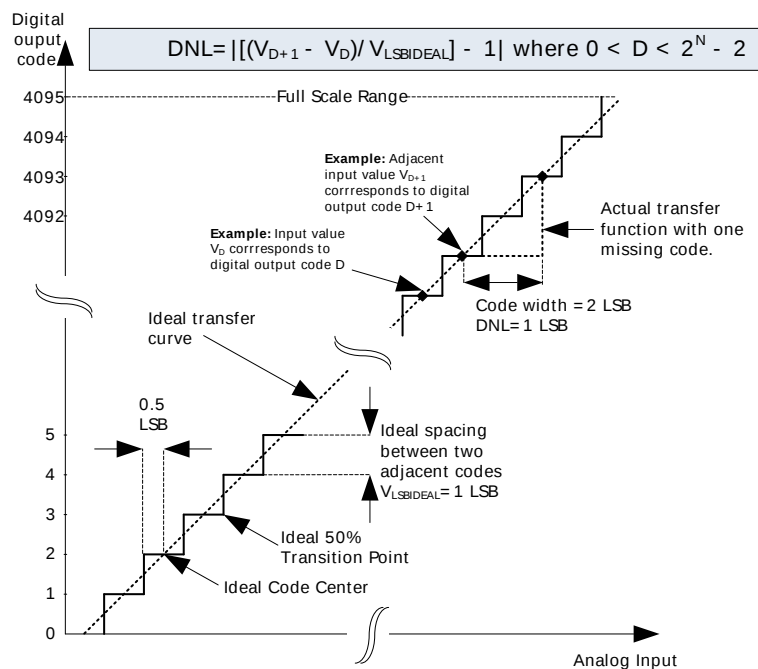
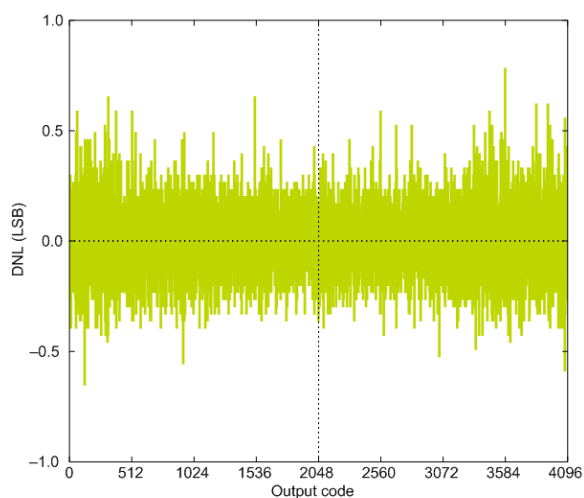
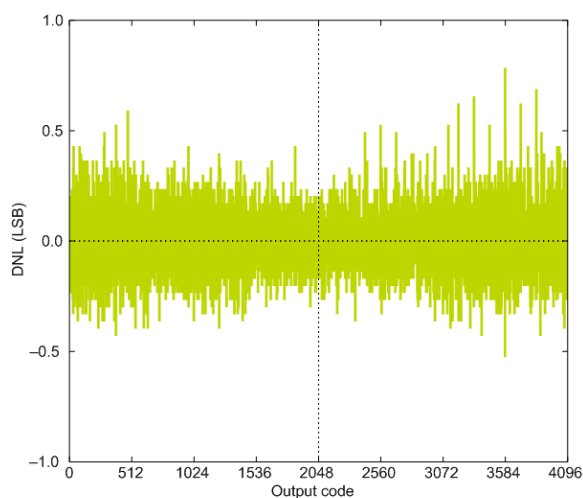
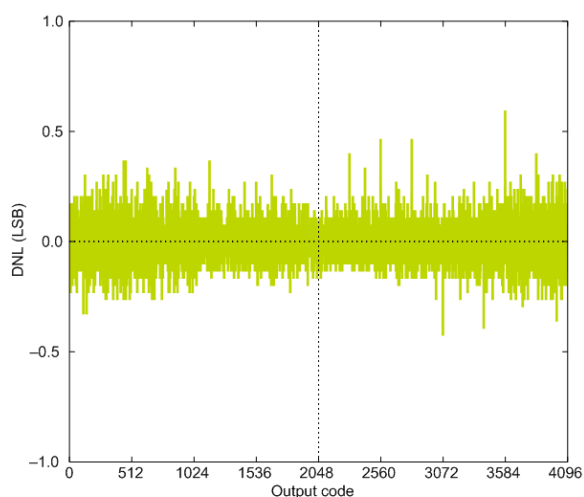
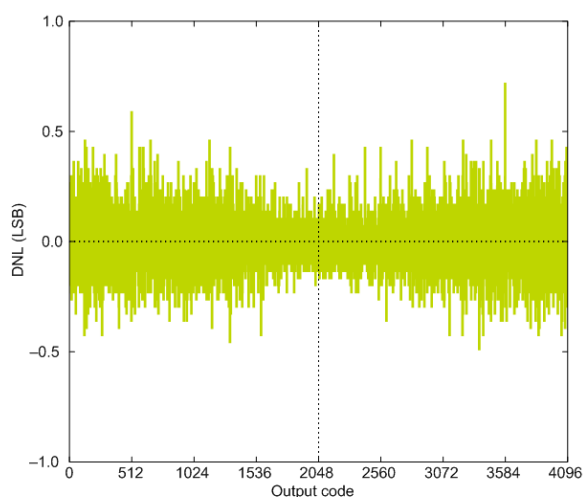
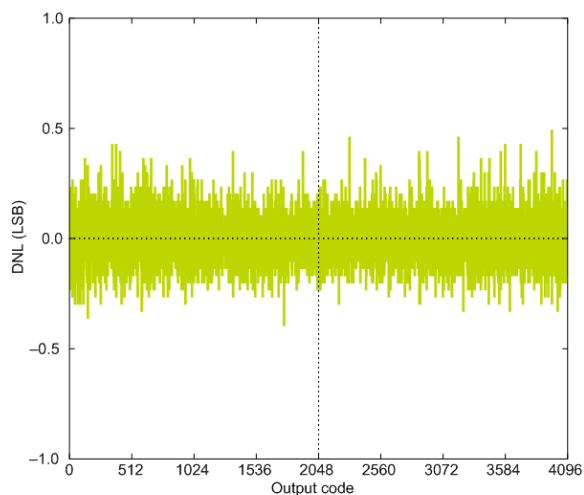
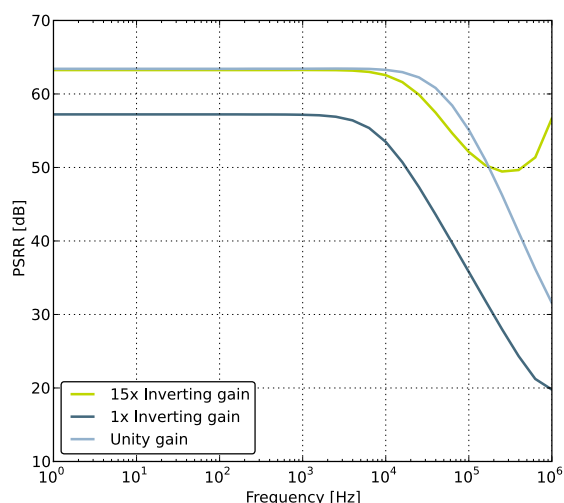
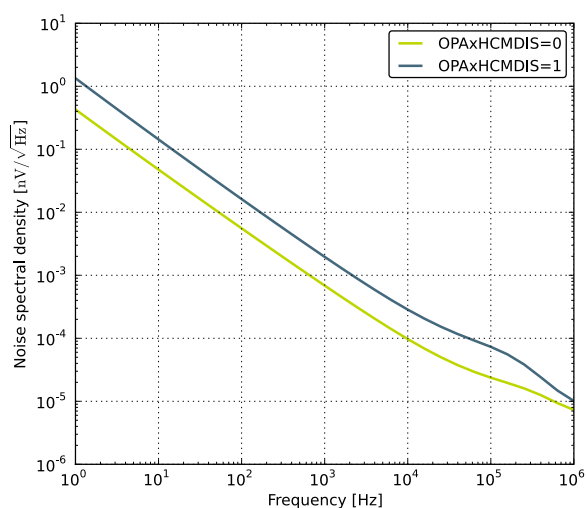
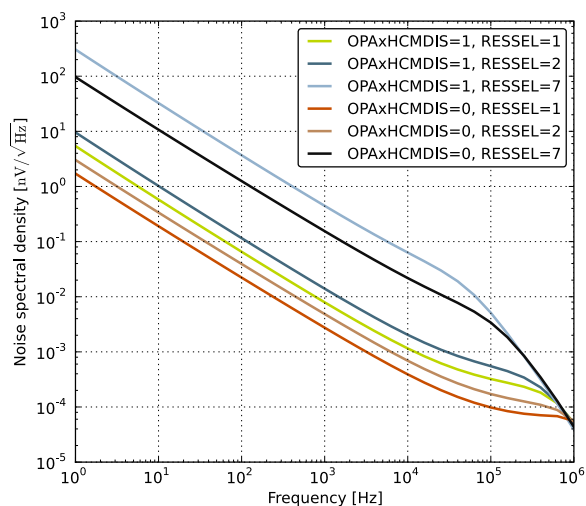
Figure 3.24. Integral Non-Linearity (INL)**Figure 3.25. Differential Non-Linearity (DNL)**

Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C**1.25V Reference****2.5V Reference****2XVDDVSS Reference****5VDIFF Reference****VDD Reference**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain		13	25	μA
G _{OL}	Open Loop Gain	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		101		dB
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		98		dB
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		91		dB
GBW _{OPAMP}	Gain Bandwidth Product	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		6.1		MHz
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		1.8		MHz
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.25		MHz
PM _{OPAMP}	Phase Margin	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, C _L =75 pF		64		°
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, C _L =75 pF		58		°
R _{INPUT}	Input Resistance			100		Mohm
R _{LOAD}	Load Resistance		200			Ohm
I _{LOAD_DC}	DC Load Current				11	mA
V _{INPUT}	Input Voltage	OPAxHCMDIS=0	V _{SS}		V _{DD}	V
		OPAxHCMDIS=1	V _{SS}		V _{DD} -1.2	V
V _{OUTPUT}	Output Voltage		V _{SS}		V _{DD}	V
V _{OFFSET}	Input Offset Voltage	Unity Gain, V _{SS} <V _{in} <V _{DD} , OPAxHCMDIS=0	-13	0	11	mV
		Unity Gain, V _{SS} <V _{in} <V _{DD} -1.2, OPAxHCMDIS=1		1		mV
V _{OFFSET_DRIFT}	Input Offset Voltage Drift				0.02	mV/°C
SR _{OPAMP}	Slew Rate	(OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0		3.2		V/μs
		(OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1		0.8		V/μs
		(OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1		0.1		V/μs
N _{OPAMP}	Voltage Noise	V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=0		101		μV _{RMS}
		V _{out} =1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAx- HCMDIS=1		141		μV _{RMS}

Figure 3.34. OPAMP Negative Power Supply Rejection Ratio**Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) $V_{out}=1V$** **Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)**

3.13 Analog Comparator (ACMP)

Table 3.18. ACMP

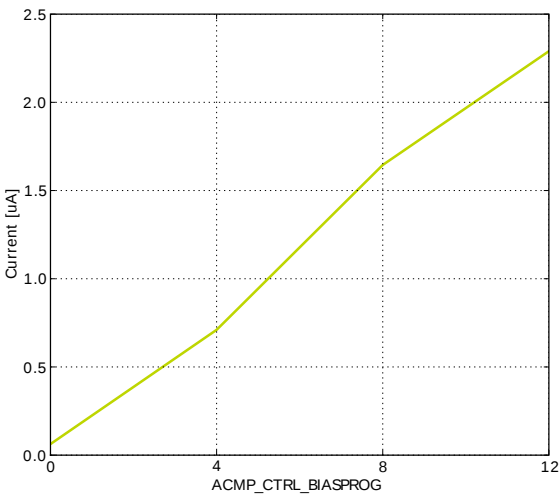
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ACMPIN}	Input voltage range		0		V_{DD}	V
V_{ACMPCM}	ACMP Common Mode voltage range		0		V_{DD}	V
I_{ACMP}	Active current	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register		0.1	0.4	μA
		BIASPROG=0b1111, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register		2.87	15	μA
		BIASPROG=0b1111, FULL-BIAS=1 and HALFBIAS=0 in ACMPn_CTRL register		195	520	μA
$I_{ACMPREF}$	Current consumption of internal voltage reference	Internal voltage reference off. Using external voltage reference		0		μA
		Internal voltage reference		5		μA
$V_{ACMPOFFSET}$	Offset voltage	BIASPROG= 0b1010, FULL-BIAS=0 and HALFBIAS=0 in ACMPn_CTRL register	-12	0	12	mV
$V_{ACMPHYST}$	ACMP hysteresis	Programmable		17		mV
R_{CSRES}	Capacitive Sense Internal Resistance	CSRESSEL=0b00 in ACMPn_INPUTSEL		39		kOhm
		CSRESSEL=0b01 in ACMPn_INPUTSEL		71		kOhm
		CSRESSEL=0b10 in ACMPn_INPUTSEL		104		kOhm
		CSRESSEL=0b11 in ACMPn_INPUTSEL		136		kOhm
$t_{ACMPSTART}$	Startup time				10	μs

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 46) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

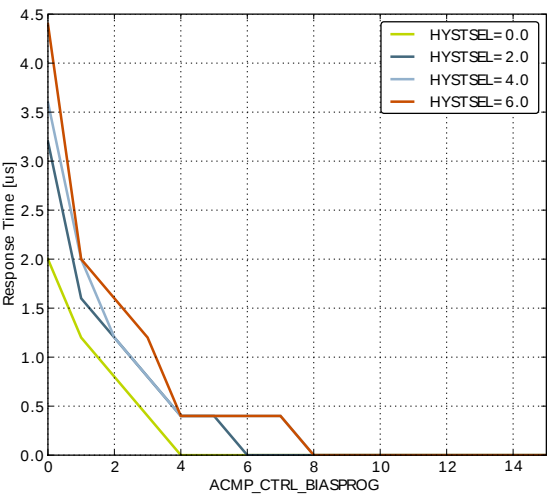
Total ACMP Active Current

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

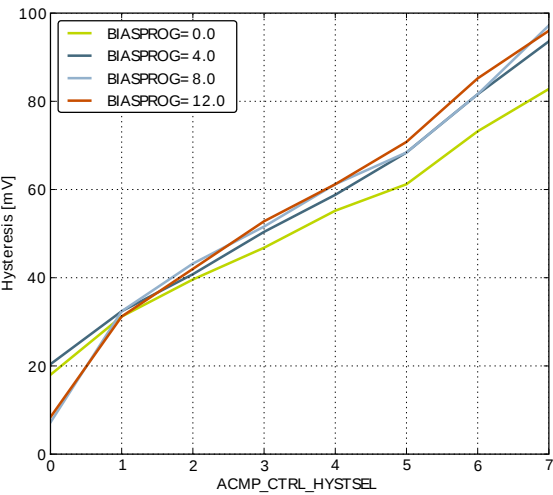
Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1



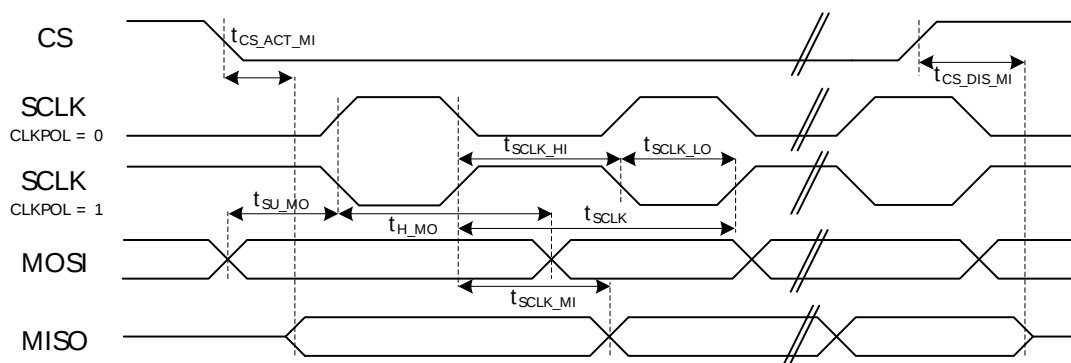
Current consumption, HYSTSEL = 4



Response time



Hysteresis

Figure 3.39. SPI Slave Timing**Table 3.25. SPI Slave Timing**

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SCLK_sl}^{1\ 2}$	SCKL period	$6 * t_{HFPER-CLK}$			ns
$t_{SCLK_hi}^{1\ 2}$	SCLK high period	$3 * t_{HFPER-CLK}$			ns
$t_{SCLK_lo}^{1\ 2}$	SCLK low period	$3 * t_{HFPER-CLK}$			ns
$t_{CS_ACT_MI}^{1\ 2}$	CS active to MISO	5.00		35.00	ns
$t_{CS_DIS_MI}^{1\ 2}$	CS disable to MISO	5.00		35.00	ns
$t_{SU_MO}^{1\ 2}$	MOSI setup time	5.00			ns
$t_{H_MO}^{1\ 2}$	MOSI hold time	$2 + 2 * t_{HF-CLK}$			ns
$t_{SCLK_MI}^{1\ 2}$	SCLK to MISO	$7 + t_{HFPER-CLK}$		$42 + 2 * t_{HFPERCLK}$	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

²Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 3.26. SPI Slave Timing with SSSEARLY and SMSDELAY

Symbol	Parameter	Min	Typ	Max	Unit
$t_{SCLK_sl}^{12}$	SCKL period	$6 * t_{HFPER-CLK}$			ns
$t_{SCLK_hi}^{12}$	SCLK high period	$3 * t_{HFPER-CLK}$			ns
$t_{SCLK_lo}^{12}$	SCLK low period	$3 * t_{HFPER-CLK}$			ns
$t_{CS_ACT_MI}^{12}$	CS active to MISO	5.00		35.00	ns
$t_{CS_DIS_MI}^{12}$	CS disable to MISO	5.00		35.00	ns
$t_{SU_MO}^{12}$	MOSI setup time	5.00			ns
$t_{H_MO}^{12}$	MOSI hold time	$2 + 2 * t_{HF-CLK}$			ns

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
					ETM_TD0 #3
4	PA3		TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground			
9	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
10	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
11	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
12	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
13	PC4	ACMP0_CH4 DAC0_P0 / OPAMP_P0	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 DAC0_N0 / OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
22	VSS	Ground			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX
BOOT_TX	PE10							Bootloader TX
BU_VIN	PD8							Battery input for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
DAC0_N0 / OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
DAC0_N1 / OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
DAC0_P0 / OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
DAC0_P1 / OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6					Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5							I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exit output 0.
LES_ALTEX1	PD7							LESENSE alternate exit output 1.
LES_ALTEX2	PA3							LESENSE alternate exit output 2.
LES_ALTEX3	PA4							LESENSE alternate exit output 3.
LES_ALTEX4	PA5							LESENSE alternate exit output 4.
LES_ALTEX5	PE11							LESENSE alternate exit output 5.
LES_ALTEX6	PE12							LESENSE alternate exit output 6.
LES_ALTEX7	PE13							LESENSE alternate exit output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7		PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.

List of Equations

3.1. Total ACMP Active Current 46

3.2. VCMP Trigger Level as a Function of Level Setting 48