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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	33MHz
Connectivity	I²C, IrDA, SCI, SmartCard, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b SAR; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d12363vte33v

- In order to understand the details of the CPU's functions

  Read the H8S/2600 Series, H8S/2000 Series Software Manual.
  For the execution state of each instruction in this LSI, see appendix D, Bus State during Execution of Instructions.
- In order to understand the details of a register when its name is known

  Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 24, List of Registers.

Examples:		
	Register name:	The following notation is used for cases when the same or a similar function, e.g. 16-bit timer pulse unit or serial communication, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB is on the left and the LSB is on the right.
	Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx
	Signal notation:	An overbar is added to a low-active signal: $\overline{\text{xxxx}}$

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require. http://www.renesas.com/

H8S/2368 Group Manuals:

Document Title	Document No.
H8S/2368 Group Hardware Manual	This manual
H8S/2600 Series, H8S/2000 Series Software Manual	REJ09B0139

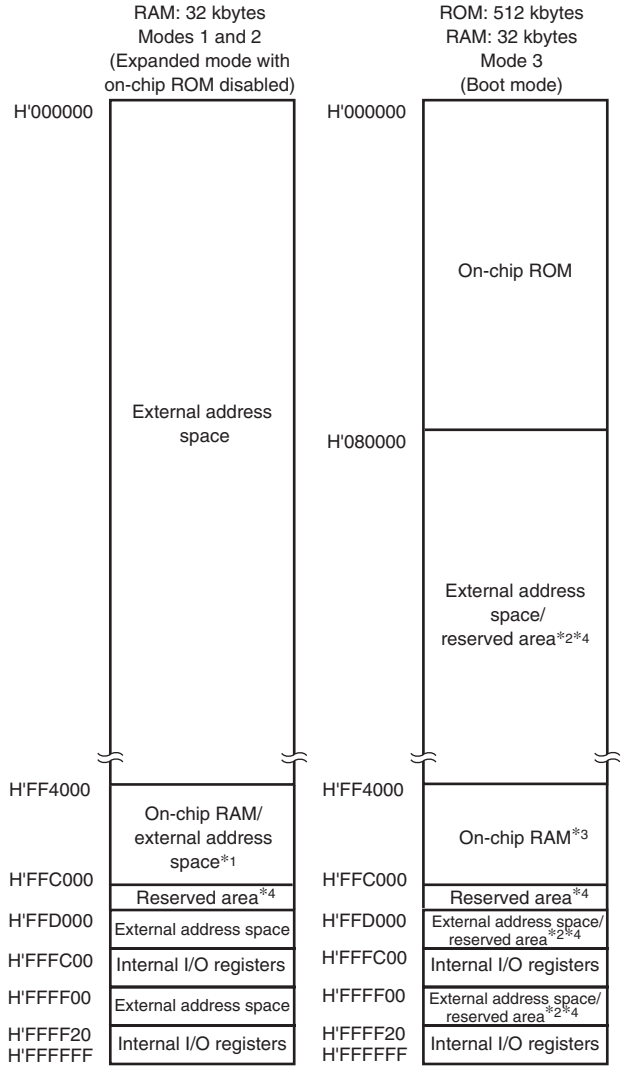
User's Manuals for Development Tools:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.6.01 User's Manual	REJ10B0161
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B0211
H8S, H8/300 Series High-performance Embedded Workshop, V.3 Tutorial	REJ10B0024
High-performance Embedded Workshop V.4.04 User's Manual	REJ10J1737

Type	Symbol	Pin No. TFP-120	Pin No. QFP-128*1	I/O	Function
Bus control	$\overline{\text{BACK}}$	107	117	Output	Indicates the bus is released to the external bus master.
	$\overline{\text{UCAS}}$	70	78	Output	Upper column address strobe signal for accessing the 16-bit DRAM space. Column address strobe signal for accessing the 8-bit DRAM space.
	$\overline{\text{LCAS}}$	71	79	Output	Lower column address strobe signal for accessing the 16-bit DRAM space.
	$\overline{\text{RAS2}}$ $\overline{\text{RAS3}}$	91 92	101 102	Output	Row address strobe signal for the DRAM interface.
	$\overline{\text{WAIT}}$	69	77	Input	Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.
	$\overline{\text{OE}}$ ($\overline{\text{OE}}$)	69, 113	77, 123	Output	Output enable signal for accessing the DRAM space. The output pins of $\overline{\text{OE}}$ and ($\overline{\text{OE}}$) are selected by the port function control register 2 (PFCR2) of port 3.
Interrupt signals	NMI	32	38	Input	Nonmaskable interrupt request pin. Fix high when not used.
	$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ ($\overline{\text{IRQ7}}$) to ($\overline{\text{IRQ0}}$)	29 to 26, 112 to 109, 102 to 95	33 to 30, 122 to 119, 112 to 105	Input	These pins request a maskable interrupt. The input pins of $\overline{\text{IRQn}}$ and ($\overline{\text{IRQn}}$) are selected by the IRQ pin select register (ITSR) of the interrupt controller. (n = 0 to 7)
DMA controller (DMAC)	$\overline{\text{DREQ1}}$ $\overline{\text{DREQ0}}$	35, 34	41, 40	Input	These signals request DMAC activation.
	$\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$	37, 36	43, 42	Output	These signals indicate the end of DMAC data transfer.
	$\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$	39, 38	45, 44	Output	DMAC single address transfer acknowledge signals.

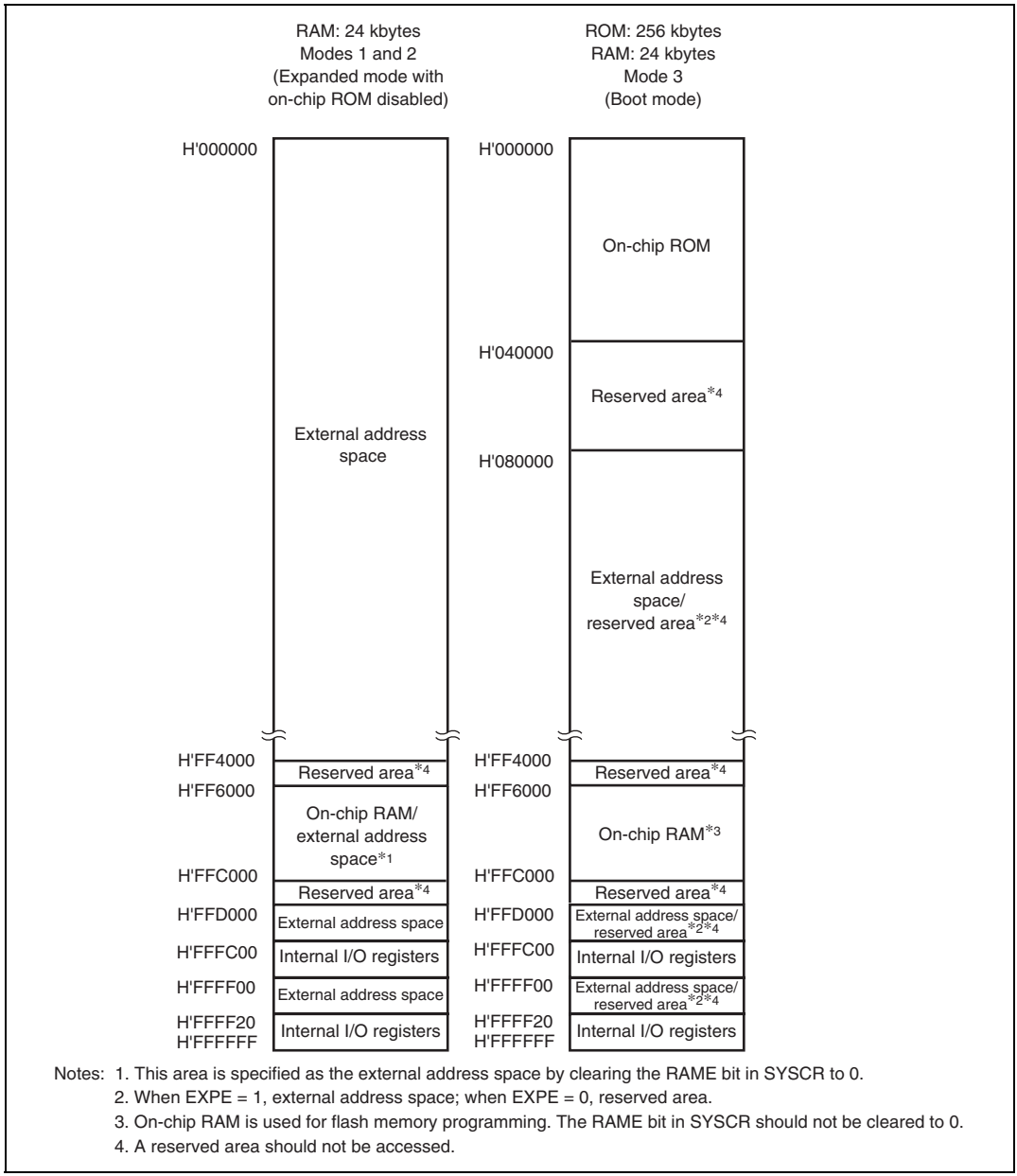
3.4 Memory Map in Each Operating Mode

Figures 3.1 to 3.15 show memory maps for each product.



Notes: 1. This area is specified as the external address space by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. On-chip RAM is used for flash memory programming. The RAME bit in SYSCR should not be cleared to 0.
4. A reserved area should not be accessed.

Figure 3.1 H8S/2368F Memory Map (1)



Notes: 1. This area is specified as the external address space by clearing the RAME bit in SYSCR to 0.
2. When EXPE = 1, external address space; when EXPE = 0, reserved area.
3. On-chip RAM is used for flash memory programming. The RAME bit in SYSCR should not be cleared to 0.
4. A reserved area should not be accessed.

Figure 3.9 H8S/2361F Memory Map (1)

- Refresh control register (REFCR)
- Refresh timer counter (RTCNT)
- Refresh time constant register (RTCOR)

6.3.1 Bus Width Control Register (ABWCR)

ABWCR designates each area in the external address space as either 8-bit access space or 16-bit access space.

Bit	Bit Name	Initial Value*	R/W	Description
7	ABW7	1/0	R/W	Area 7 to 0 Bus Width Control
6	ABW6	1/0	R/W	These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space.
5	ABW5	1/0	R/W	
4	ABW4	1/0	R/W	
3	ABW3	1/0	R/W	0: Area n is designated as 16-bit access space
2	ABW2	1/0	R/W	
1	ABW1	1/0	R/W	1: Area n is designated as 8-bit access space
0	ABW0	1/0	R/W	(n = 7 to 0)

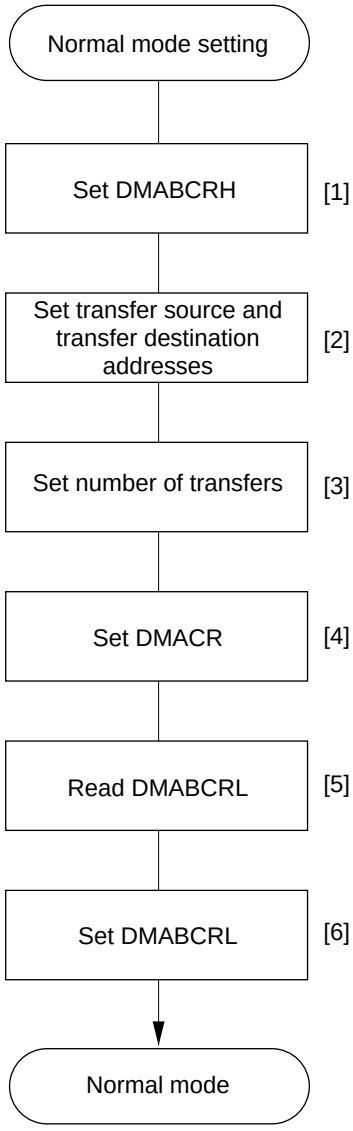
Note: * In modes 2 and 4, ABWCR is initialized to 1. In modes 1 and 7, ABWCR is initialized to 0.

6.3.2 Access State Control Register (ASTCR)

ASTCR designates each area in the external address space as either 2-state access space or 3-state access space.

Bit	Bit Name	Initial Value	R/W	Description
7	AST7	1	R/W	Area 7 to 0 Access State Control
6	AST6	1	R/W	These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space. Wait state insertion is enabled or disabled at the same time.
5	AST5	1	R/W	
4	AST4	1	R/W	
3	AST3	1	R/W	
2	AST2	1	R/W	
1	AST1	1	R/W	
0	AST0	1	R/W	0: Area n is designated as 2-state access space Wait state insertion in area n access is disabled 1: Area n is designated as 3-state access space Wait state insertion in area n access is enabled (n = 7 to 0)

Bit	Bit Name	Initial Value	R/W	Description
3	DTF3	0	R/W	• Channel B
2	DTF2	0	R/W	0000: Setting prohibited
1	DTF1	0	R/W	0001: Activated by A/D converter conversion end interrupt
0	DTF0	0	R/W	0010: Activated by $\overline{\text{DREQ}}$ pin falling edge input (detected as a low level in the first transfer after transfer is enabled)
				0011: Activated by $\overline{\text{DREQ}}$ pin low-level input
				0100: Activated by SCI channel 0 transmission complete interrupt
				0101: Activated by SCI channel 0 reception complete interrupt
				0110: Activated by SCI channel 1 transmission complete interrupt
				0111: Activated by SCI channel 1 reception complete interrupt
				1000: Activated by TPU channel 0 compare match/input capture A interrupt
				1001: Activated by TPU channel 1 compare match/input capture A interrupt
				1010: Activated by TPU channel 2 compare match/input capture A interrupt
				1011: Activated by TPU channel 3 compare match/input capture A interrupt
				1100: Activated by TPU channel 4 compare match/input capture A interrupt
				1101: Activated by TPU channel 5 compare match/input capture A interrupt
				1110: Setting prohibited
				1111: Setting prohibited
				The same factor can be selected for more than one channel. In this case, activation starts with the highest-priority channel according to the relative channel priorities. For relative channel priorities, see section 7.5.12, Multi-Channel Operation.



[1] Set each bit in DMABCRH.
- Set the FAE bit to 1 to select full address mode.
- Specify enabling or disabling of internal interrupt clearing with the DTA bit.

[2] Set the transfer source address in MARA, and the transfer destination address in MARB.

[3] Set the number of transfers in ETCRA.

[4] Set each bit in DMACRA and DMACRB.
- Set the transfer data size with the DTSZ bit.
- Specify whether MARA is to be incremented, decremented, or fixed, with the SAID and SAIDE bits.
- Clear the BLKE bit to 0 to select normal mode.
- Specify whether MARB is to be incremented, decremented, or fixed, with the DAID and DAIDE bits.
- Select the activation source with bits DTF3 to DTF0.

[5] Read DTE = 0 and DTME = 0 in DMABCRL.

[6] Set each bit in DMABCRL.
- Specify enabling or disabling of transfer end interrupts with the DTIE bit.
- Set both the DTME bit and the DTE bit to 1 to enable transfer.

Figure 7.12 Example of Normal Mode Setting Procedure

9.7 Port 9

Port 9 is a 2-bit input-only port. Port 9 has the following register.

- Port 9 register (PORT9)

9.7.1 Port 9 Register (PORT9)

PORT9 is an 8-bit read-only register that shows port 4 pin states.

PORT9 cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	Undefined	R	Reserved If read they will return an undefined value.
5	P95	—*	R	The pin states are always read when a port 9 read is performed.
4	P94	—*	R	
3	—	Undefined	R	Reserved If read they will return an undefined value.
2	—	Undefined	R	
1	—	Undefined	R	
0	—	Undefined	R	

Note: * Determined by the states of pins P95 and P94.

9.7.2 Pin Functions

Port 9 also functions as the pins for A/D converter analog input and D/A converter analog output. The correspondence between pins are as follows.

P95/AN13/DA3

Pin function	AN13 input
	DA3 output

P94/AN12/DA2

Pin function	AN12 input
	DA2 output

9.11.4 Port D Pull-up Control Register (PDPCR)

PDPCR controls on/off states of the input pull-up MOS of port D. PDPCR is valid in mode 7.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7PCR	0	R/W	When PDDDR = 0 (input port), the input pull-up MOS of the input pin is on when the corresponding bit is set to 1.
6	PD6PCR	0	R/W	
5	PD5PCR	0	R/W	
4	PD4PCR	0	R/W	
3	PD3PCR	0	R/W	
2	PD2PCR	0	R/W	
1	PD1PCR	0	R/W	
0	PD0PCR	0	R/W	

9.11.5 Pin Functions

Port D pins also function as the pins for data I/Os. The correspondence between the register specification and the pin functions is shown below.

- PD7/D15, PD6/D14, PD5/D13, PD4/D12, PD3/D11, PD2/D10, PD1/D9, PD0/D8

The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PDDDR.

Operating mode	1, 2, 4	7		
EXPE	—	0		1
PDnDDR	—	0	1	—
Pin function	Data I/O	PDn input	PDn output	Data I/O

Legend: n = 7 to 0

9.11.6 Port D MOS Input Pull-Up States

Port D has a built-in MOS input pull-up function that can be controlled by software. This MOS input pull-up function can be used in mode 7. MOS input pull-up can be specified as on or off on a bit-by-bit basis.

In mode 7, when a PDDDR bit is cleared to 0, setting the corresponding PDPCR bit to 1 turns on the MOS input pull-up for that pin.

Table 9.5 summarizes the MOS input pull-up states.

Table 9.5 MOS Input Pull-Up States (Port D)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2, 4	Off	Off	Off	Off
7			On/Off	On/Off

Legend:

OFF: MOS input pull-up is always off.

On/Off: On when PDDDR = 0 and PDPCR = 1; otherwise off.

2. When TGR is an input capture register

   Figure 10.16 shows an operation example in which TGRA has been designated as an input capture register, and buffer operation has been designated for TGRA and TGRC.

   Counter clearing by TGRA input capture has been set for TCNT, and both rising and falling edges have been selected as the TIOCA pin input capture input edge.

   As buffer operation has been set, when the TCNT value is stored in TGRA upon occurrence of input capture A, the value previously stored in TGRA is simultaneously transferred to TGRC.

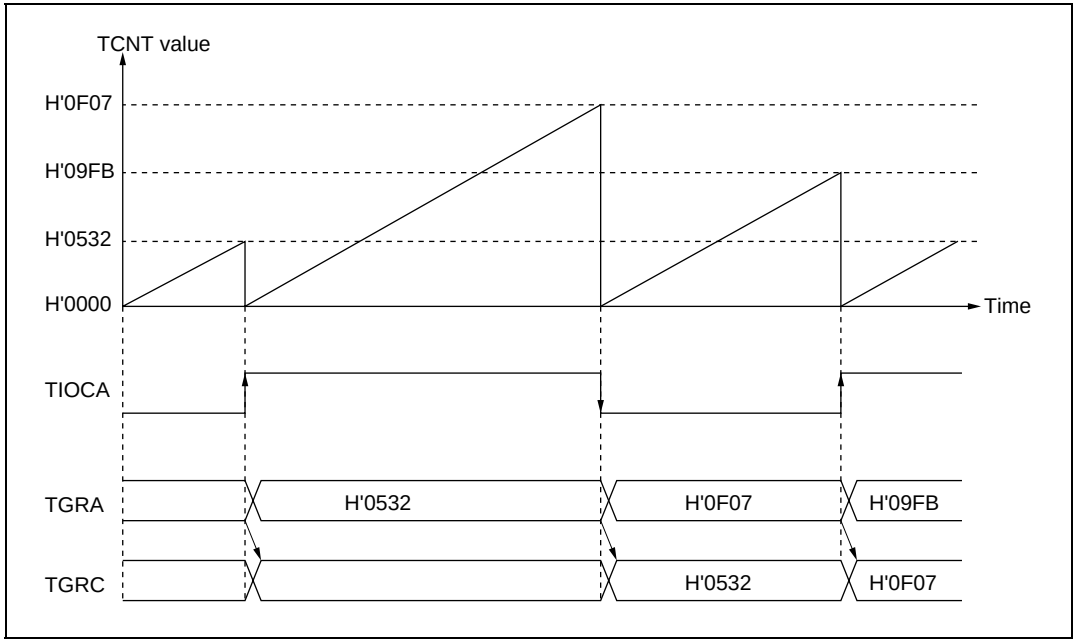
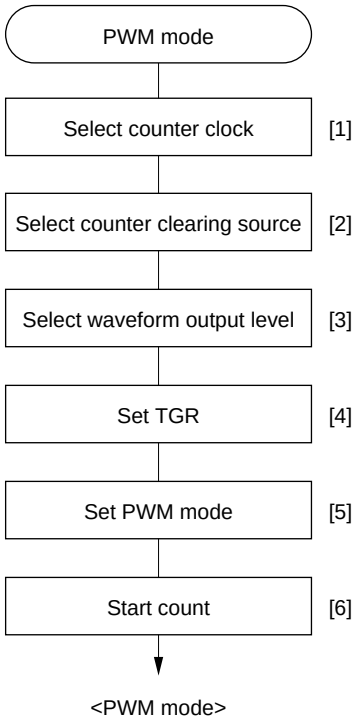


Figure 10.16 Example of Buffer Operation (2)

Example of PWM Mode Setting Procedure: Figure 10.20 shows an example of the PWM mode setting procedure.



[1] Select the counter clock with bits TPSC2 to TPSC0 in TCR. At the same time, select the input clock edge with bits CKEG1 and CKEG0 in TCR.

[2] Use bits CCLR2 to CCLR0 in TCR to select the TGR to be used as the TCNT clearing source.

[3] Use TIOR to designate the TGR as an output compare register, and select the initial value and output value.

[4] Set the cycle in the TGR selected in [2], and set the duty in the other TGRs.

[5] Select the PWM mode with bits MD3 to MD0 in TMDR.

[6] Set the CST bit in TSTR to 1 to start the count operation.

Figure 10.20 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 10.21 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the cycle, and the values set in TGRB registers as the duty.

2. Phase counting mode 2

Figure 10.26 shows an example of phase counting mode 2 operation, and table 10.33 summarizes the TCNT up/down-count conditions.

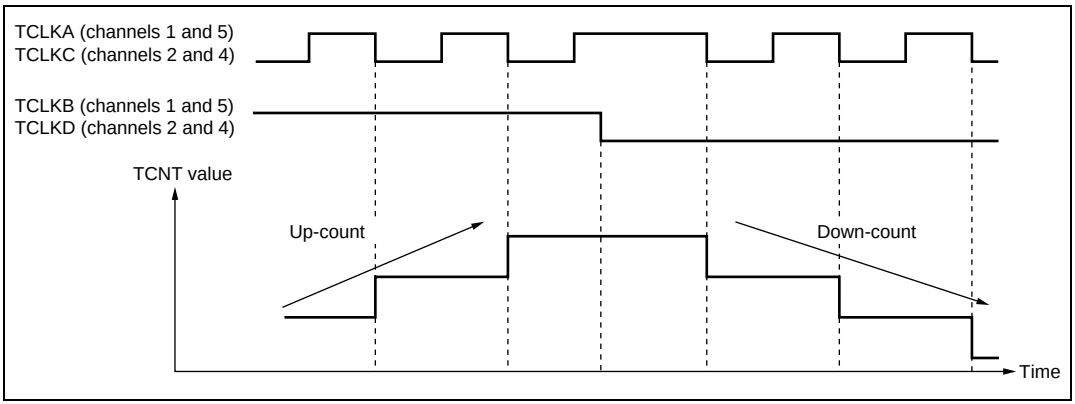


Figure 10.26 Example of Phase Counting Mode 2 Operation

Table 10.33 Up/Down-Count Conditions in Phase Counting Mode 2

TCLKA (Channels 1 and 5) TCLKC (Channels 2 and 4)	TCLKB (Channels 1 and 5) TCLKD (Channels 2 and 4)	Operation
High level	⌐↓	Don't care
Low level	↓¬	Don't care
⌐↓	Low level	Don't care
↓¬	High level	Up-count
High level	↓¬	Don't care
Low level	⌐↓	Don't care
⌐↓	High level	Don't care
↓¬	Low level	Down-count

Legend:

⌐↓ : Rising edge

↓¬ : Falling edge

Status Flag Clearing Timing: After a status flag is read as 1 by the CPU, it is cleared by writing 0 to it. When the DTC or DMAC is activated, the flag is cleared automatically. Figure 10.42 shows the timing for status flag clearing by the CPU, and figure 10.43 shows the timing for status flag clearing by the DTC or DMAC.

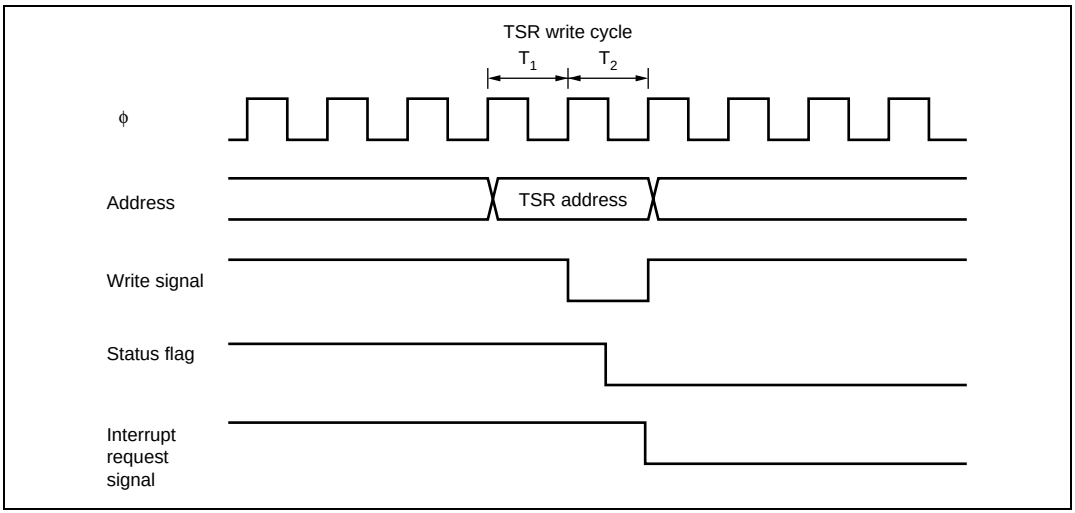


Figure 10.42 Timing for Status Flag Clearing by CPU

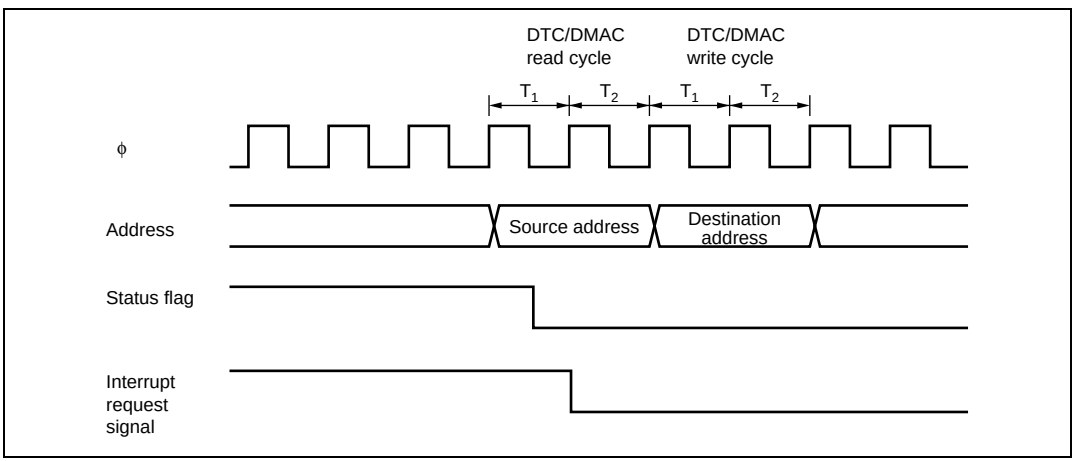


Figure 10.43 Timing for Status Flag Clearing by DTC/DMAC* Activation

If the DTC or DMAC is set for activation by the TGIA interrupt, pulse output can be obtained without imposing a load on the CPU.

11.4.4 Non-Overlapping Pulse Output

During non-overlapping operation, transfer from NDR to PODR is performed as follows:

- NDR bits are always transferred to PODR bits at compare match A.
- At compare match B, NDR bits are transferred only if their value is 0. Bits are not transferred if their value is 1.

Figure 11.6 illustrates the non-overlapping pulse output operation.

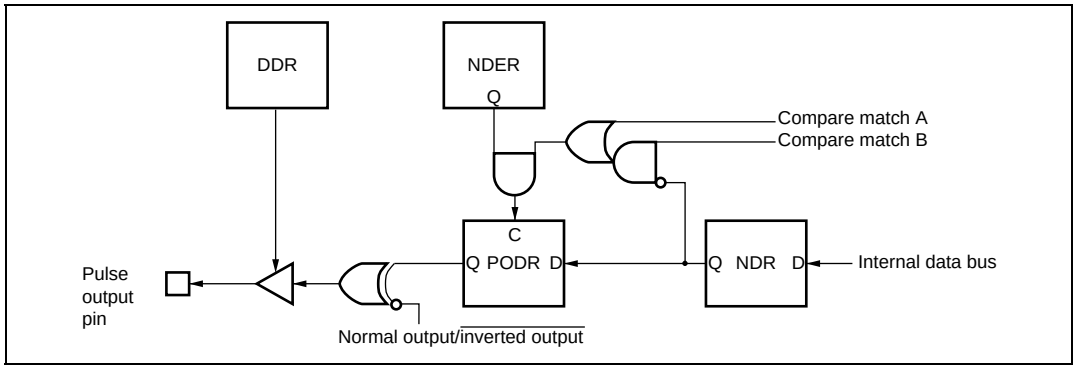


Figure 11.6 Non-Overlapping Pulse Output

Therefore, 0 data can be transferred ahead of 1 data by making compare match B occur before compare match A.

The NDR contents should not be altered during the interval from compare match B to compare match A (the non-overlap margin).

This can be accomplished by having the TGIA interrupt handling routine write the next data in NDR, or by having the TGIA interrupt activate the DTC or DMAC. Note, however, that the next data must be written before the next compare match B occurs.

Figure 11.7 shows the timing of this operation.

As in the above sample start character, with the direct convention type, the logic 1 level corresponds to state Z and the logic 0 level to state A, and transfer is performed in LSB-first order. The start character data above is H'3B. For the direct convention type, clear the SDIR and SINV bits in SCMR to 0. According to the Smart Card regulations, clear the O/$\overline{E}$ bit in SMR to 0 to select even parity mode.

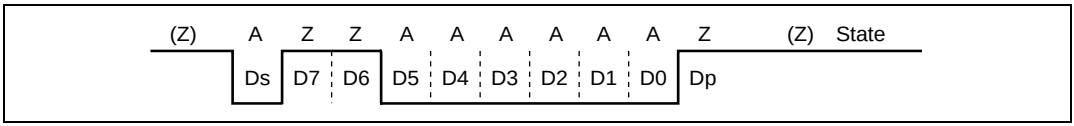


Figure 14.24 Inverse Convention (SDIR = SINV = O/$\overline{E}$ = 1)

With the inverse convention type, the logic 1 level corresponds to state A and the logic 0 level to state Z, and transfer is performed in MSB-first order. The start character data above is H'3F. For the inverse convention type, set the SDIR and SINV bits in SCMR to 1. According to the Smart Card regulations, even parity mode is the logic 0 level of the parity bit, and corresponds to state Z. In this LSI, the SINV bit inverts only data bits D7 to D0. Therefore, set the O/$\overline{E}$ bit in SMR to 1 to invert the parity bit for both transmission and reception.

14.7.3 Block Transfer Mode

Operation in block transfer mode is the same as that in normal Smart Card interface, except for the following points.

- In reception, though the parity check is performed, no error signal is output even if an error is detected. However, the PER bit in SSR is set to 1 and must be cleared before receiving the parity bit of the next frame.
- In transmission, a guard time of at least 1 etu is left between the end of the parity bit and the start of the next frame.
- In transmission, because retransmission is not performed, the TEND flag is set to 1, 11.5 etu after transmission start.
- As with the normal Smart Card interface, the ERS flag indicates the error signal status, but since error signal transfer is not performed, this flag is always cleared to 0.

  Note: etu: Elementary Time Unit (time for transfer of 1 bit)

14.7.4 Receive Data Sampling Timing and Reception Margin

Only the internal clock generated by the on-chip baud rate generator is used as transmit/receive clock in Smart Card interface. In Smart Card interface mode, the SCI operates on a basic clock with a frequency of 32, 64, 372, or 256 times the bit rate (fixed at 16 times in normal

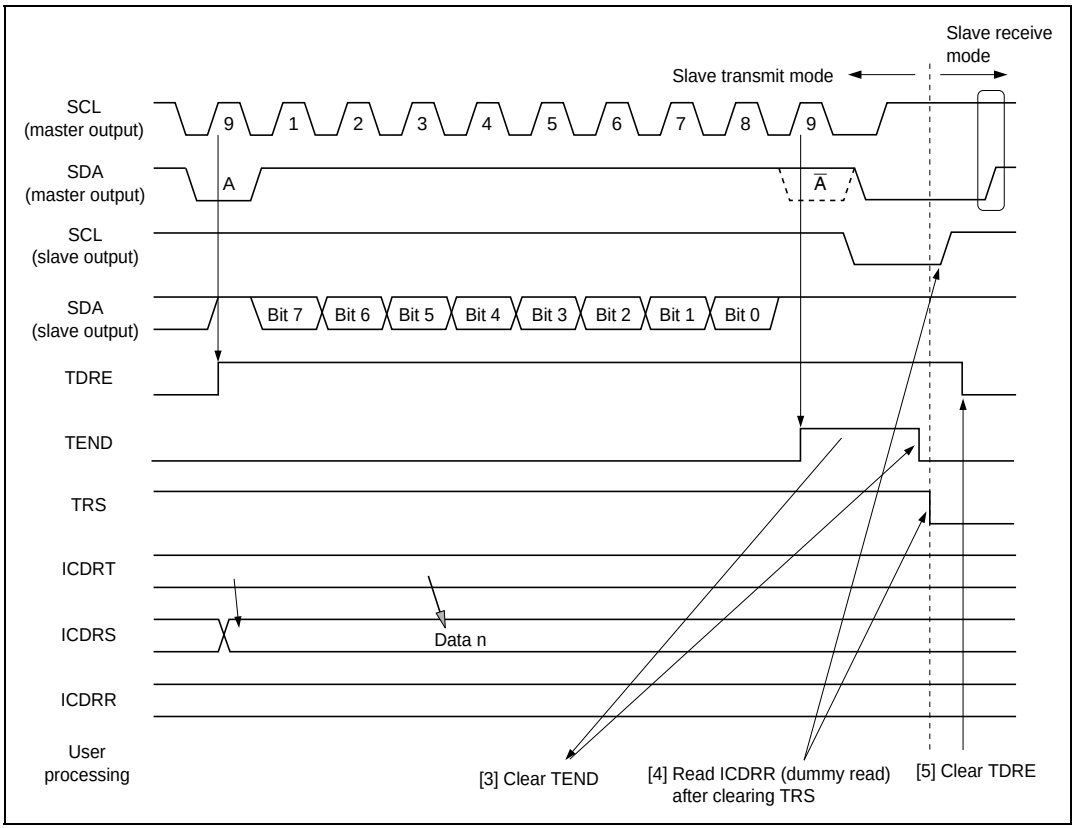


Figure 15.10 Slave Transmit Mode Operation Timing 2

15.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. For slave receive mode operation timing, refer to figures 15.11 and 15.12. The reception procedure and operations in slave receive mode are described below.

1. Set the ICE bit in ICCRA to 1. Set the MLS and WAIT bits in ICMR and the CKS3 to CKS0 bits in ICCRA to 1. (Initial setting) Set the MST and TRS bits in ICCRA to select slave receive mode, and wait until the slave address matches.
2. When the slave address matches in the first frame following detection of the start condition, the slave device outputs the level specified by ACKBT in ICIER to SDA, at the rise of the 9th clock pulse. At the same time, RDRF in ICSR is set to read ICDRR (dummy read) and RDRF is cleared. (Since the read data show the slave address and R/$\overline{W}$, it is not used.)

(k) New Bit-Rate Selection

The boot program will set a new bit rate and return the new bit rate.

This selection should be sent after sending the clock mode selection command.

Command

H'3F	Size	Bit rate	Input frequency
Number of multiplication ratios	Multiplication ratio 1	Multiplication ratio 2	
SUM			

- Command, H'3F, (one byte): Selection of new bit rate
- Size (one byte): The number of bytes that represents the bit rate, input frequency, number of multiplication ratios, and multiplication ratio
- Bit rate (two bytes): New bit rate
  One hundredth of the value (e.g. when the value is 19,200 bps, the bit rate is H'00C0, which is D'192.)
- Input frequency (two bytes): Frequency of the clock input to the boot program
  This is valid to the hundredths place and represents the value in MHz multiplied by 100. (e.g. when the value is 64 MHz, the input frequency is H'1900 (= D'6400).)
- Number of multiplication ratios (one byte): The number of multiplication ratios to which the device can be set.
- Multiplication ratio 1 (one byte): The value of multiplication or division ratios for the main operating frequency
  Multiplication ratio (one byte): The value of the multiplication ratio (e.g. when the clock frequency is multiplied by four, the multiplication ratio will be H'04.)
  Division ratio: The inverse of the division ratio, as a negative number (e.g. when the clock frequency is divided by two, the value of division ratio will be H'FE. H'FE = D'-2)
- Multiplication ratio 2 (one byte): The value of multiplication or division ratios for the peripheral frequency
  Multiplication ratio (one byte): The value of the multiplication ratio (e.g. when the clock frequency is multiplied by four, the multiplication ratio will be H'04.)
  (Division ratio: The inverse of the division ratio, as a negative number (E.g. when the clock is divided by two, the value of division ratio will be H'FE. H'FE = D'-2)
- SUM (one byte): Checksum

Response

H'06

- Response, H'06, (one byte): Response to selection of a new bit rate
  When it is possible to set the bit rate, the response will be ACK.

23.1.3 Extension Module Stop Control Registers H and L (EXMSTPCRH, EXMSTPCRL)

EXMSTPCR performs all-module-clocks-stop mode control with MSTPCR.

When entering all-module-clocks-stop mode, set EXMSTPCR to H'FFFF. Otherwise, set EXMSTPCR to H'FFFD.

- EXMSTPCRH

Bit	Bit Name	Initial Value	R/W	Module
15 to 12	—	All 1	R/W	Reserved Read/write is enabled. 1 should be written in writing.
11	MSTP27	1	R/W	—
10	MSTP26	1	R/W	—
9	MSTP25	1	R/W	—
8	MSTP24	1	R/W	—

- EXMSTPCRL

Bit	Bit Name	Initial Value	R/W	Module
7	MSTP23	1	R/W	—
6	MSTP22	1	R/W	—
5	MSTP21	1	R/W	—
4	MSTP20	1	R/W	I^2C bus interface 2_1 (IIC2_1)
3	MSTP19	1	R/W	I^2C bus interface 2_0 (IIC2_0)
2	MSTP18	1	R/W	—
1	MSTP17	0	R/W	—
0	MSTP16	1	R/W	—