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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

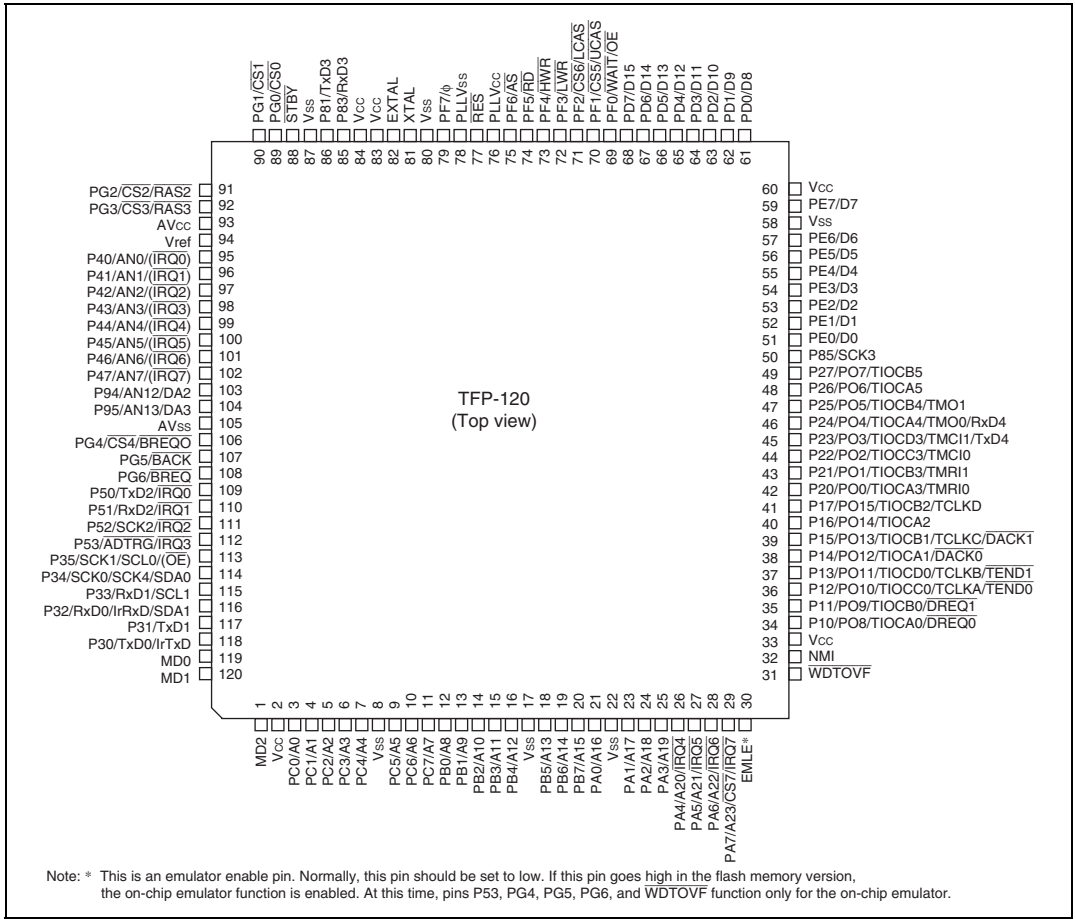
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2360vte34v

1.3 Pin Description

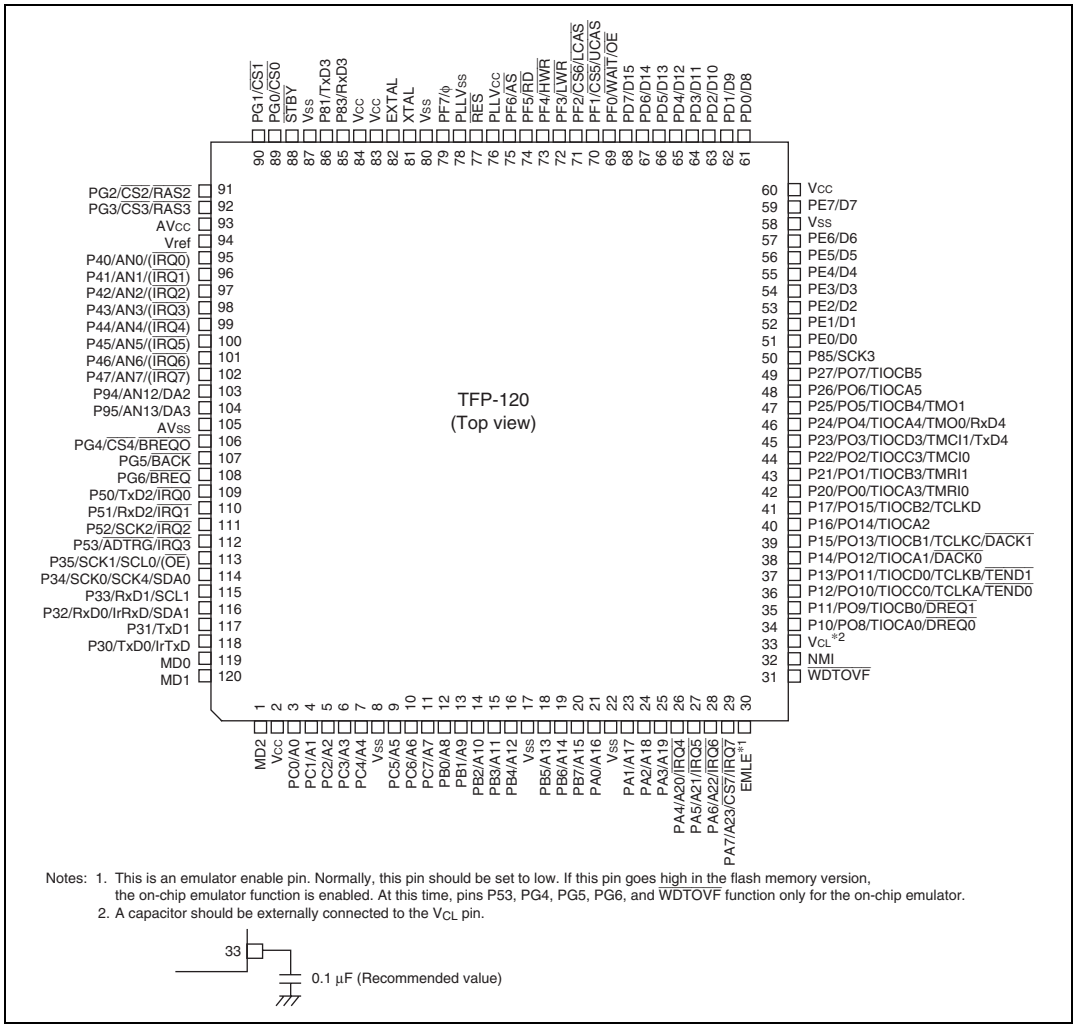
1.3.1 Pin Arrangement

Figures 1.3 to 1.5 show the pin arrangements of this LSI.



Note: * This is an emulator enable pin. Normally, this pin should be set to low. If this pin goes high in the flash memory version, the on-chip emulator function is enabled. At this time, pins P53, PG4, PG5, PG6, and WDTOVF function only for the on-chip emulator.

Figure 1.3 Pin Arrangement of H8S/2367F, H8S/2365, and H8S/2363



Notes: 1. This is an emulator enable pin. Normally, this pin should be set to low. If this pin goes high in the flash memory version, the on-chip emulator function is enabled. At this time, pins P53, PG4, PG5, PG6, and WDTOVF function only for the on-chip emulator.
2. A capacitor should be externally connected to the V_{CL} pin.

Figure 1.4 Pin Arrangement of H8S/2368 0.18 µm F-ZTAT Group

Type	Symbol	Pin No. TFP-120	Pin No. QFP-128*1	I/O	Function
Bus control	$\overline{\text{BACK}}$	107	117	Output	Indicates the bus is released to the external bus master.
	$\overline{\text{UCAS}}$	70	78	Output	Upper column address strobe signal for accessing the 16-bit DRAM space. Column address strobe signal for accessing the 8-bit DRAM space.
	$\overline{\text{LCAS}}$	71	79	Output	Lower column address strobe signal for accessing the 16-bit DRAM space.
	$\overline{\text{RAS2}}$ $\overline{\text{RAS3}}$	91 92	101 102	Output	Row address strobe signal for the DRAM interface.
	$\overline{\text{WAIT}}$	69	77	Input	Requests insertion of a wait state in the bus cycle when accessing external 3-state address space.
	$\overline{\text{OE}}$ ($\overline{\text{OE}}$)	69, 113	77, 123	Output	Output enable signal for accessing the DRAM space. The output pins of $\overline{\text{OE}}$ and ($\overline{\text{OE}}$) are selected by the port function control register 2 (PFCR2) of port 3.
Interrupt signals	NMI	32	38	Input	Nonmaskable interrupt request pin. Fix high when not used.
	$\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ ($\overline{\text{IRQ7}}$) to ($\overline{\text{IRQ0}}$)	29 to 26, 112 to 109, 102 to 95	33 to 30, 122 to 119, 112 to 105	Input	These pins request a maskable interrupt. The input pins of $\overline{\text{IRQn}}$ and ($\overline{\text{IRQn}}$) are selected by the IRQ pin select register (ITSR) of the interrupt controller. (n = 0 to 7)
DMA controller (DMAC)	$\overline{\text{DREQ1}}$ $\overline{\text{DREQ0}}$	35, 34	41, 40	Input	These signals request DMAC activation.
	$\overline{\text{TEND1}}$, $\overline{\text{TEND0}}$	37, 36	43, 42	Output	These signals indicate the end of DMAC data transfer.
	$\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$	39, 38	45, 44	Output	DMAC single address transfer acknowledge signals.

— 16 × 16-bit register-register multiply: 20 states (MULXU.W), 21 states (MULXS.W)
— 32 ÷ 16-bit register-register divide: 20 states (DIVXU.W)

- Two CPU operating modes
  — Normal mode*
  — Advanced mode

Note: * For this LSI, normal mode is not available.

- Power-down state
  — Transition to power-down state by SLEEP instruction
  — Selectable CPU clock speed

2.1.1 Differences between H8S/2600 CPU and H8S/2000 CPU

The differences between the H8S/2600 CPU and the H8S/2000 CPU are as shown below.

- Register configuration
  The MAC register is supported only by the H8S/2600 CPU.
- Basic instructions
  The four instructions MAC, CLRMAC, LDMAC, and STMAC are supported only by the H8S/2600 CPU.
- The number of execution states of the MULXU and MULXS instructions

		Execution States	
Instruction	**Mnemonic**	**H8S/2600**	**H8S/2000**
MULXU	MULXU.B Rs, Rd	3	12
	MULXU.W Rs, ERd	4	20
MULXS	MULXS.B Rs, Rd	4	13
	MULXS.W Rs, ERd	5	21

In addition, there are differences in address space, CCR and EXR register functions, power-down modes, etc., depending on the model.

4.7 Stack Status after Exception Handling

Figure 4.3 shows the stack after completion of trap instruction exception handling and interrupt exception handling.

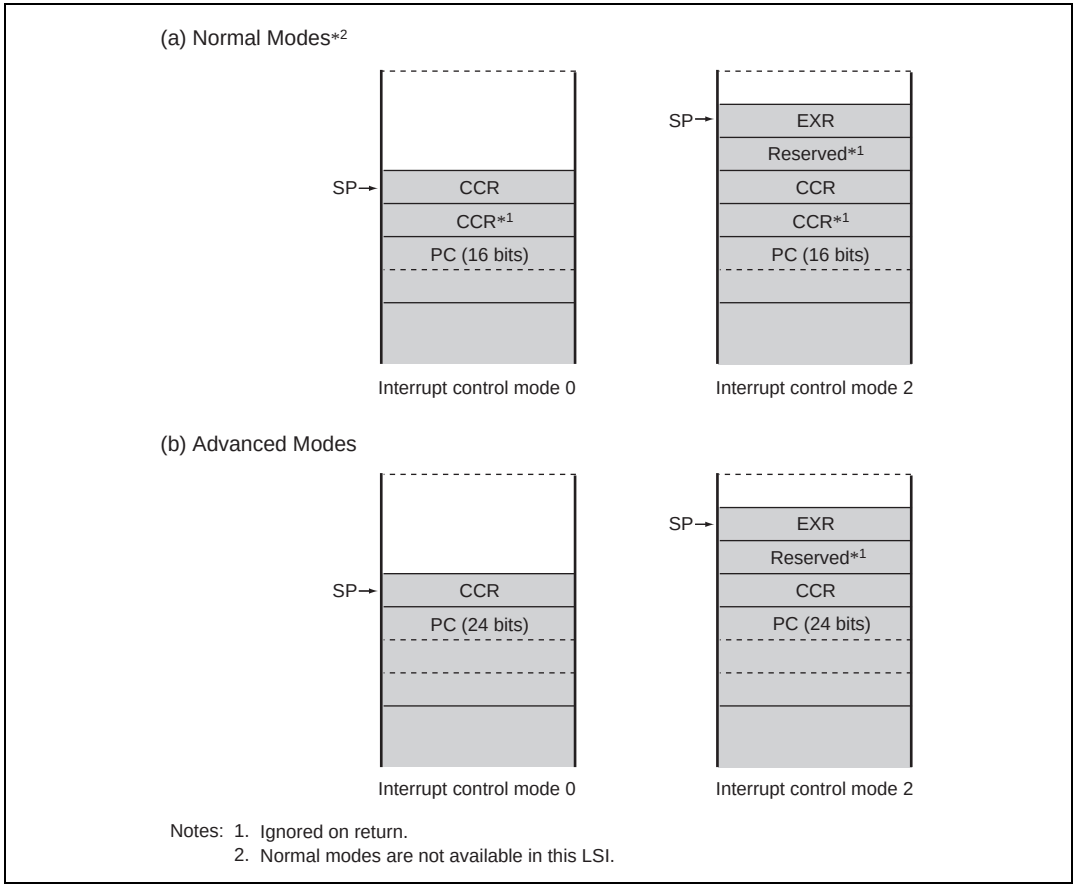


Figure 4.3 Stack Status after Exception Handling

- P22/PO2/TIOCC3/TMCI0

  The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR_3, bits IOC3 to IOC0 in TIORL_3, and bits CCLR2 to CCLR0 in TCR_3), bit NDER2 in NDERL, and bit P22DDR.

TPU channel 3 settings	(1) in table below	(2) in table below		
P22DDR	—	0	1	1
NDER2	—	—	0	1
Pin function	TIOCC3 output	P22 input	P22 output	PO2 output
		TIOCC3 input*1		
	TMCI0 input*2			

Notes: 1. TIOCC3 input when MD3 to MD0 = B'0000 and IOC3 to IOC0 = B'10××.

2. When used as the TMR external clock input pin, the external clock is selected by the CKS2 to CKS0 bits in TCR_1.

TPU channel 3 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000		B'001×	B'0010	B'0011	
IOC3 to IOC0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	B'××00	Other than B'××00	Other than B'××00	
CCLR2 to CCLR0	—	—	—	—	Other than B'101	B'101
Output function	—	Output compare output	—	PWM*3 mode 1 output	PWM mode 2 output	—

Legend:

×: Don't care

Note: 3. TIOCD3 output disabled.
Output disabled and settings (2) effective when BFA = 1 or BFB = 1 in TMDR_3.

9.11.2 Port D Data Register (PDDR)

PDDR stores output data for the port D pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7DR	0	R/W	Output data for a pin is stored when the pin function is specified to a general purpose I/O.
6	PD6DR	0	R/W	
5	PD5DR	0	R/W	
4	PD4DR	0	R/W	
3	PD3DR	0	R/W	
2	PD2DR	0	R/W	
1	PD1DR	0	R/W	
0	PD0DR	0	R/W	

9.11.3 Port D Register (PORTD)

PORTD shows port D pin states.

PORTD cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7	—*	R	If a port D read is performed while PDDDR bits are set to 1, the PDDR values are read. If a port D read is performed while PDDDR bits are cleared to 0, the pin states are read.
6	PD6	—*	R	
5	PD5	—*	R	
4	PD4	—*	R	
3	PD3	—*	R	
2	PD2	—*	R	
1	PD1	—*	R	
0	PD0	—*	R	

Note: * Determined by the states of pins PD7 to PD0.

9.14.2 Port G Data Register (PGDR)

PGDR stores output data for the port G pins.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0, and cannot be modified.
6	PG6DR	0	R/W	An output data for a pin is stored when the pin function is specified to a general purpose I/O.
5	PG5DR	0	R/W	
4	PG4DR	0	R/W	
3	PG3DR	0	R/W	
2	PG2DR	0	R/W	
1	PG1DR	0	R/W	
0	PG0DR	0	R/W	

9.14.3 Port G Register (PORTG)

PORTG shows port G pin states.

PORTG cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	—	Undefined	—	Reserved If this bit is read, it will return an undefined value.
6	PG6	—*	R	If a port G read is performed while PGDDR bits are set to 1, the PGDR values are read. If a port G read is performed while PGDDR bits are cleared to 0, the pin states are read.
5	PG5	—*	R	
4	PG4	—*	R	
3	PG3	—*	R	
2	PG2	—*	R	
1	PG1	—*	R	
0	PG0	—*	R	

Note: * Determined by the states of pins PG6 to PG0.

Bit	Bit Name	Initial Value	R/W	Description
1	G0CMS1	1	R/W	Group 0 Compare Match Select 1 and 0
0	G0CMS0	1	R/W	Select output trigger of pulse output group 0. 00: Compare match in TPU channel 0 01: Compare match in TPU channel 1 10: Compare match in TPU channel 2 11: Compare match in TPU channel 3

11.3.5 PPG Output Mode Register (PMR)

PMR selects the pulse output mode of the PPG for each group. If inverted output is selected, a low-level pulse is output when PODRH is 1 and a high-level pulse is output when PODRH is 0. If non-overlapping operation is selected, PPG updates its output values at compare match A or B of the TPU that becomes the output trigger. For details, refer to section 11.4.4, Non-Overlapping Pulse Output.

Bit	Bit Name	Initial Value	R/W	Description
7	G3INV	1	R/W	Group 3 Inversion Selects direct output or inverted output for pulse output group 3. 0: Inverted output 1: Direct output
6	G2INV	1	R/W	Group 2 Inversion Selects direct output or inverted output for pulse output group 2. 0: Inverted output 1: Direct output
5	G1INV	1	R/W	Group 1 Inversion Selects direct output or inverted output for pulse output group 1. 0: Inverted output 1: Direct output
4	G0INV	1	R/W	Group 0 Inversion Selects direct output or inverted output for pulse output group 0. 0: Inverted output 1: Direct output

12.5.3 Timing of Timer Output when Compare-Match Occurs

When compare match A or B occurs, the timer output changes as specified by bits OS3 to OS0 in TCSR.

Figure 12.6 shows the timing when the output is set to toggle at compare match A.

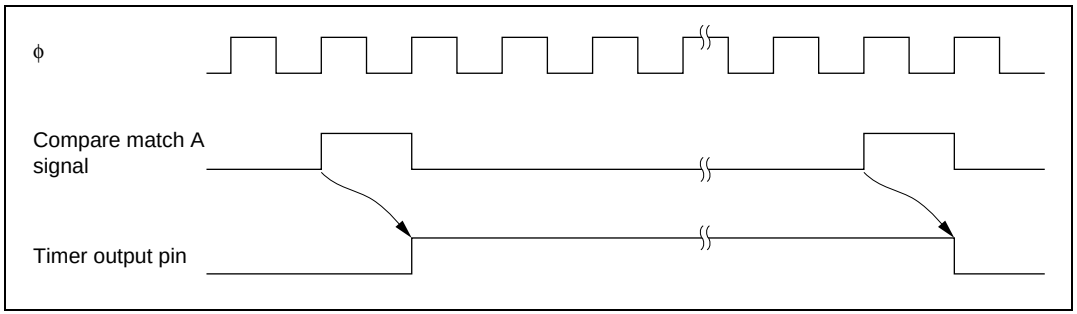


Figure 12.6 Timing of Timer Output

12.5.4 Timing of Compare Match Clear

TCNT is cleared when compare match A or B occurs, depending on the setting of the CCLR1 and CCLR0 bits in TCR. Figure 12.7 shows the timing of this operation.

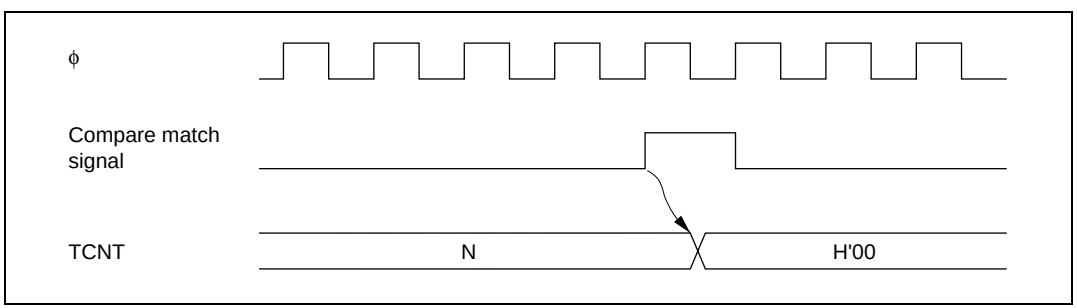


Figure 12.7 Timing of Compare Match Clear

14.8 IrDA Operation

When the IrDA function is enabled with bit IrE in IrCR, the SCI_0 TxD0 and RxD0 signals are subjected to waveform encoding/decoding conforming to IrDA specification version 1.0 (IrTxD and IrRxD pins). By connecting these pins to an infrared transceiver/receiver, it is possible to implement infrared transmission/reception conforming to the IrDA specification version 1.0 system.

In the IrDA specification version 1.0 system, communication is started at a transfer rate of 9600 bps, and subsequently the transfer rate can be varied as necessary. As the IrDA interface in this LSI does not include a function for varying the transfer rate automatically, the transfer rate setting must be changed by software.

Figure 14.33 shows a block diagram of the IrDA function.

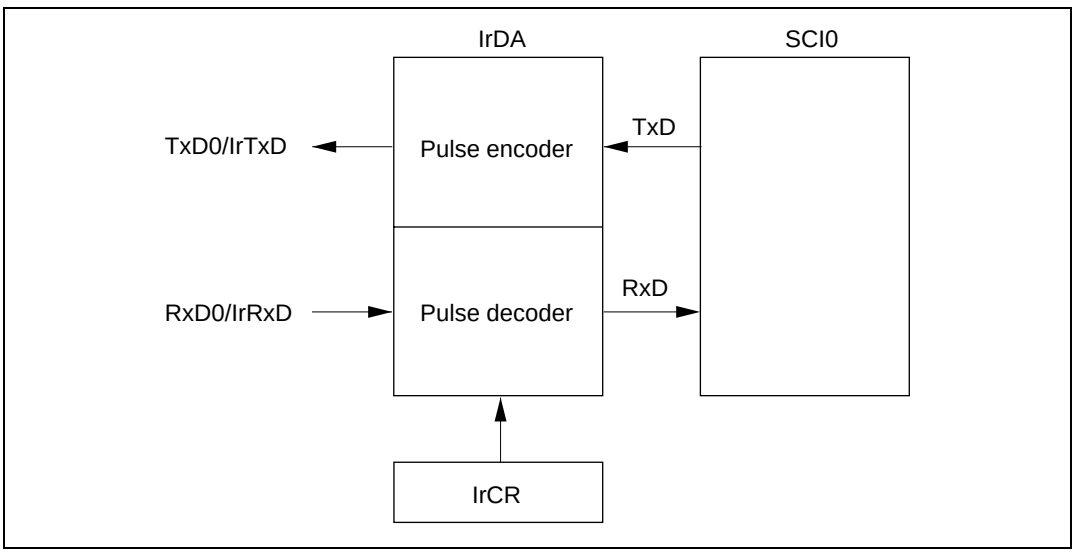


Figure 14.33 Block Diagram of IrDA

Transmission: In transmission, the output signal (UART frame) from the SCI is converted to an IR frame by the IrDA interface (see figure 14.34).

When the serial data is 0, a high pulse of 3/16 the bit rate (interval equivalent to the width of one bit) is output (initial value). The high-level pulse can be varied according to the setting of bits IrCKS2 to IrCKS0 in IrCR.

Bit	Bit Name	Initial Value	R/W	Description
2	BC2	0	R/W	Bit Counter 2 to 0
1	BC1	0	R/W	These bits specify the number of bits to be transferred next. When read, the remaining number of transfer bits is indicated. The data is transferred with one addition acknowledge bit. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL line is low. The value returns to 000 at the end of a data transfer, including the acknowledge bit. With the clock synchronous serial format, these bits should not be modified. 000: 9 001: 2 010: 3 011: 4 100: 5 101: 6 110: 7 111: 8
0	BC0	0	R/W	

15.3.4 I²C Bus Interrupt Enable Register (ICIER)

ICIER is an 8-bit readable/writable register that enables or disables interrupt sources and acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When the TDRE bit in ICSR is set to 1, this bit enables or disables the transmit data empty interrupt (TXI). 0: Transmit data empty interrupt request (TXI) is disabled. 1: Transmit data empty interrupt request (TXI) is enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disabled. 1: Transmit end interrupt request (TEI) is enabled.

16.3 Register Descriptions

The A/D converter has the following registers.

- A/D data register A (ADDRA)
- A/D data register B (ADDRB)
- A/D data register C (ADDRC)
- A/D data register D (ADDRD)
- A/D data register E (ADDRE)
- A/D data register F (ADDRF)
- A/D data register G (ADDRG)
- A/D data register H (ADDRH)
- A/D control/status register (ADCSR)
- A/D control register (ADCR)

16.3.1 A/D Data Registers A to H (ADDRA to ADDRH)

There are eight 16-bit read-only ADDR registers, ADDRA to ADDRH, used to store the results of A/D conversion. The ADDR registers, which store a conversion result for each channel, are shown in table 16.2.

The converted 10-bit data is stored to bits 15 to 6. The lower 6-bit data is always read as 0.

The data bus between the CPU and the A/D converter is 16-bit width. The data can be read directly from the CPU.

19.6 On-Board Programming Modes

In an on-board programming mode, programming, erasing, and verification for the on-chip flash memory can be performed. There are two on-board programming modes: boot mode and user program mode. Table 19.4 shows how to select boot mode. User program mode can be selected by setting the control bits by software. For a diagram that shows mode transitions of flash memory, see figure 19.2.

Table 19.4 Setting On-Board Programming Mode

	Mode Setting	MD2	MD1	MD0
Boot mode	Single-chip activation expanded mode with on-chip ROM enabled	0	1	1

19.6.1 Boot Mode

When this LSI enters boot mode, the embedded boot program is started. The boot program transfers the programming control program from the externally connected host to the on-chip RAM via the SCI_1. When the flash memory is all erased, the programming control program is executed.

Table 19.5 shows the boot mode operations between reset end and branching to the programming control program.

1. When the boot program is initiated, the SCI_1 should be set to asynchronous mode, the chip measures the low-level period of asynchronous SCI communication data (H'00) transmitted continuously from the host. The chip then calculates the bit rate of transmission from the host, and adjusts the SCI_1 bit rate to match that of the host. The transfer format is 8-bit data, 1 stop bit, and no parity. The reset should end with the RxD pin high. The RxD and TxD pins should be pulled up on the board if necessary. After the reset ends, it takes approximately 100 states before the chip is ready to measure the low-level period.
2. After matching the bit rates, the chip transmits one H'00 byte to the host to indicate the end of bit rate adjustment. The host should confirm that this adjustment end indication (H'00) has been received normally, and transmit one H'55 byte to the chip. If reception could not be performed normally, initiate boot mode again by a reset. Depending on the host's transfer bit rate and system clock frequency of this LSI, there will be a discrepancy between the bit rates of the host and the chip. To operate the SCI properly, set the host's transfer bit rate and system clock frequency of this LSI within the ranges listed in table 19.6.

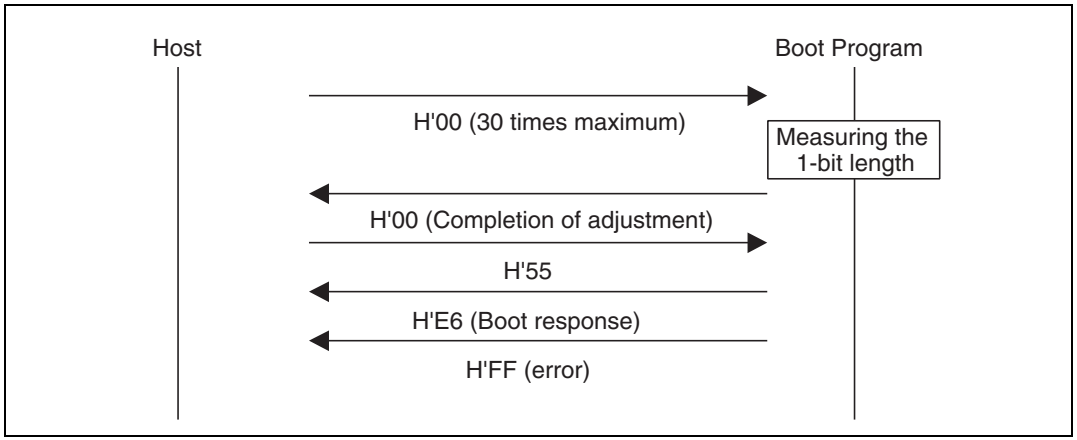


Figure 20.18 Bit-Rate-Adjustment Sequence

(3) Communications Protocol

After adjustment of the bit rate, the protocol for communications between the host and the boot program is as shown below.

1. One-byte commands and one-byte responses

   These commands and responses are comprised of a single byte. These are consists of the inquiries and the ACK for successful completion.
2. n-byte commands or n-byte responses

   These commands and responses are comprised of n bytes of data. These are selections and responses to inquiries.

   The amount of programming data is not included under this heading because it is determined in another command.
3. Error response

   The error response is a response to inquiries. It consists of an error response and an error code and comes two bytes.
4. Programming of 128 bytes

   The size is not specified in commands. The size of n is indicated in response to the programming unit inquiry.
5. Memory read response

   This response consists of 4 bytes of data.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ETCR_1A	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	DMAC
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_1BH	—	—	—	—	—	—	—	—	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_1BL	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
IOARV1B	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
ETCR_1B	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
DMAWER	—	—	—	—	WE1B	WE1A	WE0B	WE0A	
DMATCR	—	—	TEE1	TEE0	—	—	—	—	
DMACR_0A*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_0A*3	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	
DMACR_0B*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_0B*3	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	
DMACR_1A*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_1A*3	DTSZ	SAID	SAIDE	BLKDIR	BLKE	—	—	—	
DMACR_1B*2	DTSZ	DTID	RPE	DTDIR	DTF3	DTF2	DTF1	DTF0	
DMACR_1B*3	—	DAID	DAIDE	—	DTF3	DTF2	DTF1	DTF0	
DMABCRH*2	FAE1	FAE0	SAE1	SAE0	DTA1B	DTA1A	DTA0B	DTA0A	
DMABCRH*3	FAE1	FAE0	—	—	DTA1	—	DTA0	—	
DMABCRL*2	DTE1B	DTE1A	DTE0B	DTE0A	DTIE1B	DTIE1A	DTIE0B	DTIE0A	
DMABCRL*3	DTME1	DTE1	DTME0	DTE0	DTIE1B	DTIE1A	DTIE0B	DTIE0A	
DTCERA	DTCEA7	DTCEA6	DTCEA5	DTCEA4	DTCEA3	DTCEA2	DTCEA1	DTCEA0	DTC
DTCERB	—	—	—	—	—	—	—	—	
DTCERC	—	DTCEC6	DTCEC5	DTCEC4	DTCEC3	DTCEC2	DTCEC1	DTCEC0	
DTCERD	DTCED7	DTCED6	DTCED5	DTCED4	DTCED3	DTCED2	DTCED1	DTCED0	
DTCERE	DTCEE7	DTCEE6	DTCEE5	DTCEE4	DTCEE3	DTCEE2	DTCEE1	DTCEE0	
DTCERF	DTCEF7	DTCEF6	DTCEF5	DTCEF4	DTCEF3	DTCEF2	DTCEF1	DTCEF0	
DTCERG	DTCEG7	DTCEG6	DTCEG5	DTCEG4	DTCEG3	DTCEG2	—	—	
DTCERH	—	—	—	—	—	—	—	—	

Register Name	Reset	High-Speed	Clock Division	Sleep	Module Stop	All Module Clock Stop	Software Standby	Hardware Standby	Module
MAR_0AH	Initialized	—	—	—	—	—	—	Initialized	DMAC
MAR_0AL	Initialized	—	—	—	—	—	—	Initialized	
IOAR_0A	Initialized	—	—	—	—	—	—	Initialized	
ETCR_0A	Initialized	—	—	—	—	—	—	Initialized	
MAR_0BH	Initialized	—	—	—	—	—	—	Initialized	
MAR_0BL	Initialized	—	—	—	—	—	—	Initialized	
IOAR_0B	Initialized	—	—	—	—	—	—	Initialized	
ETCR_0B	Initialized	—	—	—	—	—	—	Initialized	
MAR_1AH	Initialized	—	—	—	—	—	—	Initialized	
MAR_1AL	Initialized	—	—	—	—	—	—	Initialized	
IOAR_1A	Initialized	—	—	—	—	—	—	Initialized	
ETCR_1A	Initialized	—	—	—	—	—	—	Initialized	
MAR_1BH	Initialized	—	—	—	—	—	—	Initialized	
MAR_1BL	Initialized	—	—	—	—	—	—	Initialized	
IOAR_1B	Initialized	—	—	—	—	—	—	Initialized	
ETCR_1B	Initialized	—	—	—	—	—	—	Initialized	
DMAWER	Initialized	—	—	—	—	—	—	Initialized	
DMATCR	Initialized	—	—	—	—	—	—	Initialized	
DMACR_0A	Initialized	—	—	—	—	—	—	Initialized	
DMACR_0B	Initialized	—	—	—	—	—	—	Initialized	
DMACR_1A	Initialized	—	—	—	—	—	—	Initialized	
DMACR_1B	Initialized	—	—	—	—	—	—	Initialized	
DMABCRH	Initialized	—	—	—	—	—	—	Initialized	
DMABCRL	Initialized	—	—	—	—	—	—	Initialized	
DTCERA	Initialized	—	—	—	—	—	—	Initialized	DTC
DTCERB	Initialized	—	—	—	—	—	—	Initialized	
DTCERC	Initialized	—	—	—	—	—	—	Initialized	
DTCERD	Initialized	—	—	—	—	—	—	Initialized	
DTCERE	Initialized	—	—	—	—	—	—	Initialized	
DTCERF	Initialized	—	—	—	—	—	—	Initialized	
DTCERG	Initialized	—	—	—	—	—	—	Initialized	

Instruction	1	2	3	4	5	6	7	8	9
STC CCR,Rd	R:W NEXT								
STC EXR,Rd	R:W NEXT								
STC CCR,@ERd	R:W 2nd	R:W NEXT	W:W EA						
STC EXR,@ERd	R:W 2nd	R:W NEXT	W:W EA						
STC CCR, @(d:16,ERd)	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC EXR, @(d:16,ERd)	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC CCR, @(d:32,ERd)	R:W 2nd	R:W 3rd	R:W 4th	R:W 5th	R:W NEXT	W:W EA			
STC EXR, @(d:32,ERd)	R:W 2nd	R:W 3rd	R:W 4th	R:W 5th	R:W NEXT	W:W EA			
STC CCR,@-ERd	R:W 2nd	R:W NEXT	1 state of internal operation	W:W EA					
STC EXR,@-ERd	R:W 2nd	R:W NEXT	1 state of internal operation	W:W EA					
STC CCR,@aa:16	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC EXR,@aa:16	R:W 2nd	R:W 3rd	R:W NEXT	W:W EA					
STC CCR,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:W NEXT	W:W EA				
STC EXR,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:W NEXT	W:W EA				
STM.L (ERn-ERn+1), @-SP*8	R:W 2nd	R:W NEXT	1 state of internal operation	W:W:M Stack (H)*2	W:W Stack (L) *2				
STM.L (ERn-ERn+2), @-SP*8	R:W 2nd	R:W NEXT	1 state of internal operation	W:W:M Stack (H)*2	W:W Stack (L) *2				