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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	120-TQFP
Supplier Device Package	120-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2368vte34v

Item	Page	Revision (See Manual for Details)
9.13.4 Pin Functions	391	Table amended • PF7/ϕ (Before) PFDDR → (After) PF7DDR
	393	Table amended • PF1/$\overline{CS5}$/$\overline{UCAS}$

PF1DDR	—	0	1	0	1	0	1	—	0	1	0	1
Pin function	$\overline{UCAS}$ output	PF1 input	$\overline{CS5}$ output	PF1 input	PF1 output	PF1 input	PF1 output	$\overline{UCAS}$ output	PF1 input	$\overline{CS5}$ output	PF1 input	PF1 output

14.3.7 Serial Status Register (SSR) Normal Serial Communication Interface Mode (When SMIF in SCMR is 0)	558	Note amended Note: * Only 0 can be written, to clear the flag. Alternately, use the bit clear instruction to clear the flag.
Smart Card Interface Mode (When SMIF in SCMR is 1)	562	Note amended Notes: 1. Only 0 can be written, to clear the flag. Alternately, use the bit clear instruction to clear the flag. 2. etu: Elementary Time Unit: (time for transfer of 1 bit)
14.3.9 Bit Rate Register (BRR) Table 14.3 BRR Settings for Various Bit Rates (Asynchronous Mode)	565	Table amended

	Operating Frequency ϕ (MHz)											
	8			9.8304			10			12		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
19200	0	12	0.16	0	15	0.00	0	15	–1.73	0	19	–2.34
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	—	—	—	0	7	0.00	0	7	–1.73	0	9	–2.34

	Operating Frequency ϕ (MHz)											
	12.288			14			14.7456			16		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	39	0.00	0	45	–0.93	0	47	0.00	0	51	0.16
19200	0	19	0.00	0	22	–0.93	0	23	0.00	0	25	0.16
31250	0	11	2.40	0	13	0.00	0	14	–1.70	0	15	0.00
38400	0	9	0.00	—	—	—	0	11	0.00	0	12	0.16

Type	Symbol	Pin No. TFP-120	Pin No. QFP-128*1	I/O	Function
System control	$\overline{\text{RES}}$	77	85	Input	Reset pin. When this pin is driven low, the chip is reset.
	$\overline{\text{STBY}}$	88	96	Input	When this pin is driven low, a transition is made to hardware standby mode.
	EMLE	30	34	Input	Enables emulator. This pin should be connected to the power supply (0 V).
Address bus	A23 to A0	29 to 23, 21 to 18, 16 to 9, 7 to 3	33 to 27, 25 to 22, 20 to 13, 11 to 7	Output	Address output pins.
Data bus	D15 to D0	68 to 61, 59, 57 to 51	76 to 69, 65, 63 to 57	Input/ output	These pins constitute a bidirectional data bus.
Bus control	$\overline{\text{CS7}}$ to $\overline{\text{CS0}}$	29,71,70, 106, 92 to 89	33,79,78, 116,102, 101,98,97	Output	Signals that select division areas 7 to 0 in the external address space.
	$\overline{\text{AS}}$	75	83	Output	When this pin is low, it indicates that address output on the address bus is valid.
	$\overline{\text{RD}}$	74	82	Output	When this pin is low, it indicates that the external address space is being read.
	$\overline{\text{HWR}}$	73	81	Output	Strobe signal indicating that external address space is to be written, and the upper half (D15 to D8) of the data bus is enabled. Write enable signal for accessing the DRAM space.
	$\overline{\text{LWR}}$	72	80	Output	Strobe signal indicating that external address space is to be written, and the lower half (D7 to D0) of the data bus is enabled.
	$\overline{\text{BREQ}}$	108	118	Input	The external bus master requests the bus to this LSI.
	$\overline{\text{BREQO}}$	106	116	Input	External bus request signal when the internal bus master accesses the external space in external bus release state.

6.6.4 Pins Used for DRAM Interface

Table 6.6 shows the pins used for DRAM interfacing and their functions. Since the $\overline{CS2}$, $\overline{CS5}$ pins are in the input state after a reset, set the corresponding DDR to 1 when $\overline{RAS2}$, $\overline{RAS5}$ signals are output.

Table 6.6 DRAM Interface Pins

Pin	With DRAM Setting	Name	I/O	Function
$\overline{HWR}$	$\overline{WE}$	Write enable	Output	Write enable for DRAM space access
$\overline{CS2}$	$\overline{RAS2}$	Row address strobe 2/ row address strobe	Output	Row address strobe when area 2 is designated as DRAM space or row address strobe when areas 2 to 5 are designated as continuous DRAM space
$\overline{CS3}$	$\overline{RAS3}$	Row address strobe 3	Output	Row address strobe when area 3 is designated as DRAM space
$\overline{UCAS}$	$\overline{UCAS}$	Upper column address strobe	Output	Upper column address strobe for 16-bit DRAM space access or column address strobe for 8-bit DRAM space access
$\overline{LCAS}$	$\overline{LCAS}$	Lower column address strobe	Output	Lower column address strobe signal for 16-bit DRAM space access
$\overline{RD}$, $\overline{OE}$	$\overline{OE}$	Output enable	Output	Output enable signal for DRAM space access
$\overline{WAIT}$	$\overline{WAIT}$	Wait	Input	Wait request signal
A15 to A0	A15 to A0	Address pins	Output	Row address/column address multiplexed output
D15 to D0	D15 to D0	Data pins	I/O	Data input/output pins

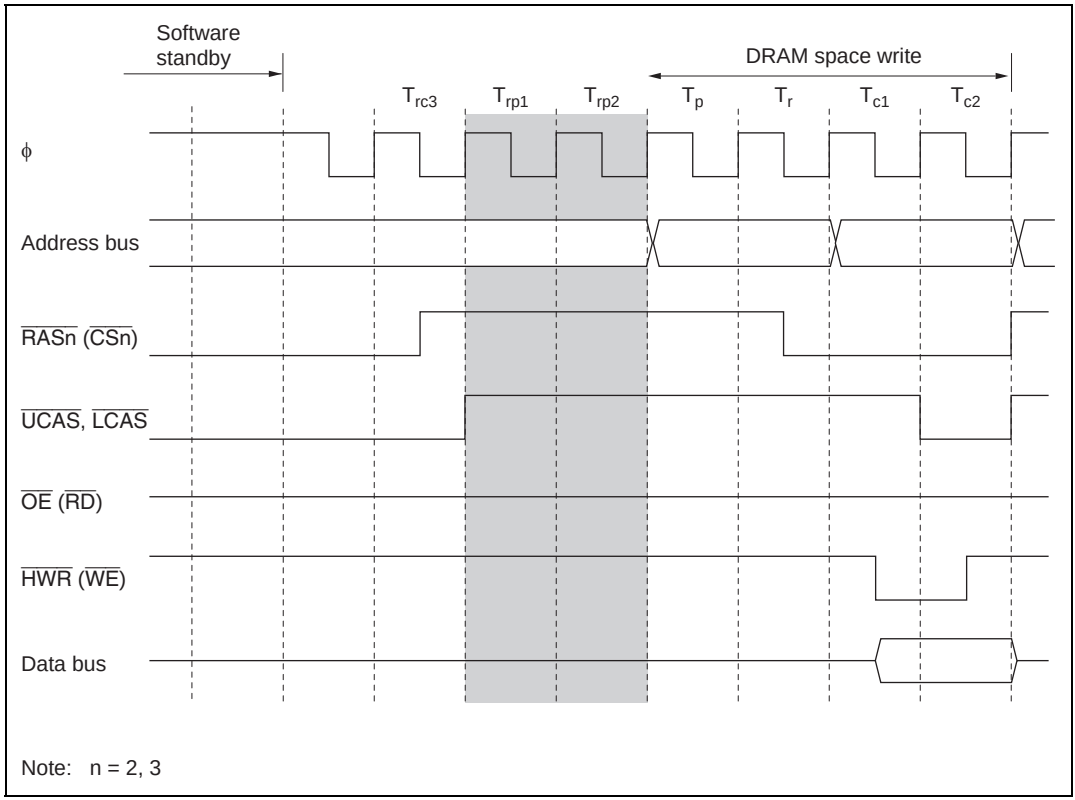


Figure 6.39 Example of Timing when Precharge Time after Self-Refreshing Is Extended by 2 States

Refreshing and All-Module-Clocks-Stopped Mode: In this LSI, if the ACSE bit is set to 1 in MSTPCRH, and then a SLEEP instruction is executed with the setting for all peripheral module clocks to be stopped (MSTPCR = H'FFFF, EXMSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE, EXMSTPCR = H'FFFF), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered, in which the bus controller and I/O port clocks are also stopped. As the bus controller clock is also stopped in this mode, CBR refreshing is not executed. If DRAM is connected externally and DRAM data is to be retained in sleep mode, the ACSE bit must be cleared to 0 in MSTPCRH.

6.6.13 DMAC Single Address Transfer Mode and DRAM Interface

When burst mode is selected on the DRAM interface, the $\overline{\text{DACK}}$ output timing can be selected with the DDS bit in DRAMCR. When DRAM space is accessed in DMAC single address mode at the same time, these bits select whether or not burst access is to be performed.

Section 7 DMA Controller (DMAC)

This LSI has a built-in DMA controller (DMAC) which can carry out data transfer on up to 4 channels.

7.1 Features

- Choice of short address mode or full address mode
  - — Short address mode
    Maximum of 4 channels can be used
    Dual address mode or single address mode can be selected
    In dual address mode, one of the two addresses, transfer source and transfer destination, is specified as 24 bits and the other as 16 bits
    In single address mode, transfer source or transfer destination address only is specified as 24 bits
    In single address mode, transfer can be performed in one bus cycle
    Choice of sequential mode, idle mode, or repeat mode for dual address mode and single address mode
  - — Full address mode
    Maximum of 2 channels can be used
    Transfer source and transfer destination addresses as specified as 24 bits
    Choice of normal mode or block transfer mode
- 16-Mbyte address space can be specified directly
- Byte or word can be set as the transfer unit
- Activation sources: internal interrupt, external request, auto-request (depending on transfer mode)
  Six 16-bit timer-pulse unit (TPU) compare match/input capture interrupts
  Serial communication interface (SCI_0, SCI_1) transmission complete interrupt, reception complete interrupt
  A/D converter conversion end interrupt
  External request
  Auto-request
- Module stop mode can be set

9.4 Port 4

Port 4 is an 8-bit input-only port. Port 4 has the following register.

- Port 4 register (PORT4)

9.4.1 Port 4 Register (PORT4)

PORT4 is an 8-bit read-only register that shows port 4 pin states.

PORT4 cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	P47	—*	R	The pin states are always read from this register.
6	P46	—*	R	
5	P45	—*	R	
4	P44	—*	R	
3	P43	—*	R	
2	P42	—*	R	
1	P41	—*	R	
0	P40	—*	R	

Note: * Determined by the states of pins P47 to P40.

9.5.3 Port 5 Register (PORT5)

PORT5 shows the pin states. PORT5 cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	Undefined	R	Reserved Undefined values are read from these bits.
3	P53	—*	R	If bits P53 to P50 are read while P5DDR bits are set to 1, the P5DR values are read. If a port 5 read is performed while P5DDR bits are cleared to 0, the pin states are read.
2	P52	—*	R	
1	P51	—*	R	
0	P50	—*	R	

Note: * Determined by the states of pins P53 to P50.

9.5.4 Pin Functions

Port 5 pins also function as the pins for SCI I/Os, A/D converter inputs, and interrupt inputs. The correspondence between the register specification and the pin functions is shown below.

- P53/$\overline{\text{ADTRG}}$/$\overline{\text{IRQ3}}$

The pin function is switched as shown below according to the combination of bits TRGS1 and TRGS0 in the A/D control register (ADCR), bit ITS3 in ITSR, and bit P53DDR.

P53DDR	0	1
Pin function	P53 input	P53 output
	$\overline{\text{ADTRG}}$ input*1	
	$\overline{\text{IRQ3}}$ interrupt input*2	

Notes: 1. $\overline{\text{ADTRG}}$ input when TRGS1 = TRGS0 = 1.
2. $\overline{\text{IRQ3}}$ input when ITS3 = 0.

Section 11 Programmable Pulse Generator (PPG)

The programmable pulse generator (PPG) provides pulse outputs by using the 16-bit timer pulse unit (TPU) as a time base. The PPG pulse outputs are divided into 4-bit groups (groups 3 to 0) that can operate both simultaneously and independently. The block diagram of PPG is shown in figure 11.1

11.1 Features

- 16-bit output data
- Four output groups
- Selectable output trigger signals
- Non-overlap mode
- Can operate together with the data transfer controller (DTC) and the DMA controller (DMAC)
- Settable inverted output
- Module stop mode can be set

11.3.2 Output Data Registers H, L (PODRH, PODRL)

PODRH and PODRL store output data for use in pulse output. A bit that has been set for pulse output by NDER is read-only and cannot be modified.

- PODRH

Bit	Bit Name	Initial Value	R/W	Description
7	POD15	0	R/W	Output Data Register 15 to 8
6	POD14	0	R/W	For bits which have been set to pulse output by NDERH, the output trigger transfers NDRH values to this register during PPG operation. While NDERH is set to 1, the CPU cannot write to this register. While NDERH is cleared, the initial output value of the pulse can be set.
5	POD13	0	R/W	
4	POD12	0	R/W	
3	POD11	0	R/W	
2	POD10	0	R/W	
1	POD9	0	R/W	
0	POD8	0	R/W	

- PODRL

Bit	Bit Name	Initial Value	R/W	Description
7	POD7	0	R/W	Output Data Register 7 to 0
6	POD6	0	R/W	For bits which have been set to pulse output by NDERL, the output trigger transfers NDRL values to this register during PPG operation. While NDERL is set to 1, the CPU cannot write to this register. While NDERL is cleared, the initial output value of the pulse can be set.
5	POD5	0	R/W	
4	POD4	0	R/W	
3	POD3	0	R/W	
2	POD2	0	R/W	
1	POD1	0	R/W	
0	POD0	0	R/W	

11.4.1 Output Timing

If pulse output is enabled, NDR contents are transferred to PODR and output when the specified compare match event occurs. Figure 11.3 shows the timing of these operations for the case of normal output in groups 2 and 3, triggered by compare match A.

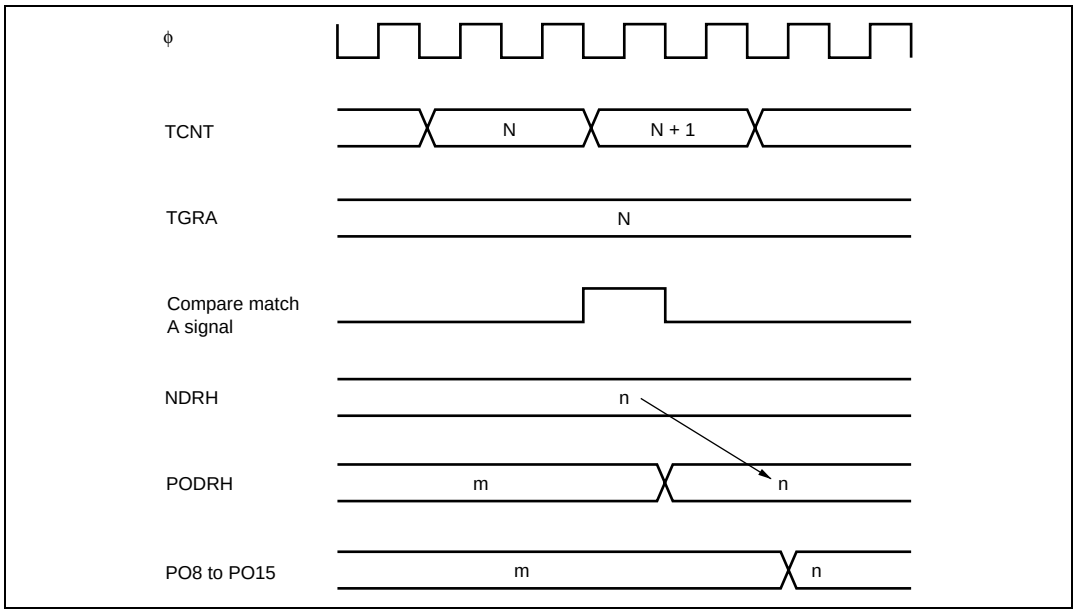


Figure 11.3 Timing of Transfer and Output of NDR Contents (Example)

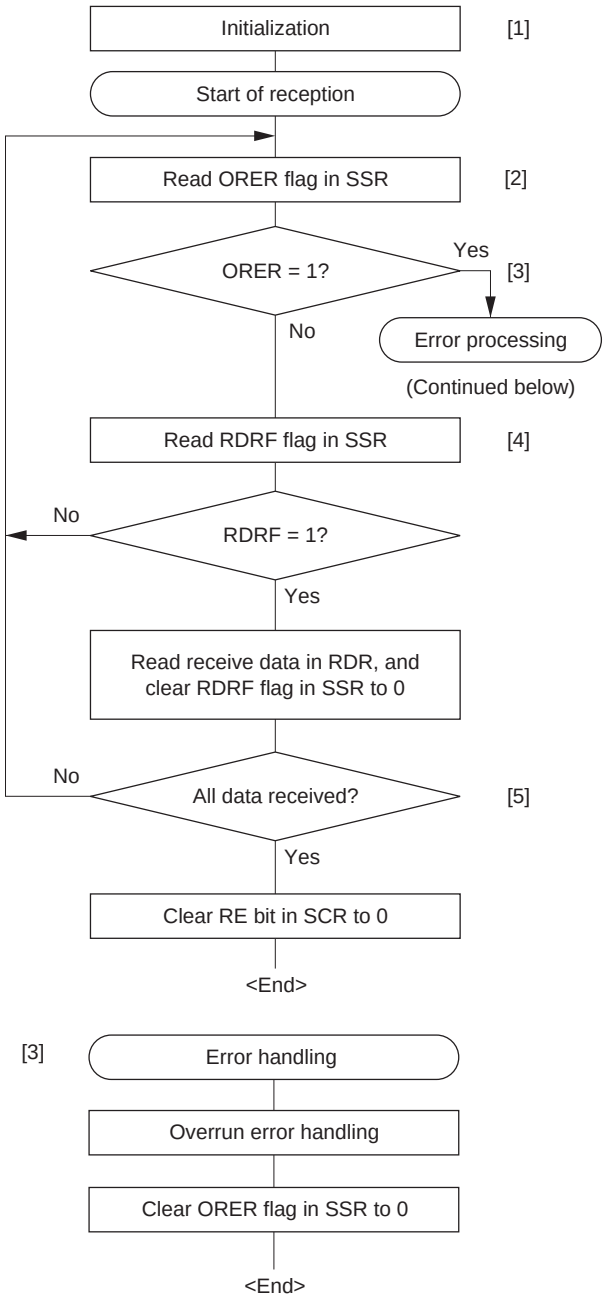
Bit	Bit Name	Initial Value	R/W	Description
3	PER	0	R/(W)*	Parity Error Indicates that a parity error occurred while receiving in asynchronous mode and the reception has ended abnormally. [Setting condition] When a parity error is detected during reception If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either. [Clearing condition] When 0 is written to PER after reading PER = 1 The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.
2	TEND	1	R	Transmit End [Setting conditions] • When the TE bit in SCR is 0 • When TDRE = 1 at transmission of the last bit of a 1-byte serial transmit character [Clearing conditions] • When 0 is written to TDRE after reading TDRE = 1 • When the DMAC or DTC is activated by a TXI interrupt and writes data to TDR
1	MPB	0	R	Multiprocessor Bit MPB stores the multiprocessor bit in the receive data. When the RE bit in SCR is cleared to 0 its previous state is retained.
0	MPBT	0	R/W	Multiprocessor Bit Transfer MPBT sets the multiprocessor bit to be added to the transmit data.

Note: * Only 0 can be written, to clear the flag. Alternately, use the bit clear instruction to clear the flag.

14.3.10 IrDA Control Register (IrCR)

IrCR selects the function of SCI_0.

Bit	Bit Name	Initial Value	R/W	Description
7	IrE	0	R/W	IrDA Enable Specifies normal SCI mode or IrDA mode for SCI_0 input/output. 0: Pins TxD0/IrTxD and RxD0/IrRxD function as TxD0 and RxD0 1: Pins TxD0/IrTxD and RxD0/IrRxD function as IrTxD and IrRxD
6 5 4	IrCKS2 IrCKS1 IrCKS0	0 0 0	R/W R/W R/W	IrDA Clock Select 2 to 0 Specifies the high pulse width in IrTxD output pulse encoding when the IrDA function is enabled. 000: Pulse width = B × 3/16 (3/16 of bit rate) 001: Pulse width = ϕ/2 010: Pulse width = ϕ/4 011: Pulse width = ϕ/8 100: Pulse width = ϕ/16 101: Pulse width = ϕ/32 110: Pulse width = ϕ/64 111: Pulse width = ϕ/128
3 to 0	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.



[1] SCI initialization:
The RxD pin is automatically designated as the receive data input pin.

[2] [3] Receive error handling:
If a receive error occurs, read the ORER flag in SSR, and after performing the appropriate error handling, clear the ORER flag to 0. Transfer cannot be resumed if the ORER flag is set to 1.

[4] SCI status check and receive data read:
Read SSR and check that the RDRF flag is set to 1, then read the receive data in RDR and clear the RDRF flag to 0. Transition of the RDRF flag from 0 to 1 can also be identified by an RXI interrupt.

[5] Serial reception continuation procedure:
To continue serial reception, before the MSB (bit 7) of the current frame is received, finish reading the RDRF flag, reading RDR, and clearing the RDRF flag to 0. The RDRF flag is cleared automatically when the DMAC or DTC is activated by a receive-data-full interrupt (RXI) request and the RDR value is read.

Figure 14.19 Sample Serial Reception Flowchart

(g) User Boot MAT Information Inquiry

The boot program will return the number of user boot MATs and their addresses.

Command

H'24

- Command, H'24, (one byte): Inquiry regarding user boot MAT information

Response

H'34	Size	Number of areas	
Area-start address			Area-last address
...			
SUM			

- Response, H'34, (one byte): Response to user boot MAT information inquiry
- Size (one byte): The number of bytes that represents the number of areas, area-start addresses, and area-last address
- Number of Areas (one byte): The number of consecutive user boot MAT areas
  When user boot MAT areas are consecutive, the number of areas returned is H'01.
- Area-start address (four byte): Start address of the area
- Area-last address (four byte): Last address of the area
  There are as many groups of data representing the start and last addresses as there are areas.
- SUM (one byte): Checksum

(h) User MAT Information Inquiry

The boot program will return the number of user MATs and their addresses.

Command

H'25

- Command, H'25, (one byte): Inquiry regarding user MAT information

Response

H'35	Size	Number of areas	
Start address area			Last address area
...			
SUM			

- Response, H'35, (one byte): Response to the user MAT information inquiry
- Size (one byte): The number of bytes that represents the number of areas, area-start address and area-last address
- Number of areas (one byte): The number of consecutive user MAT areas
  When the user MAT areas are consecutive, the number of areas is H'01.
- Area-start address (four byte): Start address of the area

Register Name	Abbreviation	Bit No.	Address	Module	Data Width	Access States
Smart card mode register_1	SCMR_1	8	H'FF86	SCI_1	8	2
Serial mode register_2	SMR_2	8	H'FF88	SCI_2	8	2
Bit rate register_2	BRR_2	8	H'FF89	SCI_2	8	2
Serial control register_2	SCR_2	8	H'FF8A	SCI_2	8	2
Transmit data register_2	TDR_2	8	H'FF8B	SCI_2	8	2
Serial status register_2	SSR_2	8	H'FF8C	SCI_2	8	2
Receive data register_2	RDR_2	8	H'FF8D	SCI_2	8	2
Smart card mode register_2	SCMR_2	8	H'FF8E	SCI_2	8	2
A/D data register A	ADDRA	16	H'FF90	A/D	16	2
A/D data register B	ADDRB	16	H'FF92	A/D	16	2
A/D data register C	ADDRC	16	H'FF94	A/D	16	2
A/D data register D	ADDRD	16	H'FF96	A/D	16	2
A/D data register E	ADDRE	16	H'FF98	A/D	16	2
A/D data register F	ADDRF	16	H'FF9A	A/D	16	2
A/D data register G	ADDRG	16	H'FF9C	A/D	16	2
A/D data register H	ADDRH	16	H'FF9E	A/D	16	2
A/D control/status register	ADCSR	8	H'FFA0	A/D	16	2
A/D control register	ADCR	8	H'FFA1	A/D	16	2
D/A data register 2	DADR2	8	H'FFA8	D/A	8	2
D/A data register 3	DADR3	8	H'FFA9	D/A	8	2
D/A control register 23	DACR23	8	H'FFAA	D/A	8	2
Timer control register_0	TCR_0	8	H'FFB0	TMR_0	16	2
Timer control register_1	TCR_1	8	H'FFB1	TMR_1	16	2
Timer control/status register_0	TCSR_0	8	H'FFB2	TMR_0	16	2
Timer control/status register_1	TCSR_1	8	H'FFB3	TMR_1	16	2
Time constant register_A0	TCORA_0	8	H'FFB4	TMR_0	16	2
Time constant register_A1	TCORA_1	8	H'FFB5	TMR_1	16	2
Time constant register_B0	TCORB_0	8	H'FFB6	TMR_0	16	2
Time constant register_B1	TCORB_1	8	H'FFB7	TMR_1	16	2
Timer counter_0	TCNT_0	8	H'FFB8	TMR_0	16	2
Timer counter_1	TCNT_1	8	H'FFB9	TMR_1	16	2

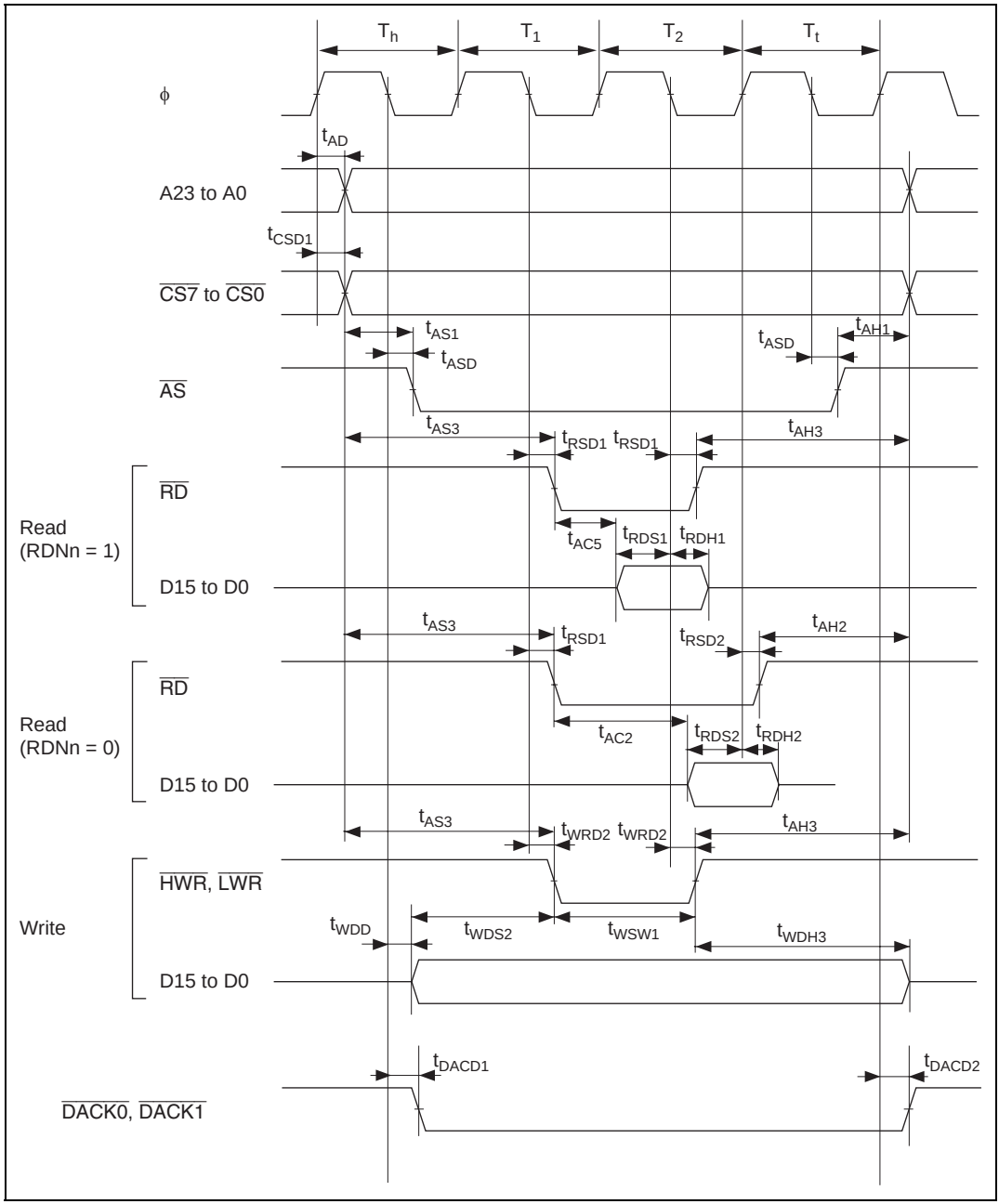


Figure 25.9 Basic Bus Timing: Two-State Access ($\overline{CS}$ Assertion Period Extended)

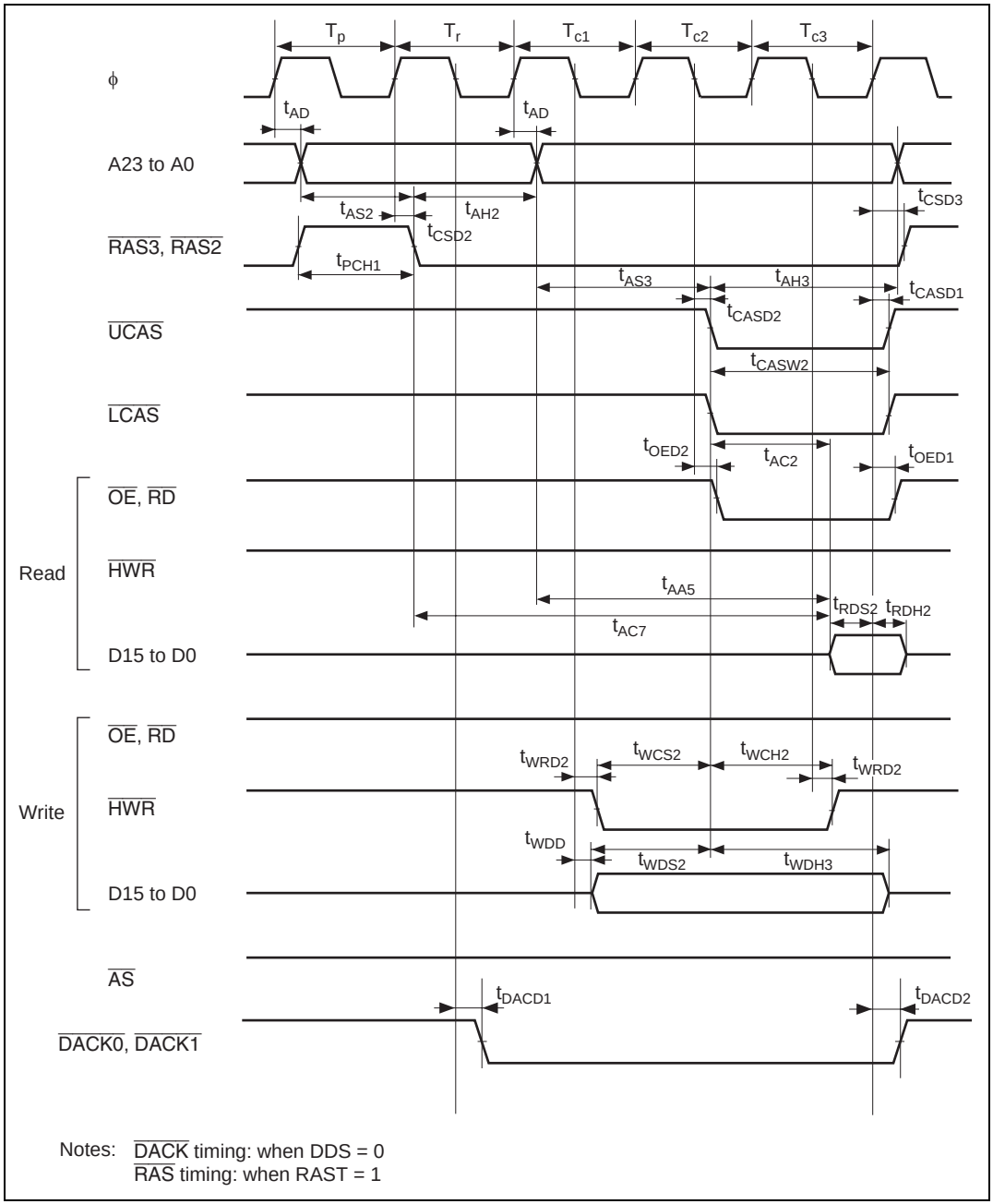


Figure 25.16 DRAM Access Timing: Three-State Access (RAST = 1)

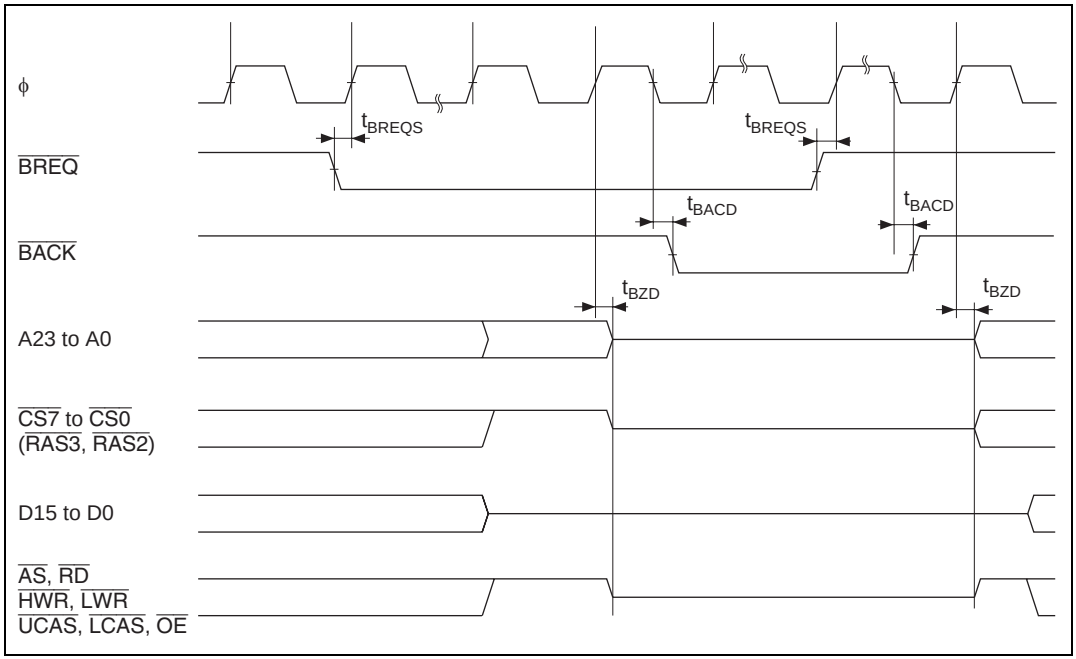


Figure 25.22 External Bus Release Timing

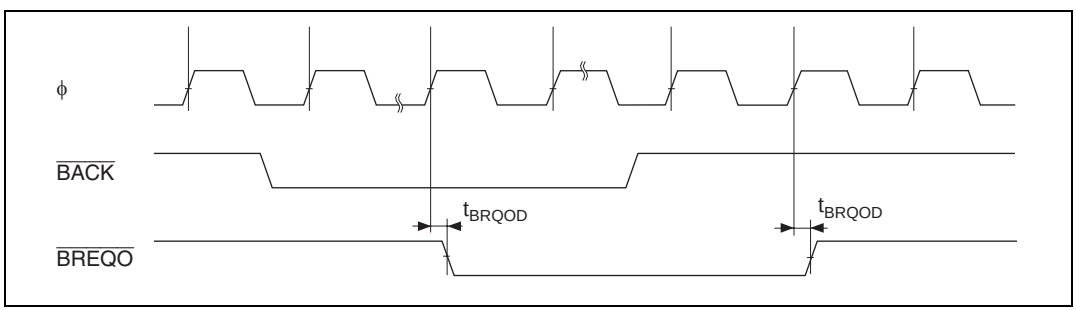


Figure 25.23 External Bus Request Output Timing

Table 25.20 Bus Timing (2)

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min	Max	Unit	Test Conditions
$\overline{WR}$ delay time 1	t_{WRD1}	—	15	ns	Figures 25.6 to 25.19
$\overline{WR}$ delay time 2	t_{WRD2}	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 \times t_{cyc}$ –13	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	$1.5 \times t_{cyc}$ –13	—	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data setup time 1	t_{WDS1}	$0.5 \times t_{cyc}$ –13	—	ns	
Write data setup time 2	t_{WDS2}	$1.0 \times t_{cyc}$ –13	—	ns	
Write data setup time 3	t_{WDS3}	$1.5 \times t_{cyc}$ –13	—	ns	
Write data hold time 1	t_{WDH1}	$0.5 \times t_{cyc}$ –8	—	ns	
Write data hold time 2	t_{WDH2}	$1.0 \times t_{cyc}$ –8	—	ns	
Write data hold time 3	t_{WDH3}	$1.5 \times t_{cyc}$ –8	—	ns	
Write command setup time 1	t_{WCS1}	$0.5 \times t_{cyc}$ –10	—	ns	
Write command setup time 2	t_{WCS2}	$1.0 \times t_{cyc}$ –10	—	ns	
Write command hold time 1	t_{WCH1}	$0.5 \times t_{cyc}$ –10	—	ns	
Write command hold time 2	t_{WCH2}	$1.0 \times t_{cyc}$ –10	—	ns	
Read command setup time 1	t_{RCS1}	$1.5 \times t_{cyc}$ –10	—	ns	
Read command setup time 2	t_{RCS2}	$2.0 \times t_{cyc}$ –10	—	ns	
Read command hold time	t_{RCH}	$0.5 \times t_{cyc}$ –10	—	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	15	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	15	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	$0.5 \times t_{cyc}$ –10	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	$1.5 \times t_{cyc}$ –10	—	ns	
$\overline{CAS}$ pulse width 1	t_{CASW1}	$1.0 \times t_{cyc}$ –20	—	ns	
$\overline{CAS}$ pulse width 2	t_{CASW2}	$1.5 \times t_{cyc}$ –20	—	ns	
$\overline{CAS}$ precharge time 1	t_{CPW1}	$1.0 \times t_{cyc}$ –20	—	ns	
$\overline{CAS}$ precharge time 2	t_{CPW2}	$1.5 \times t_{cyc}$ –20	—	ns	
$\overline{OE}$ delay time 1	t_{OED1}	—	15	ns	
$\overline{OE}$ delay time 2	t_{OED2}	—	15	ns	

Appendix

A. I/O Port States in Each Pin State

Port Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
Port 1	1, 2. 4, 7	T	T	Keep	Keep	I/O port
Port 2	1, 2. 4, 7	T	T	Keep	Keep	I/O port
P34 to P30	1, 2. 4, 7	T	T	Keep	Keep	I/O port
P35/($\overline{OE}$)	1, 2. 4, 7	T	T	[OPE = 0, $\overline{OE}$ (CKE) output] T [OPE = 1, $\overline{OE}$ output] H [Other than the above] Keep	[$\overline{OE}$ (CKE) output] T [Other than the above] Keep	[$\overline{OE}$ output] $\overline{OE}$ (CKE) [Other than the above] I/O port
Port 4	1, 2. 4, 7	T	T	T	T	Input port
P53 to P50	1, 2. 4, 7	T	T	Keep	Keep	I/O port
Port 8	1, 2. 4, 7	T	T	Keep	Keep	I/O port
P95/DA3	1, 2. 4, 7	T	T	[DAOE3 = 1] Keep [DAOE3 = 0] T	Keep	Input port
P94/DA2	1, 2. 4, 7	T	T	[DAOE2 = 1] Keep [DAOE2 = 0] T	Keep	Input port