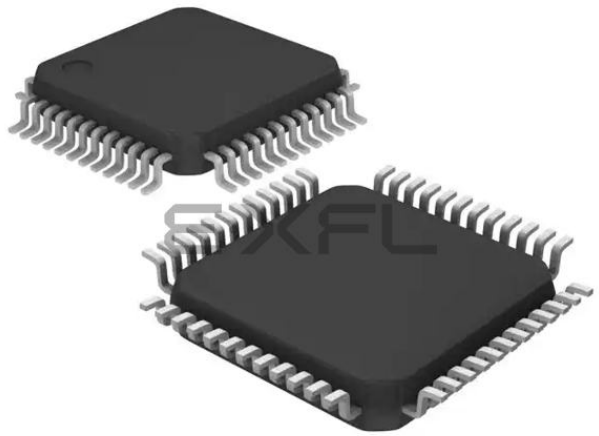

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano100le3bn

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano100 Features – Base Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access
  - 64K/32K/123K bytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 8 channels: one VDMA channel, 6 PDMA channels and one CRC channel
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode

- Supports word/half-word/byte transfer data width from/to peripheral
- Supports address direction: increment, fixed, and wrap around

- CRC
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
    - CRC-8: $X^8 + X^2 + X + 1$
    - CRC-16: $X^{16} + X^{15} + X^2 + 1$
    - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12 MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PD.0 ~ PD.1 and PC.6 ~ PC.7
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC, DAC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode

receiving

- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests: one for transmitting and the other for receiving

- ADC
  - 12-bit SAR ADC up to 2Msps conversion rate
  - Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
  - Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion started by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC
- DAC
  - 12-bit monotonic output with 400K conversion rate
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Synchronized update capability for two DACs (group function)
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Reset (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process

- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire, no slave select signal, bi-direction interface
- Wake system up from Power-down mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
- I^2S
  - Interface with external audio CODEC
  - Operated as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports I^2S and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two PDMA requests: one for transmitting and the other for receiving

2.4 Nano130 Features – Advanced Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC 25egiste
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

3.3.2.2 NuMicro™ Nano110 LQFP 64-pin

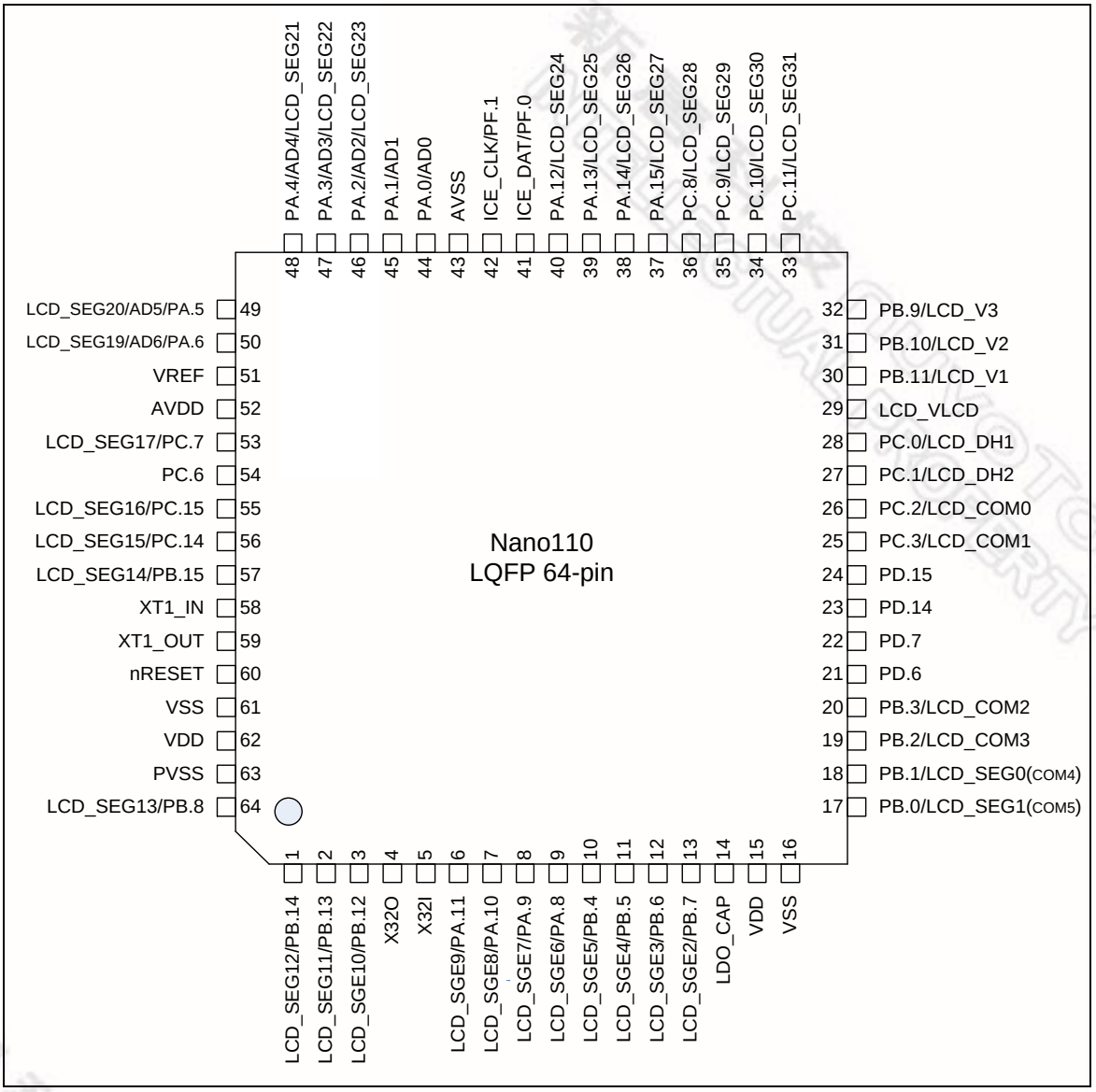


Figure 3-6 NuMicro™ Nano110 LQFP 64-pin Diagram

3.3.3.3 NuMicro™ Nano120 LQFP 48-pin

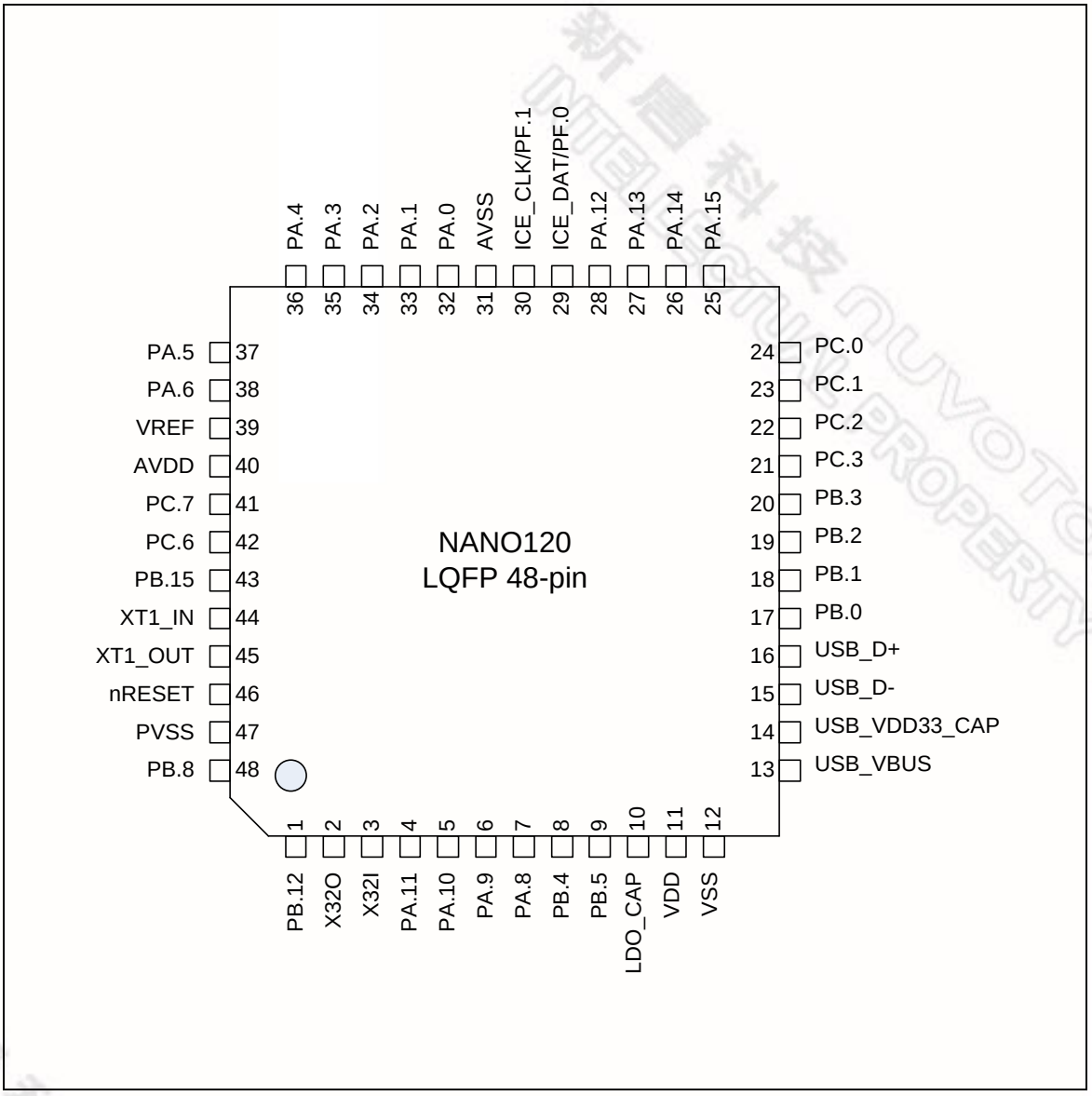


Figure 3-9 NuMicro™ Nano120 LQFP 48-pin Diagram

3.4 Pin Description

3.4.1 NuMicro™ Nano100 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
1			PE.13	**I/O**	General purpose digital I/O pin
2	1		PB.14	**I/O**	General purpose digital I/O pin
			INT0	**I**	External interrupt0 input pin
			SC2_CD	**I**	SmartCard2 card detect pin
			SPI2_SS1	**I/O**	SPI2 2nd slave select pin
3	2		PB.13	**I/O**	General purpose digital I/O pin
			EBI_AD1	**I/O**	EBI Address/Data bus bit1
4	3	1	PB.12	**I/O**	General purpose digital I/O pin
			EBI_AD0	**I/O**	EBI Address/Data bus bit0
			FCLKO	**O**	Frequency Divider output pin
5					NC
6	4	2	X32O	**O**	External 32.768 kHz crystal output pin
7	5	3	X32I	**I**	External 32.768 kHz crystal input pin
8					NC
9	6	4	PA.11	**I/O**	General purpose digital I/O pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
			EBI_nRD	**O**	EBI read enable output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	PA.10	**I/O**	General purpose digital I/O pin
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			EBI_nWR	**O**	EBI write enable output pin
			SC0_PWR	**O**	SmartCard0 Power pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	PA.9	**I/O**	General purpose digital I/O pin
			I2C0_SCL	**I/O**	I^2C0 clock pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin			
			PWM0_CH2	**I/O**	PWM0 Channel2 output
			EBI_AD15	**I/O**	EBI Address/Data bus bit15
			TC2	**I**	Timer2 capture input
			UART0_RXD	**I**	UART0 Data receiver input pin
78	39	27	PA.13	**I/O**	General purpose digital I/O pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			EBI_AD14	**I/O**	EBI Address/Data bus bit14
			TC1	**I**	Timer1 capture input
			I2C0_SCL	**I/O**	I^2C0 clock pin
79	40	28	PA.12	**I/O**	General purpose digital I/O pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			EBI_AD13	**I/O**	EBI Address/Data bus bit13
			TC0	**I**	Timer0 capture input
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
80	41	29	ICE_DAT	**I/O**	Serial Wired Debugger Data pin
			PF.0	**I/O**	General purpose digital I/O pin
			INT0	**I**	External interrupt0 input pin
81	42	30	ICE_CLK	**I**	Serial Wired Debugger Clock pin
			PF.1	**I/O**	General purpose digital I/O pin
			FCLKO	**O**	Frequency Divider output pin
			INT1	**I**	External interrupt1 input pin
82					NC
83			VDD	**P**	Power supply for I/O ports and LDO source for internal PLL and digital circuit
84					NC
85			VSS	**P**	Ground
86			VSS	**P**	Ground
87	43	31	AVSS	**AP**	Ground Pin for analog circuit
88			AVSS	**AP**	Ground Pin for analog circuit
89	44	32	PA.0	**I/O**	General purpose digital I/O pin

3.4.2 NuMicro™ Nano110 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.13	I/O	General purpose digital I/O pin
			LCD_SEG27	O	LCD segment output 27 at LQFP128
2	1		PB.14	I/O	General purpose digital I/O pin
			INT0	I	External interrupt0 input pin
			SC2_CD	I	SmartCard2 card detect
			SPI2_SS1	I/O	SPI2 2nd slave select pin
			LCD_SEG12	O	LCD segment output 12 at LQFP64
			LCD_SEG26	O	LCD segment output 26 at LQFP128
3	2		PB.13	I/O	General purpose digital I/O pin
			EBI_AD1	I/O	EBI Address/Data bus bit1
			LCD_SEG11	O	LCD segment output 11 at LQFP64
			LCD_SEG25	O	LCD segment output 25 at LQFP128
4	3		PB.12	I/O	General purpose digital I/O pin
			EBI_AD0	I/O	EBI Address/Data bus bit0
			FCLKO	O	Frequency Divider output pin
			LCD_SEG10	O	LCD segment output 10 at LQFP64
			LCD_SEG24	O	LCD segment output 24 at LQFP128
5					NC
6	4		X32O	O	External 32.768 kHz crystal output pin
7	5		X32I	I	External 32.768 kHz crystal input pin
8					NC
9	6		PA.11	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I2C1 clock pin
			EBI_nRD	O	EBI read enable output pin
			SC0_RST	O	SmartCard0 RST pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG9	O	LCD segment output 9 at LQFP64
			LCD_SEG23	O	LCD segment output 23 at LQFP128
10	7		PA.10	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			EBI_nWR	**O**	EBI write enable output pin
			SC0_PWR	**O**	SmartCard0 Power pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
			LCD_SEG8	**O**	LCD segment output 8 at LQFP64
			LCD_SEG22	**O**	LCD segment output 22 at LQFP128
11	8		PA.9	**I/O**	General purpose digital I/O pin
			I2C0_SCL	**I/O**	I^2C0 clock pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	**I/O**	SPI2 serial clock pin
			LCD_SEG7	**O**	LCD segment output 7 at LQFP64
			LCD_SEG21	**O**	LCD segment output 21 at LQFP128
12	9		PA.8	**I/O**	General purpose digital I/O pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin(SC0_UART_TXD)
			SPI2_SS0	**I/O**	SPI2 1st slave select pin
			LCD_SEG6	**O**	LCD segment output 6 at LQFP64
			LCD_SEG20	**O**	LCD segment output 20 at LQFP128
13			PD.8	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at LQFP128
14			PD.9	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at LQFP128
15			PD.10	**I/O**	General purpose digital I/O pin
			LCD_SEG17	**O**	LCD segment output 17 at LQFP128
16			PD.11	**I/O**	General purpose digital I/O pin
			LCD_SEG16	**O**	LCD segment output 16 at LQFP128
17			PD.12	**I/O**	General purpose digital I/O pin
			LCD_SEG15	**O**	LCD segment output 15 at LQFP128
18			PD.13	**I/O**	General purpose digital I/O pin
			LCD_SEG14	**O**	LCD segment output 14 at LQFP128

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			LCD_SEG0	O	LCD segment output 0 at LQFP64 (or as LCD_COM4)
			LCD_SEG6	O	LCD segment output 6 at LQFP128
46	19		PB.2	I/O	General purpose digital I/O pin
			UART0_RTSn	O	UART0 Request to Send output pin
			EBI_nWRL	O	EBI low byte write enable output pin
			SPI1_CLK	I/O	SPI1 serial clock pin
			LCD_COM3	O	LCD common output 3 at LQFP64
			LCD_SEG5	O	LCD segment output 5 at LQFP128
47	20		PB.3	I/O	General purpose digital I/O pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			EBI_nWRH	O	EBI high byte write enable output pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			LCD_COM2	O	LCD common output 2 at LQFP64
			LCD_SEG4	O	LCD segment output 4 at LQFP128
48	21		PD.6	I/O	General purpose digital I/O pin
			LCD_SEG3	O	LCD segment output 3 at LQFP128
49	22		PD.7	I/O	General purpose digital I/O pin
			LCD_SEG2	O	LCD segment output 2 at LQFP128
50	23		PD.14	I/O	General purpose digital I/O pin
			LCD_SEG1	O	LCD segment output 1 at LQFP128 (or as LCD_COM5)
51	24		PD.15	I/O	General purpose digital I/O pin
			LCD_SEG0	O	LCD segment output 0 at LQFP128 (or as LCD_COM4)
52			PC.5	I/O	General purpose digital I/O pin
			SPI0_MOSI1	I/O	SPI0 2nd MOSI (Master Out, Slave In) pin
			LCD_COM3	O	LCD common output 3 at LQFP128
53			PC.4	I/O	General purpose digital I/O pin
			SPI0_MISO1	I/O	SPI0 2nd MISO (Master In, Slave Out) pin
			LCD_COM2	O	LCD common output 2 at LQFP128

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
54	25		PC.3	**I/O**	General purpose digital I/O pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
			I2S_DO	**O**	I2S data output
			SC1_RST	**O**	SmartCard1 RST pin
			LCD_COM1	**O**	LCD common output 1 at LQFP64
			LCD_COM1	**O**	LCD common output 1 at LQFP128
55	26		PC.2	**I/O**	General purpose digital I/O pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
			I2S_DI	**I**	I2S data input
			SC1_PWR	**O**	SmartCard1 PWR pin
			LCD_COM0	**O**	LCD common output 0 at LQFP64
			LCD_COM0	**O**	LCD common output 0 at LQFP128
56	27		PC.1	**I/O**	General purpose digital I/O pin
			SPI0_CLK	**I/O**	SPI0 serial clock pin
			I2S_BCLK	**I/O**	I2S bit clock pin
			SC1_DAT	**I/O**	SmartCard1 DATA pin(SC1_UART_RXD)
			LCD_DH2	**O**	LCD externl capacitor pin of charge pump circuit at LQFP64
			LCD_DH2	**O**	LCD externl capacitor pin of charge pump circuit at LQFP128
57	28		PC.0 / MCLKO	**I/O**	General purpose digital I/O pin / Module clock output pin
			SPI0_SS0	**I/O**	SPI0 1st slave select pin
			I2S_LRCLK	**I/O**	I2S left right channel clock
			SC1_CLK	**O**	SmartCard1 clock pin(SC1_UART_TXD)
			LCD_DH1	**O**	LCD externl capacitor pin of charge pump circuit at LQFP64
			LCD_DH1	**O**	LCD externl capacitor pin of charge pump circuit at LQFP128
58			PE.6	**I/O**	General purpose digital I/O pin
59	29		LCD_VLCD	**AO**	LCD power supply pin
60					NC

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
			EBI_MCLK	O	EBI external clock output pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			LCD_SEG28	O	LCD segment output 28 at LQFP64
76	37		PA.15	I/O	General purpose digital I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output
			I2S_MCLK	O	I^2S master clock output pin
			TC3	I	Timer3 capture input
			SC0_PWR	O	SmartCard0 Power pin
			UART0_TXD	O	UART0 Data transmitter output pin
			LCD_SEG27	O	LCD segment output 27 at LQFP64
77	38		PA.14	I/O	General purpose digital I/O pin
			PWM0_CH2	I/O	PWM0 Channel2 output
			EBI_AD15	I/O	EBI Address/Data bus bit15
			TC2	I	Timer2 capture input
			UART0_RXD	I	UART0 Data receiver input pin
			LCD_SEG26	O	LCD segment output 26 at LQFP64
78	39		PA.13	I/O	General purpose digital I/O pin
			PWM0_CH1	I/O	PWM0 Channel1 output
			EBI_AD14	I/O	EBI Address/Data bus bit14
			TC1	I	Timer1 capture input
			I2C0_SCL	I/O	I^2C0 clock pin
			LCD_SEG25	O	LCD segment output 25 at LQFP64
79	40		PA.12	I/O	General purpose digital I/O pin
			PWM0_CH0	I/O	PWM0 Channel0 output
			EBI_AD13	I/O	EBI Address/Data bus bit13
			TC0	I	Timer0 capture input
			I2C0_SDA	I/O	I^2C0 data I/O pin
			LCD_SEG24	O	LCD segment output 24 at LQFP64
80	41		ICE_DAT	I/O	Serial Wired Debugger Data pin
			PF.0	I/O	General purpose digital I/O pin

3.4.3 NuMicro™ Nano120 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128	LQFP 64	LQFP 48			
1			PE.13	**I/O**	General purpose digital IO pin
2	1		PB.14	**I/O**	General purpose digital IO pin
			INT0	**I**	External interrupt0 input pin
			SC2_CD	**I**	SmartCard2 card detect
			SPI2_SS1	**I/O**	SPI2 2nd slave select pin
3	2		PB.13	**I/O**	General purpose digital IO pin
			EBI_AD1	**I/O**	EBI Address/Data bus bit1
4	3	1	PB.12	**I/O**	General purpose digital IO pin
			EBI_AD0	**I/O**	EBI Address/Data bus bit0
			FCLKO	**O**	Frequency Divider output pin
5					NC
6	4	2	X32O	**O**	External 32.768 kHz crystal output pin
7	5	3	X32I	**I**	External 32.768 kHz crystal input pin
8					NC
9	6	4	PA.11	**I/O**	General purpose digital IO pin
			I2C1_SCL	**I/O**	I2C 1 clock pin
			EBI_nRD	**O**	EBI read enable output pin
			SC0_RST	**O**	SmartCard0 RST pin
			SPI2_MOSI0	**I/O**	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	PA.10	**I/O**	General purpose digital IO pin
			I2C1_SDA	**I/O**	I2C 1 data I/O pin
			EBI_nWR	**O**	EBI write enable output pin
			SC0_PWR	**O**	SmartCard0 Power pin
			SPI2_MISO0	**I/O**	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	PA.9	**I/O**	General purpose digital IO pin
			I2C0_SCL	**I/O**	I2C 0 clock pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			SPI2_CLK	**I/O**	SPI2 serial clock pin

3.4.4 NuMicro™ Nano130 Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
1			PE.13	I/O	General purpose digital I/O pin
			LCD_SEG27	O	LCD segment output 27 at LQFP128
2	1		PB.14	I/O	General purpose digital I/O pin
			INT0	I	External interrupt0 input pin
			SC2_CD	I	SmartCard2 card detect
			SPI2_SS1	I/O	SPI2 2nd slave select pin
			LCD_SEG12	O	LCD segment output 12 at LQFP64
			LCD_SEG26	O	LCD segment output 26 at LQFP128
3	2		PB.13	I/O	General purpose digital I/O pin
			EBI_AD1	I/O	EBI Address/Data bus bit1
			LCD_SEG11	O	LCD segment output 11 at LQFP64
			LCD_SEG25	O	LCD segment output 25 at LQFP128
4	3		PB.12	I/O	General purpose digital I/O pin
			EBI_AD0	I/O	EBI Address/Data bus bit0
			FCLKO	O	Frequency Divider output pin
			LCD_SEG10	O	LCD segment output 10 at LQFP64
			LCD_SEG24	O	LCD segment output 24 at LQFP128
5					NC
6	4		X32O	O	External 32.768 kHz crystal output pin
7	5		X32I	I	External 32.768 kHz crystal input pin
8					NC
9	6		PA.11	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I2C1 clock pin
			EBI_nRD	O	EBI read enable output pin
			SC0_RST	O	SmartCard0 RST pin
			SPI2_MOSI0	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
			LCD_SEG9	O	LCD segment output 9 at LQFP64
			LCD_SEG23	O	LCD segment output 23 at LQFP128
10	7		PA.10	I/O	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin			
70			PC.13	I/O	General purpose digital I/O pin
			SPI1_MOSI1	I/O	SPI1 2nd MOSI (Master Out, Slave In) pin
			PWM1_CH1	O	PWM1 Channel1 output
			SNOOPER	I	Snooper pin
			INT1	I	External interrupt 1 input pin
			I2C0_SCL	O	I2C0 clock pin
71			PC.12	I/O	General purpose digital I/O pin
			SPI1_MISO1	I/O	SPI1 2nd MISO (Master In, Slave Out) pin
			PWM1_CH0	O	PWM1 Channel0 output
			INT0	I	External interrupt0 input pin
			I2C0_SDA	I/O	I2C0 data I/O pin
72	33		PC.11	I/O	General purpose digital I/O pin
			SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
			UART1_TXD	O	UART1 Data transmitter output pin
			LCD_SEG31	O	LCD segment output 31 at LQFP64
73	34		PC.10	I/O	General purpose digital I/O pin
			SPI1_MISO0	I/O	SPI1 1st MISO (Master In, Slave Out) pin
			UART1_RXD	I	UART1 Data receiver input pin
			LCD_SEG30	O	LCD segment output 30 at LQFP64
74	35		PC.9	I/O	General purpose digital I/O pin
			SPI1_CLK	I/O	SPI1 serial clock pin
			I2C1_SCL	I/O	I2C1 clock pin
			LCD_SEG29	O	LCD segment output 29 at LQFP64
75	36		PC.8	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			EBI_MCLK	O	EBI external clock output pin
			I2C1_SDA	I/O	I2C1 data I/O pin
			LCD_SEG28	O	LCD segment output 28 at LQFP64
76	37		PA.15	I/O	General purpose digital I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output

3.5 Nano100 Block Diagram

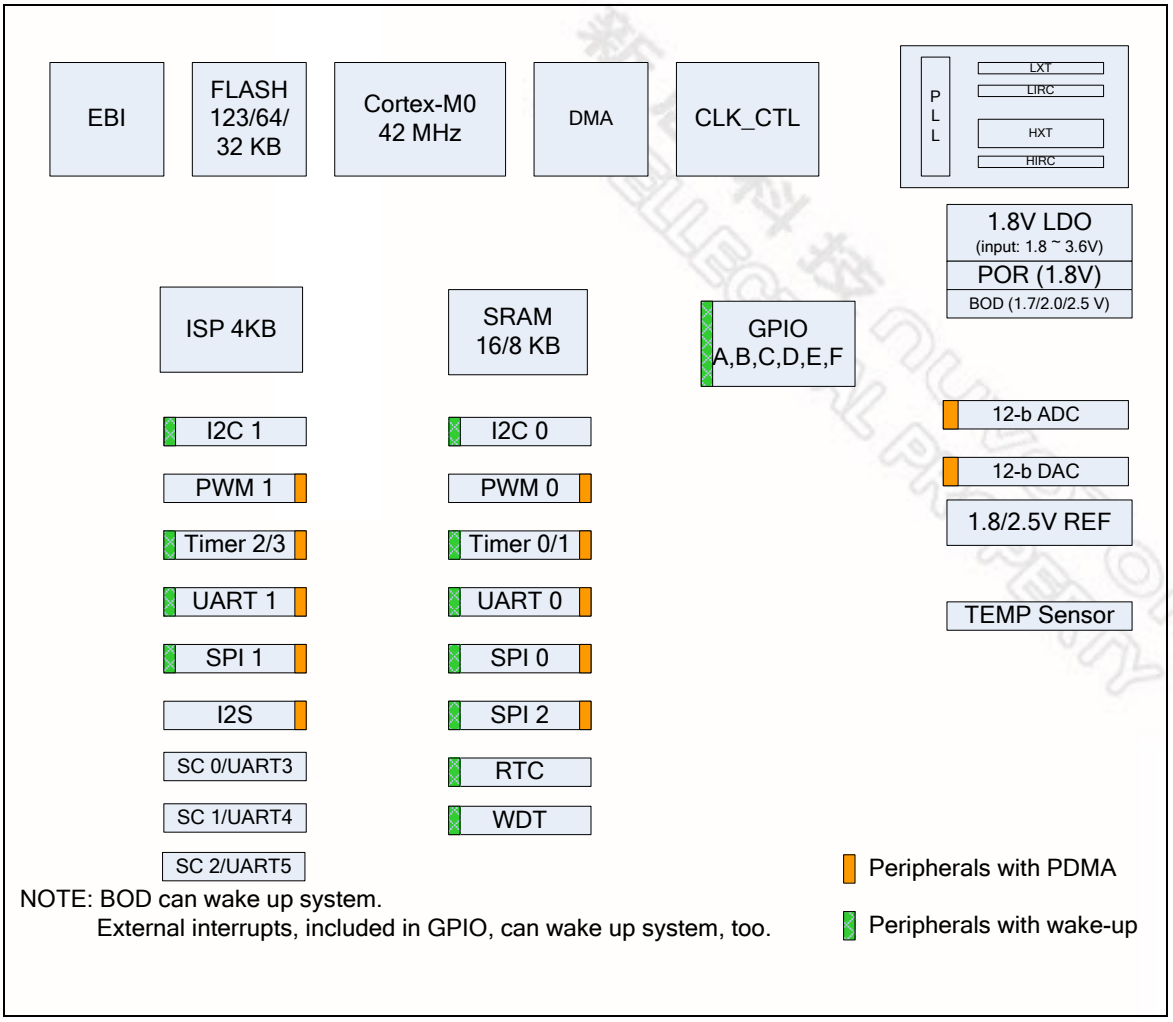
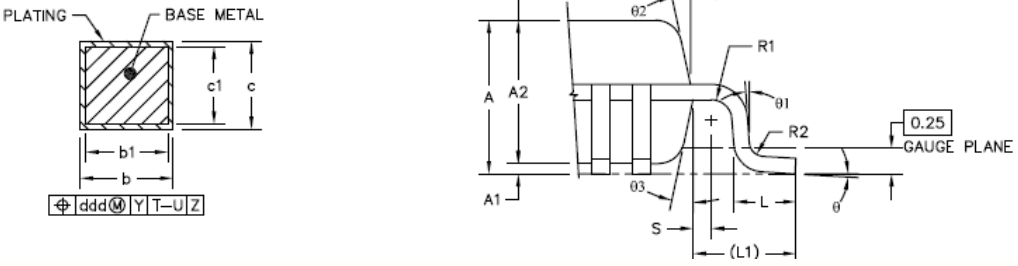


Figure 4-12 NuMicro™ Nano100 Block Diagram

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



5 REVISION HISTORY

Date	Revision	Description
2012.10.11	1.00	Initial release
2012.12.11	1.01	1. Added SmartCard UART mode description in Pin Description. 2. Unified the abbreviation (TMR) in the Timer Controller section. 3. Modified the specifications of external input clock. 4. Added LCD COM4 and COM5 description for each pin description and diagram. 5. Updated the ADC enabled by timer event description in the ADC section. 6. Changed Timer0/1 Ch0/1 to Timer x (x=0, 1, 2, 3) in the Timer Controller section.
2013.03.05	1.05	1. Corrected the pin descriptions in section 3.4.
2013.05.28	1.06	1. Updated the Nano110 LQFP128-pin diagram in section 3.3.2. 2. Updated “12 MHz OSC has 2 % deviation within all temperarure range” in sections 2.1 to 2.4. 3. Added Nano110RC2BN to the Nano110 LCD Line Selection Guide.
2013.12.04	1.07	1. Updated Nano100 series selection code in section 3.1. 2. Added the Nano100 QFN48 package in section 3.2. 3. Added a note that “Output voltage for ADC/LCD shared pins cannot be higher than VDD because these pins are without 5V tolerance.” for pin description in section 3.4.
2014.06.17	1.08	1. Modified the pin description in section 3.4.