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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 42MHz |
| Connectivity | I²C, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 7x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano120se3bn |

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# 1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM® Cortex™-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded Flash and 8K/16K-byte embedded SRAM. Integrating LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed function, RTC, 12-bit SAR ADC, 12-bit DAC and provides high performance connectivity peripheral interfaces such as UART, SPI, $I^2C$, $I^2S$, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection (ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 12- channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2x$I^2C$, $I^2S$, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano110 LCD line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates LCD 4x40 or 6x38 (COM/Segment). RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2x$I^2C$, $I^2S$, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano110 LCD line supports Brown-out Detector,

# 2 FEATURES

The equipped features are dependent on the product line and their sub products.

## 2.1 Nano100 Features – Base Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access
  - 64K/32K/123K bytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 8 channels: one VDMA channel, 6 PDMA channels and one CRC channel
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode

- Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
- Interrupt or reset selectable when watchdog time-out
- Wake system up from Power-down mode

- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
- PWM/Capture
  - Supports 2 PWM modules, each has two 16-bit PWM generators
  - Provides eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
  - Supports Capture interrupt
- UART
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up from Power-down mode
- SPI
  - Up to three sets of SPI controller

- ADC
  - 12-bit SAR ADC up to 2Msps conversion rate
  - Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
  - Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to enable ADC
- DAC
  - 12-bit monotonic output with 400K conversion rate
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Synchronized update capability for two DACs (group function)
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports
  - Separates receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Reset (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal

- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire, no slave select signal, bi-direction interface
- Wake system up from Power-down mode

- $I^2C$
  - Up to two sets of $I^2C$ device
  - Master/Slave up to 1Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the $I^2C$ interrupt if the $I^2C$ bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
- $I^2S$
  - Interface with external audio CODEC
  - Operated as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports $I^2S$ and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two PDMA requests: one for transmitting and the other for receiving

- ADC
  - 12-bit SAR ADC up to 2Msps conversion rate
  - Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3).
  - Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD
  - Supports single scan, single cycle scan, and continuous scan modes
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC
- DAC
  - 12-bit monotonic output with 400K conversion rate
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Synchronized update capability for two DACs (group function)
  - Supports up to four timer time-out event (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports
  - Separates receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Reset (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal

## 2.4 Nano130 Features – Advanced Line

- Core
  - ARM® Cortex™-M0 core running up to 42 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 42 MHz with zero wait state for discontinuous address read access.
  - 64K/32K/123K bytes application program memory (APROM)
  - 4KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 8 channels: one VDMA channel,6 PDMA channels, and one CRC 25egiste
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12MHz OSC, can be trimmed to 0.25% deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 120 MHz, for high performance system operation and USB application (48 MHz).
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance (except ADC and DAC shared pins)
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Supports internal trigger event to ADC, DAC and PDMA module
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source is from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6ms ~ 26sec (depends on clock source)
  - Interrupt or reset selectable on watchdog time-out

- Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
- Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
- Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD
- Single scan/single cycle scan/continuous scan
- Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection (comparator function)
- Conversion start by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- DAC
  - 12-bit monotonic output with 400K conversion rate
  - Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
  - Synchronized update capability for two DACs (group function)
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion
- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to three ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Reset (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports stop clock level and clock stop (clock keep) function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card is removed
  - Support UART mode (Half Duplex)
- LCD

## 3.2 NuMicro™ Nano100 Products Selection Guide

### 3.2.1 NuMicro™ Nano100 Base Line Selection Guide

| Part No. | Flash (Kbytes) | SRAM (Kbytes) | Data Flash | ISP ROM (Kbytes) | I/O | Timer (32-bit) | Connectivity | | | | I2S | PWM (16-bit | ADC (12-bit) | RTC | EBI | IRC 10KHz 12MHz | PDMA | LCD | DAC (12-bit) | ISO-7816-3 | ISP ICP | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | UART | SPI | I2C | USB | | | | | | | | | | | | |
| NANO100NC2BN | 32K | 8K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 0 | 7 | V | - | V | 8 | - | 2 | 2 | V | QFN48* |
| NANO100ND2BN | 64K | 8K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | QFN48* |
| NANO100ND3BN | 64K | 16K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | QFN48* |
| NANO100NE3BN | 128K | 16K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | QFN48* |
| NANO100LC2BN | 32K | 8K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO100LD2BN | 64K | 8K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO100LD3BN | 64K | 16K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO100LE3BN | 128K | 16K | Configurable | 4K | up to 38 | 4x32-bit | 4 | 3 | 2 | - | 1 | 6 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO100SC2BN | 32K | 8K | Configurable | 4K | up to 52 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO100SD2BN | 64K | 8K | Configurable | 4K | up to 52 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO100SD3BN | 64K | 16K | Configurable | 4K | up to 52 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO100SE3BN | 128K | 16K | Configurable | 4K | up to 52 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO100KD3BN | 64K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | - | 2 | 3 | V | LQFP128 |
| NANO100KE3BN | 128K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | - | 2 | 3 | V | LQFP128 |

QFN*48* : 7x7, pitch 0.5 mm ; LQFP48 : 7x7, pitch 0.5 mm ; LQFP64 : 7x7, pitch 0.4 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-1 Nano100 Base Line Selection Table

### 3.2.2 NuMicro™ Nano110 LCD Line Selection Guide

| Part No. | Flash (Kbytes) | SRAM (Kbytes) | Data Flash | ISP ROM (Kbytes) | I/O | Timer (32-bit) | Connectivity | | | | I2S | PWM (16-bit | ADC (12-bit) | RTC | EBI | IRC 10KHz 12MHz | PDMA | LCD | DAC (12-bit) | ISO-7816-3 | ISP ICP | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | UART | SPI | I2C | USB | | | | | | | | | | | | |
| NANO110SC2BN | 32K | 8K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64 |
| NANO110SD2BN | 64K | 8K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64 |
| NANO110SD3BN | 64K | 16K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64 |
| NANO110SE3BN | 128K | 16K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64 |
| NANO110RC2BN | 32K | 8K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64* |
| NANO110RD2BN | 64K | 8K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64* |
| NANO110RD3BN | 64K | 16K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64* |
| NANO110RE3BN | 128K | 16K | Configurable | 4K | up to 51 | 4x32-bit | 5 | 3 | 2 | - | 1 | 7 | 7 | V | - | V | 8 | 4x31, 6x29 | 2 | 3 | V | LQFP64* |
| NANO110KC2BN | 32K | 8K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | 4x40, 6x38 | 2 | 3 | V | LQFP128 |
| NANO110KD2BN | 64K | 8K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | 4x40, 6x38 | 2 | 3 | V | LQFP128 |
| NANO110KD3BN | 64K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | 4x40, 6x38 | 2 | 3 | V | LQFP128 |
| NANO110KE3BN | 128K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | - | 1 | 8 | 12 | V | V | V | 8 | 4x40, 6x38 | 2 | 3 | V | LQFP128 |

LQFP64 : 7x7, pitch 0.4 mm ; LQFP64* : 10x10, pitch 0.5 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-2 Nano110 LCD Line Selection Table

### 3.2.3 NuMicro™ Nano120 USB Connectivity Line Selection Guide

| Part No. | Flash (Kbytes) | SRAM (Kbytes) | Data Flash | ISP ROM (Kbytes) | I/O | Timer (32-bit) | Connectivity | | | | I2S | PWM (16-bit | ADC (12-bit) | RTC | EBI | IRC 10KHz 12MHz | PDMA | LCD | DAC (12-bit) | ISO-7816-3 | ISP ICP | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | UART | SPI | I2C | USB | | | | | | | | | | | | |
| NANO120LC2BN | 32K | 8K | Configurable | 4K | up to 34 | 4x32-bit | 4 | 3 | 2 | 1 | 1 | 4 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO120LD2BN | 64K | 8K | Configurable | 4K | up to 34 | 4x32-bit | 4 | 3 | 2 | 1 | 1 | 4 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO120LD3BN | 64K | 16K | Configurable | 4K | up to 34 | 4x32-bit | 4 | 3 | 2 | 1 | 1 | 4 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO120LE3BN | 128K | 16K | Configurable | 4K | up to 34 | 4x32-bit | 4 | 3 | 2 | 1 | 1 | 4 | 7 | V | - | V | 8 | - | 2 | 2 | V | LQFP48 |
| NANO120SC2BN | 32K | 8K | Configurable | 4K | up to 48 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO120SD2BN | 64K | 8K | Configurable | 4K | up to 48 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO120SD3BN | 64K | 16K | Configurable | 4K | up to 48 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO120SE3BN | 128K | 16K | Configurable | 4K | up to 48 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 7 | V | - | V | 8 | - | 2 | 3 | V | LQFP64 |
| NANO120KD3BN | 64K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 8 | V | V | V | 8 | - | 2 | 3 | V | LQFP128 |
| NANO120KE3BN | 128K | 16K | Configurable | 4K | up to 86 | 4x32-bit | 5 | 3 | 2 | 1 | 1 | 8 | 8 | V | V | V | 8 | - | 2 | 3 | V | LQFP128 |

LQFP48 : 7x7, pitch 0.5 mm ; LQFP64 : 7x7, pitch 0.4 mm ; LQFP128 : 14x14, pitch 0.4 mm

Table 3-3 Nano120 USB Connectivity Line Selection Table

3.3.1.2 NuMicro™ Nano100 LQFP 64-pin

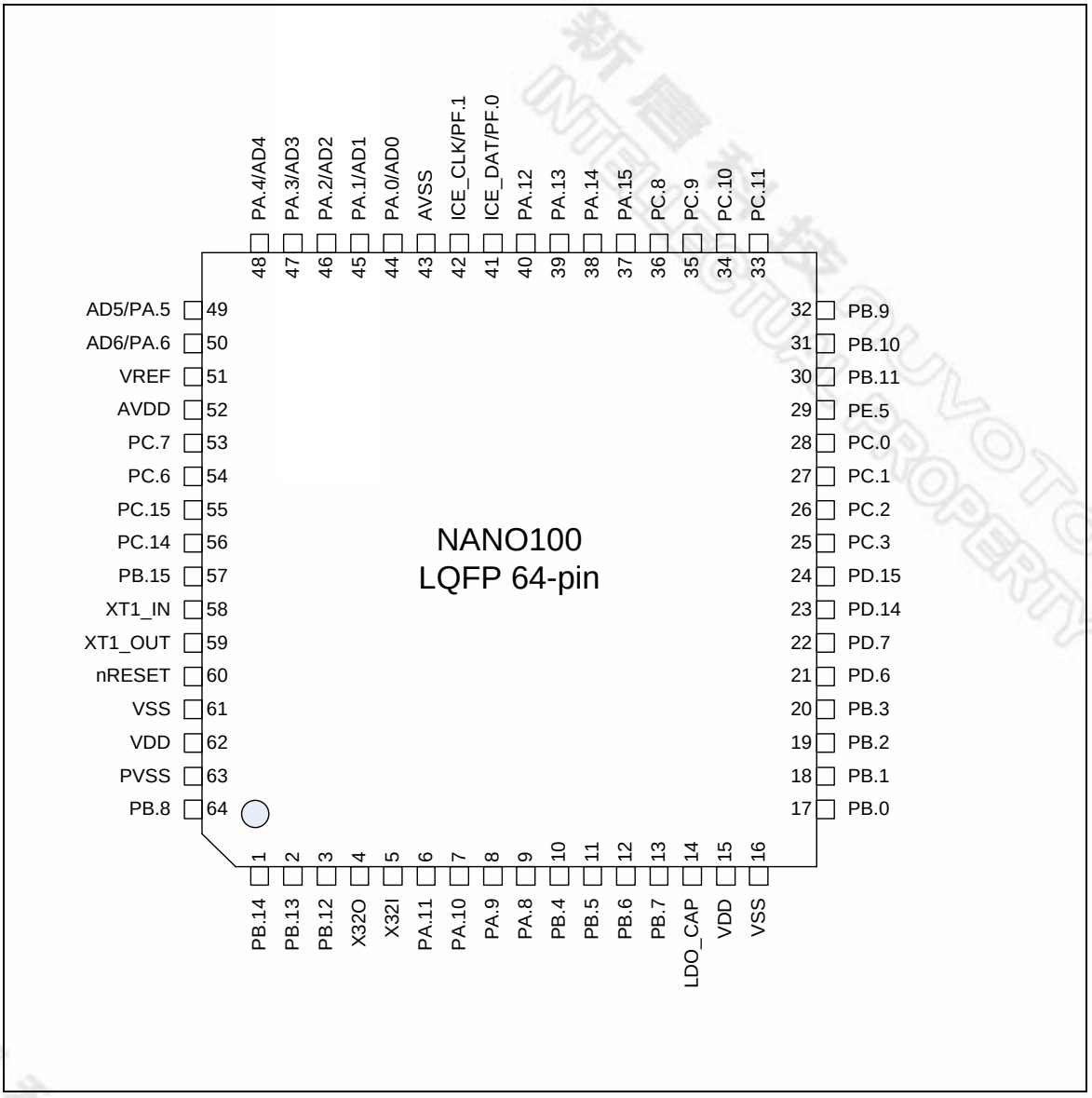



Figure 3-3 NuMicro™ Nano100 LQFP 64-pin Diagram

### 3.3.2 NuMicro™ Nano110 Pin Diagrams

#### 3.3.2.1 NuMicro™ Nano110 LQFP 128-pin

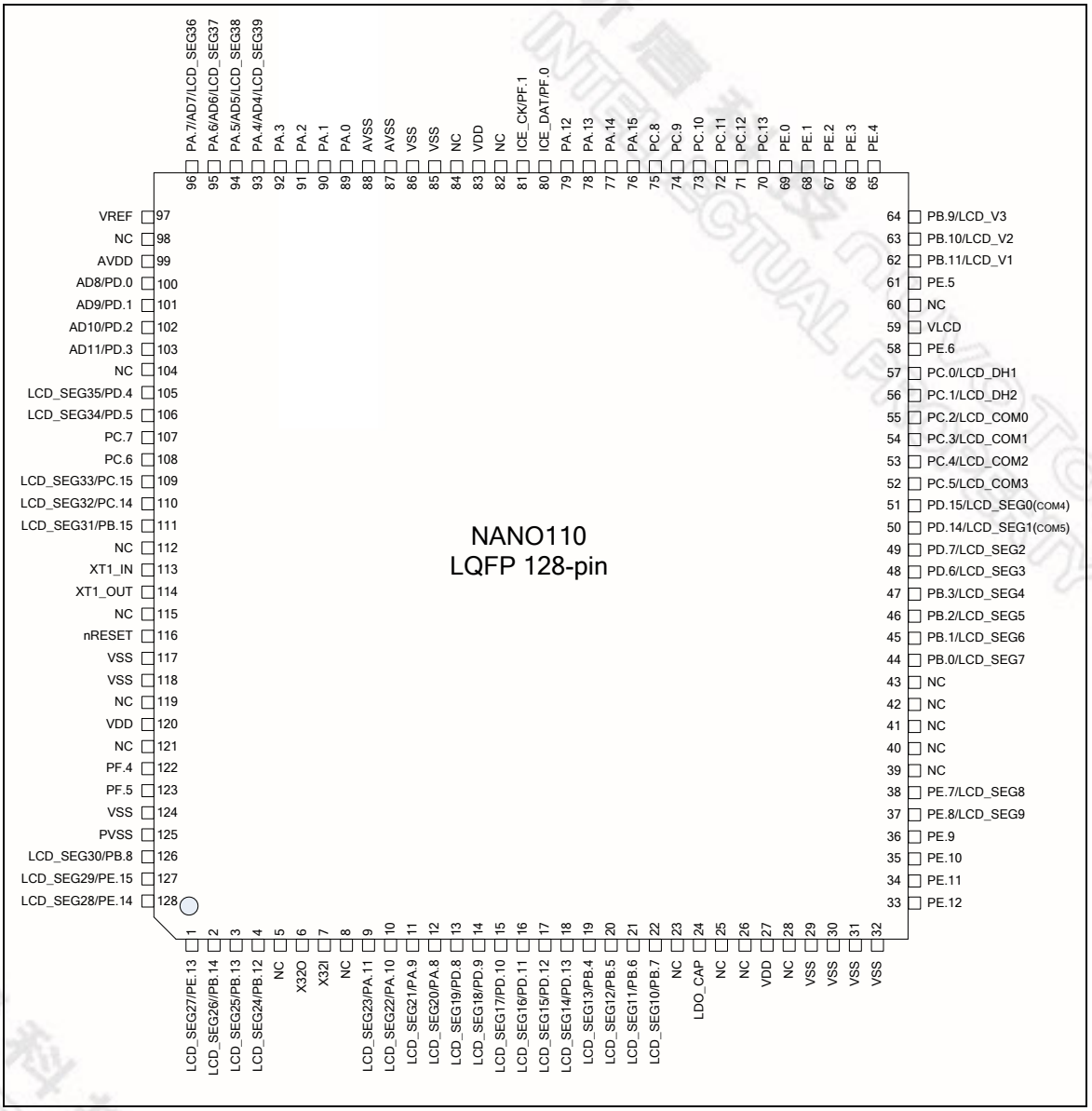



Figure 3-5 NuMicro™ Nano110 LQFP 128-pin Diagram

3.3.3.2 NuMicro™ Nano120 LQFP 64-pin

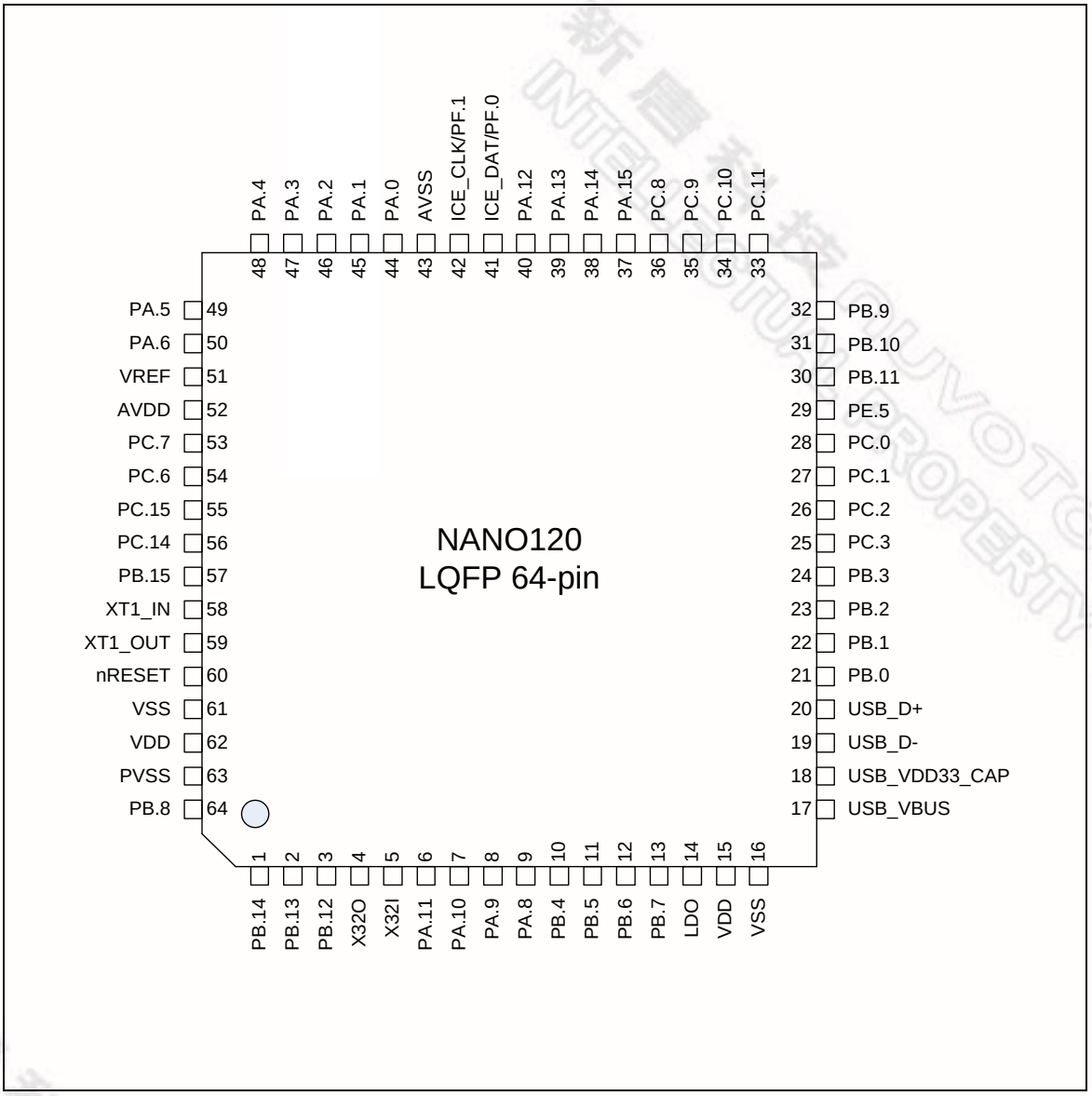



Figure 3-8 NuMicro™ Nano120 LQFP 64-pin Diagram

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 128-pin | LQFP 64-pin | LQFP/QFN 48-pin | | | |
| 61 | 29 | 21 | PE.5 | **I/O** | General purpose digital I/O pin |
| | | | PWM1_CH1 | **I/O** | PWM1 Channel1 output |
| 62 | 30 | 22 | PB.11 | **I/O** | General purpose digital I/O pin |
| | | | PWM1_CH0 | **I/O** | PWM1 Channel0 output |
| | | | TM3 | **O** | Timer3 external counter input |
| | | | SC2_DAT | **I/O** | SmartCard2 DATA pin(SC2_UART_RXD) |
| | | | SPI0_MISO0 | **I/O** | SPI0 1st MISO (Master In, Slave Out) pin |
| 63 | 31 | 23 | PB.10 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_SS1 | **I/O** | SPI0 2nd slave select pin |
| | | | TM2 | **O** | Timer2 external counter input |
| | | | SC2_CLK | **O** | SmartCard2 clock pin(SC2_UART_TXD) |
| | | | SPI0_MOSI0 | **I/O** | SPI0 1st MOSI (Master Out, Slave In) pin |
| 64 | 32 | 24 | PB.9 | **I/O** | General purpose digital I/O pin |
| | | | SPI1_SS1 | **I/O** | SPI1 2nd slave select pin |
| | | | TM1 | **O** | Timer1 external counter input |
| | | | SC2_RST | **O** | SmartCard2 RST pin |
| | | | INT0 | **I** | External interrupt0 input pin |
| 65 | | | PE.4 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_MOSI0 | **I/O** | SPI0 1st MOSI (Master Out, Slave In) pin |
| 66 | | | PE.3 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_MISO0 | **I/O** | SPI0 1st MISO (Master In, Slave Out) pin |
| 67 | | | PE.2 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_CLK | **I/O** | SPI0 serial clock pin |
| 68 | | | PE.1 | **I/O** | General purpose digital I/O pin. |
| | | | PWM1_CH3 | **I/O** | PWM1 Channel3 output |
| | | | SPI0_SS0 | **I/O** | SPI0 1st slave select pin |
| 69 | | | PE.0 | **I/O** | General purpose digital I/O pin |
| | | | PWM1_CH2 | **I/O** | PWM1 Channel2 output |
| | | | I2S_MCLK | **O** | $I^2S$ master clock output pin |
| 70 | | | PC.13 | **I/O** | General purpose digital I/O pin |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 128-pin | LQFP 64-pin | LQFP 48-pin | | | |
| 54 | 25 | | PC.3 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_MOSI0 | **I/O** | SPI0 1st MOSI (Master Out, Slave In) pin |
| | | | I2S_DO | **O** | I2S data output |
| | | | SC1_RST | **O** | SmartCard1 RST pin |
| | | | LCD_COM1 | **O** | LCD common output 1 at LQFP64 |
| | | | LCD_COM1 | **O** | LCD common output 1 at LQFP128 |
| 55 | 26 | | PC.2 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_MISO0 | **I/O** | SPI0 1st MISO (Master In, Slave Out) pin |
| | | | I2S_DI | **I** | I2S data input |
| | | | SC1_PWR | **O** | SmartCard1 PWR pin |
| | | | LCD_COM0 | **O** | LCD common output 0 at LQFP64 |
| | | | LCD_COM0 | **O** | LCD common output 0 at LQFP128 |
| 56 | 27 | | PC.1 | **I/O** | General purpose digital I/O pin |
| | | | SPI0_CLK | **I/O** | SPI0 serial clock pin |
| | | | I2S_BCLK | **I/O** | I2S bit clock pin |
| | | | SC1_DAT | **I/O** | SmartCard1 DATA pin(SC1_UART_RXD) |
| | | | LCD_DH2 | **O** | LCD externl capacitor pin of charge pump circuit at LQFP64 |
| | | | LCD_DH2 | **O** | LCD externl capacitor pin of charge pump circuit at LQFP128 |
| 57 | 28 | | PC.0 / MCLKO | **I/O** | General purpose digital I/O pin / Module clock output pin |
| | | | SPI0_SS0 | **I/O** | SPI0 1st slave select pin |
| | | | I2S_LRCLK | **I/O** | I2S left right channel clock |
| | | | SC1_CLK | **O** | SmartCard1 clock pin(SC1_UART_TXD) |
| | | | LCD_DH1 | **O** | LCD externl capacitor pin of charge pump circuit at LQFP64 |
| | | | LCD_DH1 | **O** | LCD externl capacitor pin of charge pump circuit at LQFP128 |
| 58 | | | PE.6 | **I/O** | General purpose digital I/O pin |
| 59 | 29 | | LCD_VLCD | **AO** | LCD power supply pin |
| 60 | | | | | NC |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 128-pin | LQFP 64-pin | LQFP 48-pin | | | |
| 128 | | | PE.14 | **I/O** | General purpose digital I/O pin |
| | | | LCD_SEG28 | **O** | LCD segment output 28 at LQFP128 |

**Note:**

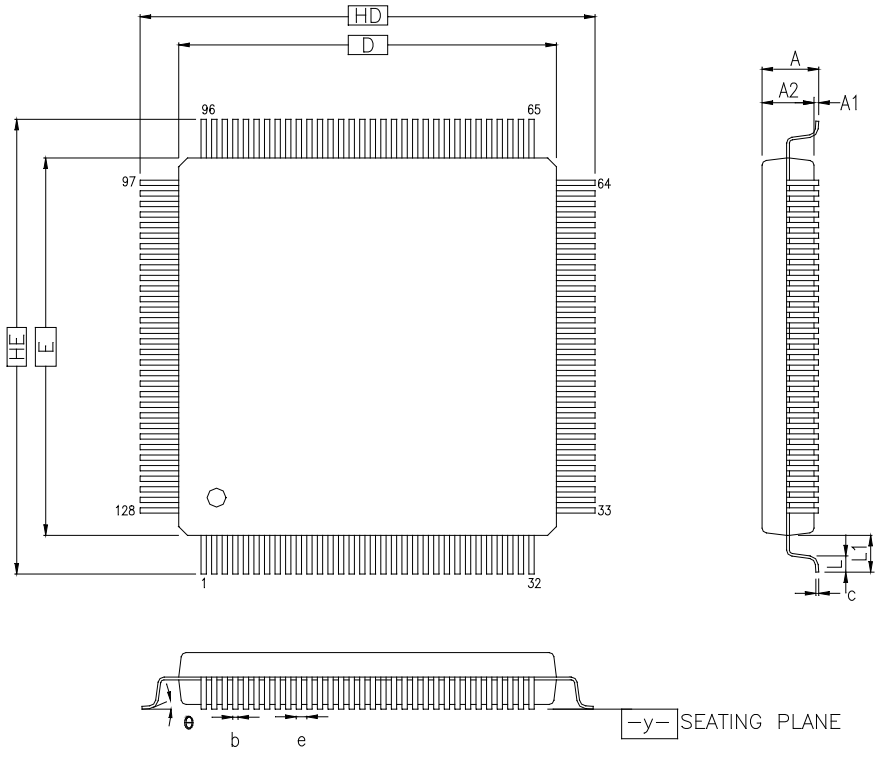
1. Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power;
2. * : Output voltage for ADC/LCD shared pins cannot be higher than VDD because these pins are without 5V tolerance.

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 128-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | SPI0_MISO0 | I/O | SPI0 1st MISO (Master In, Slave Out) pin |
| | | | LCD_V1 | O | LCD Unit voltage for LCD charge pump circuit at LQFP64 |
| | | | LCD_V1 | O | LCD Unit voltage for LCD charge pump circuit at LQFP128 |
| 63 | 31 | | PB.10 | I/O | General purpose digital I/O pin |
| | | | SPI0_SS1 | I/O | SPI0 2nd slave select pin |
| | | | TM2 | O | Timer2 external counter input |
| | | | SC2_CLK | O | SmartCard2 clock pin(SC2_UART_TXD) |
| | | | SPI0_MOSI0 | I/O | SPI0 1st MOSI (Master Out, Slave In) pin |
| | | | LCD_V2 | O | LCD driver biasing voltage at LQFP64 |
| | | | LCD_V2 | O | LCD driver biasing voltage at LQFP128 |
| 64 | 32 | | PB.9 | I/O | General purpose digital I/O pin |
| | | | SPI1_SS1 | I/O | SPI1 2nd slave select pin |
| | | | TM1 | O | Timer1 external counter input |
| | | | SC2_RST | O | SmartCard2 RST pin |
| | | | INT0 | I | External interrupt0 input pin |
| | | | LCD_V3 | O | LCD driver biasing voltage at LQFP64 |
| | | | LCD_V3 | O | LCD driver biasing voltage at LQFP128 |
| 65 | | | PE.4 | I/O | General purpose digital I/O pin |
| | | | SPI0_MOSI0 | I/O | SPI0 1st MOSI (Master Out, Slave In) pin |
| 66 | | | PE.3 | I/O | General purpose digital I/O pin |
| | | | SPI0_MISO0 | I/O | SPI0 1st MISO (Master In, Slave Out) pin |
| 67 | | | PE.2 | I/O | General purpose digital I/O pin |
| | | | SPI0_CLK | I/O | SPI0 serial clock pin |
| 68 | | | PE.1 | I/O | General purpose digital I/O pin |
| | | | PWM1_CH3 | I/O | PWM1 Channel3 output |
| | | | SPI0_SS0 | I/O | SPI0 1st slave select pin |
| 69 | | | PE.0 | I/O | General purpose digital I/O pin |
| | | | PWM1_CH2 | I/O | PWM1 Channel2 output |
| | | | I2S_MCLK | O | $I^2S$ master clock output pin |

| Pin No. | | | Pin Name | Pin Type | Description |
|---|---|---|---|---|---|
| LQFP 128-pin | LQFP 64-pin | LQFP 48-pin | | | |
| | | | EBI_AD5 | I/O | EBI Address/Data bus bit5 |
| | | | TC1 | I | Timer1 capture input |
| | | | PWM0_CH1 | O | PWM0 Channel1 output |
| | | | LCD_SEG17* | AO | LCD segment output 17 at LQFP64 |
| 108 | 54 | | PC.6 | I/O | General purpose digital I/O pin |
| | | | DA0_OUT | I | DAC0 output |
| | | | EBI_AD4 | I/O | EBI Address/Data bus bit4 |
| | | | TC0 | I | Timer0 capture input |
| | | | SC1_CD | | SmartCard1 card detect pin |
| | | | PWM0_CH0 | O | PWM0 Channel0 output |
| 109 | 55 | | PC.15 | I/O | General purpose digital I/O pin |
| | | | EBI_AD3 | I/O | EBI Address/Data bus bit3 |
| | | | TC0 | I | Timer0 capture input |
| | | | PWM1_CH2 | O | PWM1 Channel2 output |
| | | | LCD_SEG16 | AO | LCD segment output 16 at LQFP64 |
| | | | LCD_SEG33 | AO | LCD segment output 33 at LQFP128 |
| 110 | 56 | | PC.14 | I/O | General purpose digital I/O pin |
| | | | EBI_AD2 | I/O | EBI Address/Data bus bit2 |
| | | | PWM1_CH3 | I/O | PWM1 Channel3 output |
| | | | LCD_SEG15 | AO | LCD segment output 15 at LQFP64 |
| | | | LCD_SEG32 | AO | LCD segment output 32 at LQFP128 |
| 111 | 57 | | PB.15 | I/O | General purpose digital I/O pin |
| | | | INT1 | I | External interrupt1 input pin |
| | | | SNOOPER | I | Snooper pin |
| | | | SC1_CD | I | SmartCard1 card detect |
| | | | LCD_SEG14 | AO | LCD segment output 14 at LQFP64 |
| | | | LCD_SEG31 | AO | LCD segment output 31 at LQFP128 |
| 112 | | | | | NC |
| 113 | 58 | | XT1_IN | O | External 4~24 MHz crystal output pin |
| | | | PF.3 | I/O | General purpose digital I/O pin |

# 4 PACKAGE DIMENSIONS

## 4.1 LQFP128 (14x14x1.4 mm footprint 2.0 mm)




COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| HD | | 16.00 BSC. | | | 0.630 BSC. | |
| D | | 14.00 BSC. | | | 0.551 BSC. | |
| HE | | 16.00 BSC. | | | 0.630 BSC. | |
| E | | 14.00 BSC. | | | 0.551 BSC. | |
| b | 0.13 | 0.16 | 0.23 | 0.005 | 0.006 | 0.009 |
| e | | 0.40 BSC. | | | 0.016 BSC. | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | | 1.00 REF | | | 0.039 REF | |
| y | – | – | 0.1 | – | – | 0.004 |