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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	42MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I2S, LCD, POR, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano130se3bn

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM[®] Cortex[™]-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded Flash and 8K/16K-byte embedded SRAM. Integrating LCD 4x40 or 6x38 (COM/Segment), USB 2.0 full-speed function, RTC, 12-bit SAR ADC, 12-bit DAC and provides high performance connectivity peripheral interfaces such as UART, SPI, I²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection (ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM[®] Cortex[™]-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 12- channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano110 LCD line, an ultra-low power 32-bit microcontroller with the embedded ARM[®] Cortex[™]-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 42 MHz frequency with 32K/64K/128K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates LCD 4x40 or 6x38 (COM/Segment). RTC, 12-channels 12-bit SAR ADC, 2-channels 12-bit DAC and provides high performance connectivity peripheral interfaces such as 2xUART, 2xSPI, 2xI²C, I²S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 3xISO-7816-3 for Smart card. The Nano110 LCD line supports Brown-out Detector,

Watchdog Timer

- Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
- ♦ Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
- Interrupt or reset selectable when watchdog time-out
- ♦ Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
 - ◆ 6-bit down counter and 6-bit compare value to make the window period flexible
 - ♦ Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

RTC

- Supports software compensation by setting frequency compensate register (FCR)
- Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
- Supports Alarm registers (second, minute, hour, day, month, year)
- ♦ Selectable 12-hour or 24-hour mode
- ◆ Automatic leap year recognition
- ◆ Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Wake system up from Power-down mode
- Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers

PWM/Capture

- ◆ Supports 2 PWM modules, each has two 16-bit PWM generators
- Provides eight PWM outputs or four complementary paired PWM outputs
- ◆ Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
- ♦ (Shared with PWM timers) with eight 16-bit digital capture timers provides eight rising/ falling/both capture inputs.
- Supports One-shot and Continuous mode
- Supports Capture interrupt

UART

- Up to two 16-byte FIFO UART controllers
- UART ports with flow control (TX, RX, CTSn and RTSn)
- ◆ Supports IrDA (SIR) function
- Supports LIN function
- Supports RS-485 9 bit mode and direction control.
- Programmable baud rate generator
- Supports PDMA mode

- Supports hardware warm reset sequence process
- ◆ Supports hardware deactivation sequence process
- ◆ Supports hardware auto deactivation sequence when detect the card is removal
- ◆ Supports UART mode (Half Duplex)
- EBI (External bus interface) support
 - ♦ Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
 - ◆ Supports 8bit/16bit data width
 - ♦ Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1°C resolution
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40 °C ~85 °C
- Packages:
 - All Green package (RoHS)
 - ◆ LQFP 128-pin(14x14) / 64-pin(7x7) / 48-pin(7x7) / QFN 48-pin(7x7)

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UART

- Up to two 16-byte FIFO UART controllers
- ◆ UART ports with flow control (TX, RX, CTSn and RTSn)
- Supports IrDA (SIR) function
- Supports LIN function
- Supports RS-485 9 bit mode and direction control (Low Density Only)
- Programmable baud rate generator
- Supports PDMA mode
- Wake system up from Power-down mode
- SPI
 - Up to three sets of SPI controller

- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- ◆ Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- ◆ Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- ◆ Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- ◆ Supports three wire mode, no slave select signal, bi-direction interface
- ♦ Wake system up from Power-down mode
- I²C
 - Up to two sets of I²C device
 - Master/Slave up to 1Mbit/s
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master)
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
 - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
 - ♦ Built-in 14-bit time-out counter requestING the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
 - ◆ Programmable clocks allow versatile rate control
 - Supports 7-bit addressing mode
 - ◆ Supports multiple address recognition (four slave address with mask option)
- ullet I^2S
 - ◆ Interface with external audio CODEC
 - Operated as either Master or Slave mode
 - ◆ Capable of handling 8, 16, 24 and 32 bit word sizes
 - Supports Mono and stereo audio data
 - Supports I²S and MSB justified data format
 - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
 - Generates interrupt requests when buffer levels cross a programmable boundary
 - Supports two PDMA requests: one for transmitting and the other for receiving

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2.3 Nano120 Features – USB Connectivity Line

- Core
 - ◆ ARM[®] Cortex[™]-M0 core running up to 42 MHz
 - ♦ One 24-bit system timer
 - Supports Low Power Sleep mode
 - ◆ Single-cycle 32-bit hardware multiplier
 - ♦ NVIC for the 32 interrupt inputs, each with 4-levels of priority
 - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
 - ♦ Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
 - Runs up to 42 MHz with zero wait state for discontinuous address read access.
 - ♦ 64K/32K/123K bytes application program memory (APROM)
 - ◆ 4KB in system programming (ISP) loader program memory (LDROM)
 - Programmable data flash start address and memory size with 512 bytes page erase unit
 - ◆ In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
 - ♦ 16K/8K bytes embedded SRAM
 - Supports PDMA mode
- DMA: Support 8 channels: one VDMA channel, 6 PDMA channels, and one CRC channel
 - ♦ VDMA
 - Memory-to-memory transfer
 - Supports block transfer with stride
 - Supports word/half-word/byte boundary address
 - Supports address direction: increment and decrement
 - PDMA
 - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
 - Supports word boundary address
 - Supports word alignment transfer length in memory-to-memory mode
 - Supports word/half-word/byte alignment transfer length in peripheral-tomemory and memory-to-peripheral mode
 - Supports word/half-word/byte transfer data width from/to peripheral
 - Supports address: increment, fixed, and wrap around
 - ◆ CRC

- ◆ Up to 12-ch single-ended input from external pin (PA.0 ~ PA.7 and PD.0 ~ PD.3)
- ♦ Six internal channels from DAC0, DAC1, internal reference voltage (Int_VREF), Temperature sensor, AVDD, and AVSS.
- Supports three reference voltage sources from VREF pin, internal reference voltage (Int VREF), and AVDD
- Single scan/single cycle scan/continuous scan
- ◆ Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection (comparator function)
- Conversion start by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

DAC

- 12-bit monotonic output with 400K conversion rate
- Supports three reference voltage sources from VREF pin, internal reference voltage (Int_VREF), and AVDD.
- Synchronized update capability for two DACs (group function)
- ◆ Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3), software or PDMA to trigger DAC to conversion

SmartCard (SC)

- ◆ Compliant to ISO-7816-3 T=0, T=1
- ♦ Supports up to three ISO-7816-3 ports
- Separates receive/transmit 4 bytes entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- ◆ Programmable guard time selection (11 ETU ~ 266 ETU)
- ◆ A 24-bit and two 8-bit time-out counter for Answer to Reset (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports stop clock level and clock stop (clock keep) function
- ◆ Supports transmitter and receiver error retry and error limit function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detecting the card is removed
- Support UART mode (Half Duplex)
- LCD

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3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ Nano100 Series Selection Code

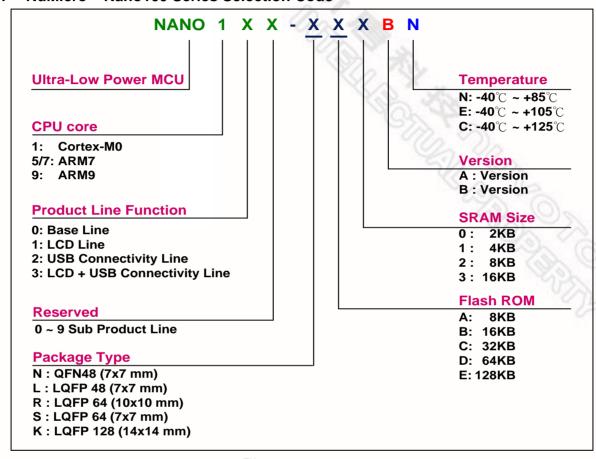


Figure 3-1 NuMicro[™] Nano100 Series Selection Code

3.3.2 NuMicro™ Nano110 Pin Diagrams

3.3.2.1 NuMicro™ Nano110 LQFP 128-pin

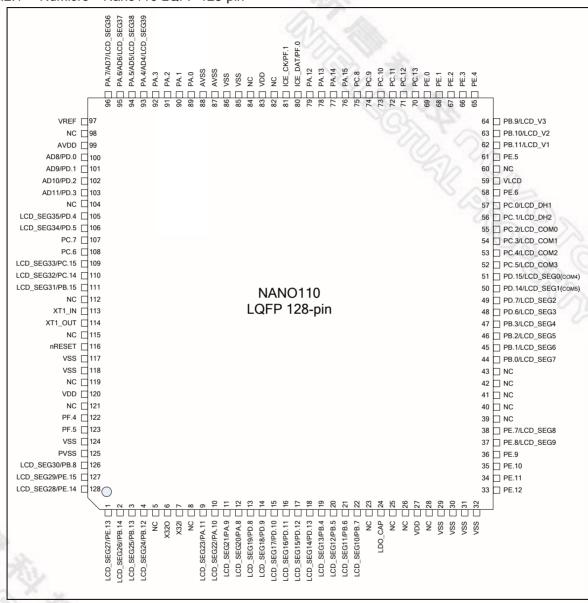


Figure 3-5 NuMicro[™] Nano110 LQFP 128-pin Diagram

	Pin No.		Din		
LQFP 128-pin	LQFP 64-pin	LQFP/QFN 48-pin	Pin Name	Pin Type	Description
			AD7	Al	ADC analog input7
			EBI_AD6	I/O	EBI Address/Data bus bit6
			TC2	I	Timer2 capture input
			SC2_DAT	I/O	SmartCard2 DATA pin(SC2_UART_RXD)
			PWM0_CH2	0	PWM0 Channel2 output
97	51	39	VREF	AP	Voltage reference input for ADC
98					NC
99	52	40	AVDD	AP	Power supply for internal analog circuit
			PD.0	I/O	General purpose digital I/O pin
			UART1_RXD	ı	UART1 Data receiver input pin
100			SPI2_SS0	I/O	SPI2 1 st slave select pin
			SC1_CLK	0	SmartCard1 clock pin(SC1_UART_TXD)
			AD8	Al	ADC analog input8
			PD.1	I/O	General purpose digital I/O pin
			UART1_TXD	0	UART1 Data transmitter output pin
101			SPI2_CLK	I/O	SPI2 serial clock pin
			SC1_DAT	I/O	SmartCard1 DATA pin(SC1_UART_RXD).
			AD9	Al	ADC analog input9
			PD.2	I/O	General purpose digital I/O pin
			UART1_RTSn	0	UART1 Request to Send output pin
102			I2S_LRCLK	I/O	I ² S left right channel clock
102			SPI2_MISO0	I/O	SPI2 1st MISO (Master In, Slave Out) pin
			SC1_PWR	0	SmartCard1 Power pin
			AD10	Al	ADC analog input10
			PD.3	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
103			I2S_BCLK	I/O	I ² S bit clock pin
103			SPI2_MOSI0	I/O	SPI2 1 st MOSI (Master Out, Slave In) pin
			SC1_RST	0	SmartCard1 RST pin
			AD11	Al	ADC analog input11

		Pin No.				
VSS			-	Pin Name	Pin Type	Description
31	29	16		VSS	Р	Ground
VSS	30			VSS	Р	Ground
PE.12 I/O General purpose digital I/O pin	31			vss	Р	Ground
Second S	32			vss	Р	Ground
UART1_CTSn	22			PE.12	I/O	General purpose digital I/O pin
34	33			UART1_CTSn	I	UART1 Clear to Send input pin
UART1_RTSn O	24			PE.11	I/O	General purpose digital I/O pin
Section Sect	34			UART1_RTSn	0	UART1 Request to Send output pin
UART1_TXD O UART1 Data transmitter output pin	25			PE.10	I/O	General purpose digital I/O pin
Section Sect	33			UART1_TXD	0	UART1 Data transmitter output pin
UART1_RXD	26			PE.9	I/O	General purpose digital I/O pin
CD_SEG9 O LCD segment output 9 at LQFP128	30			UART1_RXD	I	UART1 Data receiver input pin
LCD_SEG9	37			PE.8	I/O	General purpose digital I/O pin
18	31			LCD_SEG9	0	LCD segment output 9 at LQFP128
LCD_SEG8	38			PE.7	I/O	General purpose digital I/O pin
40	30			LCD_SEG8	0	LCD segment output 8 at LQFP128
17	39					NC
17 PB.0 I/O General purpose digital I/O pin	40					NC
17 PB.0 I/O General purpose digital I/O pin	41					NC
PB.0	42					NC
17 UARTO_RXD I	43					NC
17 SPI1_MOSI0				PB.0	I/O	General purpose digital I/O pin
LCD_SEG1 O LCD_SEG1 O LCD segment output 1 at LQFP64 (or LD_COM5) LCD_SEG7 O LCD segment output 7 at LQFP128 PB.1 VO General purpose digital I/O pin UARTO_TXD O UARTO Data transmitter output pin				UART0_RXD	I	UART0 Data receiver input pin
LCD_SEG1	44	17	LCD SEC1 LCD segmi	SPI1_MOSI0	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
PB.1 I/O General purpose digital I/O pin UARTO_TXD O UARTO Data transmitter output pin				LCD segment output 1 at LQFP64 (or as LD_COM5)		
45 18 UARTO_TXD O UARTO Data transmitter output pin				LCD_SEG7	0	LCD segment output 7 at LQFP128
		_		PB.1	I/O	General purpose digital I/O pin
SPI1_MISO0 I/O SPI1 1 st MISO (Master In, Slave Out) pin	45	18		UART0_TXD	0	UARTO Data transmitter output pin
4 I I I I I I I I I I I I I I I I I I I				SPI1_MISO0	I/O	SPI1 1 st MISO (Master In, Slave Out) pin



	Pin No.					
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin	Pin Name	Pin Type	Description	
			LCD_SEG0	0	LCD segment output 0 at LQFP64 (or as LCD_COM4)	
			LCD_SEG6	0	LCD segment output 6 at LQFP128	
			PB.2	I/O	General purpose digital I/O pin	
			UART0_RTSn	0	UART0 Request to Send output pin	
46	19		EBI_nWRL	0	EBI low byte write enable output pin	
40	19		SPI1_CLK	I/O	SPI1 serial clock pin	
			LCD_COM3	0	LCD common output 3 at LQFP64	
			LCD_SEG5	0	LCD segment output 5 at LQFP128	
			PB.3	I/O	General purpose digital I/O pin	
			UART0_CTSn	I	UART0 Clear to Send input pin	
47	20	20		EBI_nWRH	0	EBI high byte write enable output pin
47	20		SPI1_SS0	I/O	SPI1 1 st slave select pin	
			LCD_COM2	0	LCD common output 2 at LQFP64	
			LCD_SEG4	0	LCD segment output 4 at LQFP128	
48	21		PD.6	I/O	General purpose digital I/O pin	
40	21		LCD_SEG3	0	LCD segment output 3 at LQFP128	
49	22		PD.7	I/O	General purpose digital I/O pin	
43	22		LCD_SEG2	0	LCD segment output 2 at LQFP128	
			PD.14	1/0	General purpose digital I/O pin	
50	23		LCD_SEG1	0	LCD segment output 1 at LQFP128 (or as LCD_COM5)	
			PD.15	I/O	General purpose digital I/O pin	
51	24		LCD_SEG0	0	LCD segment output 0 at LQFP128 (or as LCD_COM4)	
			PC.5	I/O	General purpose digital I/O pin	
52			SPI0_MOSI1	I/O	SPI0 2 nd MOSI (Master Out, Slave In) pin	
			LCD_COM3	0	LCD common output 3 at LQFP128	
			PC.4	I/O	General purpose digital I/O pin	
53			SPI0_MISO1	I/O	SPI0 2 nd MISO (Master In, Slave Out) pin	
			LCD_COM2	0	LCD common output 2 at LQFP128	



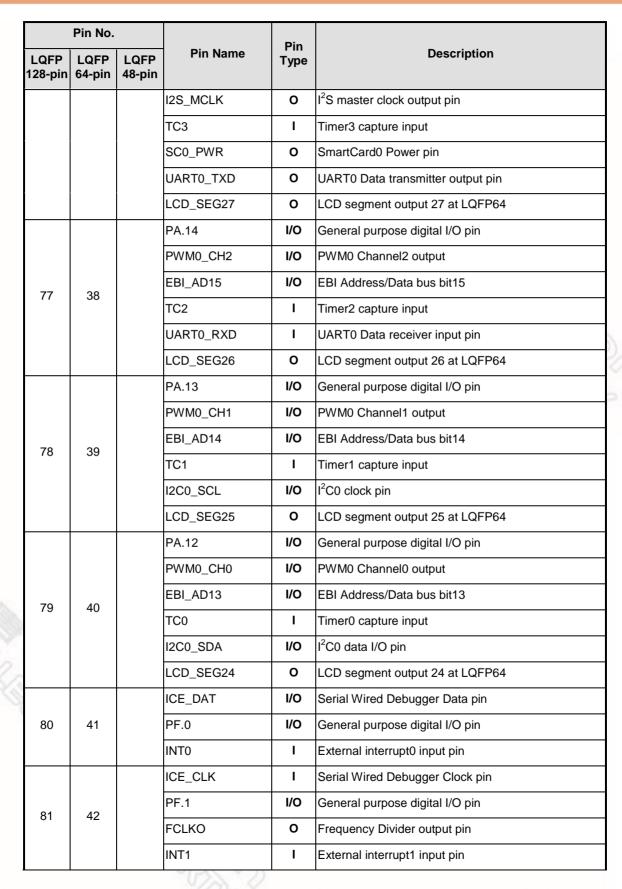
	Pin No.							
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin	Pin Name	Pin Type	Description			
			I2S_DO	0	I ² S data output			
			SPI2_MOSI1	I/O	SPI2 2 nd MOSI (Master Out, Slave In) pin			
			LCD_SEG34	AO	LCD segment output 34 at LQFP128			
			PC.7	I/O	General purpose digital I/O pin			
			DA1_OUT	AO	DAC 1 output			
407	5 0		EBI_AD5	I/O	EBI Address/Data bus bit5			
107	53		TC1	ı	Timer1 capture input			
			PWM0_CH1	0	PWM0 Channel1 output			
			LCD_SEG17*	AO	LCD segment output 17 at LQFP64			
			PC.6	I/O	General purpose digital I/O pin			
			DA0_OUT	ı	DAC0 output			
400	5 4		EBI_AD4	I/O	EBI Address/Data bus bit4			
108	54	54	54	54		TC0	ı	Timer0 capture input
			SC1_CD	I	SmartCard1 card detect pin			
			PWM0_CH0	0	PWM0 Channel0 output			
			PC.15	I/O	General purpose digital I/O pin			
			EBI_AD3	I/O	EBI Address/Data bus bit3			
400			TC0	ı	Timer0 capture input			
109	55		PWM1_CH2	0	PWM1 Channel2 output			
			LCD_SEG16	AO	LCD segment output 16 at LQFP64			
			LCD_SEG33	AO	LCD segment output 33 at LQFP128			
			PC.14	I/O	General purpose digital I/O pin			
			EBI_AD2	I/O	EBI Address/Data bus bit2			
110	56		PWM1_CH3	I/O	PWM1 Channel3 output			
			LCD_SEG15	AO	LCD segment output 15 at LQFP64			
			LCD_SEG32	AO	LCD segment output 32 at LQFP128			
			PB.15	I/O	General purpose digital I/O pin			
111	5 7		INT1	ı	External interrupt1 input pin			
111	57		SNOOPER	ı	Snooper pin			
			LCD_SEG14	AO	LCD segment output 14 at LQFP64			

	Pin No.				
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin	Pin Name	Pin Type	Description
			LCD_SEG31	AO	LCD segment output 31 at LQFP128
112					NC
440	50		XT1_IN	0	External 4~24 MHz crystal output pin
113	58		PF.3	I/O	General purpose digital I/O pin
114	<i>F</i> 0		XT1_OUT	I	External 4~24 MHz crystal input pin
114	59		PF.2	I/O	General purpose digital I/O pin
115					NC
116	60		nRESET	I	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
117	61		VSS	Р	Ground
118			VSS	Р	Ground
119					NC
120	62		VDD	Р	Power supply for I/O ports and LDO source for internal PLL and digital circuit
121					NC
122			PF.4	1/0	General purpose digital I/O pin
122			I2C0_SDA	1/0	I ² C0 data I/O pin
123			PF.5	1/0	General purpose digital I/O pin
123			I2C0_SCL	1/0	I ² C0 clock pin
124			VSS	Р	Ground
125	63		PVSS	Р	PLL Ground
			PB.8	I/O	General purpose digital I/O pin
	STADC	STADC	I	ADC external trigger input.	
		ТМО	тмо	I	Timer0 external counter input
126	64		INT0	I	External interrupt0 input pin
		SC2_PWR 0	0	SmartCard2 Power pin	
			LCD_SEG13	AO	LCD segment output 13 at LQFP64
			LCD_SEG30	AO	LCD segment output 30 at LQFP128
127			PE.15	I/O	General purpose digital I/O pin
121			LCD_SEG29	0	LCD segment output 29 at LQFP128



	Pin No.				
LQFP 128	LQFP 64	LQFP 48	Pin Name	Pin Type	Description
			PWM0_CH2	1/0	PWM0 Channel2 output
			EBI_AD15	1/0	EBI Address/Data bus bit15
			TC2	I	Timer 2 capture input
			UART0_RXD	I	UART0 Data receiver input pin
			PA.13	I/O	General purpose digital IO pin
			PWM0_CH1	I/O	PWM0 Channel1 output
78	39	27	EBI_AD14	I/O	EBI Address/Data bus bit14
			TC1	I	Timer1 capture input
			I2C0_SCL	I/O	I ² C 0 clock pin
			PA.12	I/O	General purpose digital IO pin
			PWM0_CH0	I/O	PWM0 Channel0 output
79	40	28	EBI_AD13	I/O	EBI Address/Data bus bit13
			TC0	I	Timer 0 capture input
			I2C0_SDA	1/0	I ² C 0 data I/O pin
			ICE_DAT	I/O	Serial Wired Debugger Data pin
80	41	29	PF.0	I/O	General purpose digital IO pin
			INT0	I	External interrupt0 input pin
			ICE_CLK	I	Serial Wired Debugger Clock pin
0.4	42	20	PF.1	I/O	General purpose digital IO pin
81	42	30	FCLKO	0	Frequency Divider output pin
			INT1	I	External interrupt1 input pin
82					NC
83			VDD	Р	Power supply for I/O ports and LDO source for internal PLL and digital circuit
84					NC
85			VSS	Р	Ground
86			VSS	Р	Ground
87	43	31	AVSS	AP	Ground Pin for analog circuit
88			AVSS	AP	Ground Pin for analog circuit
89	44	32	PA.0	1/0	General purpose digital IO pin







Pin No.			F.			
LQFP 128-pin	LQFP 64-pin	LQFP 48-pin	Pin Name	Pin Type	Description	
			LCD_SEG39*	AO	LCD segment output 39 at LQFP128	
			PA.5	I/O	General purpose digital I/O pin	
			AD5	Al	ADC analog input5	
			EBI_AD8	I/O	EBI Address/Data bus bit8	
94	49		SC2_RST	0	SmartCard2 RST pin	
			I2C0_SCL	I/O	I ² C0 clock pin	
			LCD_SEG20*	AO	LCD segment output 20 at LQFP64	
			LCD_SEG38*	AO	LCD segment output 38 at LQFP128	
			PA.6	I/O	General purpose digital I/O pin	
			AD6	AI	ADC analog input6	
			EBI_AD7	I/O	EBI Address/Data bus bit7	
95	50		TC3	I	Timer3 capture input	
95	50		SC2_CLK	0	SmartCard2 clock pin(SC2_UART_TXD)	
			PWM0_CH3	0	PWM0 Channel3 output	
			LCD_SEG19*	AO	LCD segment output 19 at LQFP64	
			LCD_SEG37*	AO	LCD segment output 37 at LQFP128	
			PA.7	I/O	General purpose digital I/O pin	
			AD7	AI	ADC analog input7	
			EBI_AD6	I/O	EBI Address/Data bus bit6	
96			TC2	ı	Timer2 capture input	
			SC2_DAT	I/O	SmartCard2 DATA pin(SC2_UART_RXD)	
			PWM0_CH2	0	PWM0 Channel2 output	
			LCD_SEG36*	AO	LCD segment output 36 output at LQFP128	
97	51		VREF	AP	Voltage reference input for ADC	
98					NC	
99	52		AVDD	AP	Power supply for internal analog circuit	
			PD.0	I/O	General purpose digital I/O pin	
400			UART1_RXD	I	UART1 Data receiver input pin	
100			SPI2_SS0	I/O	SPI2 1 st slave select pin	
			SC1_CLK	0	SmartCard1 clock pin(SC1_UART_TXD)	

3.6 Nano110 Block Diagram

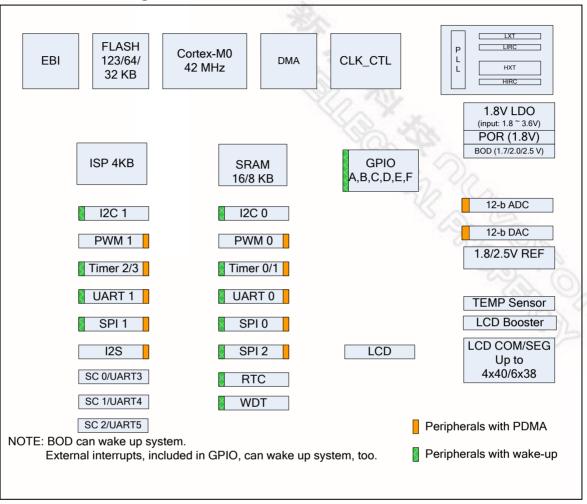
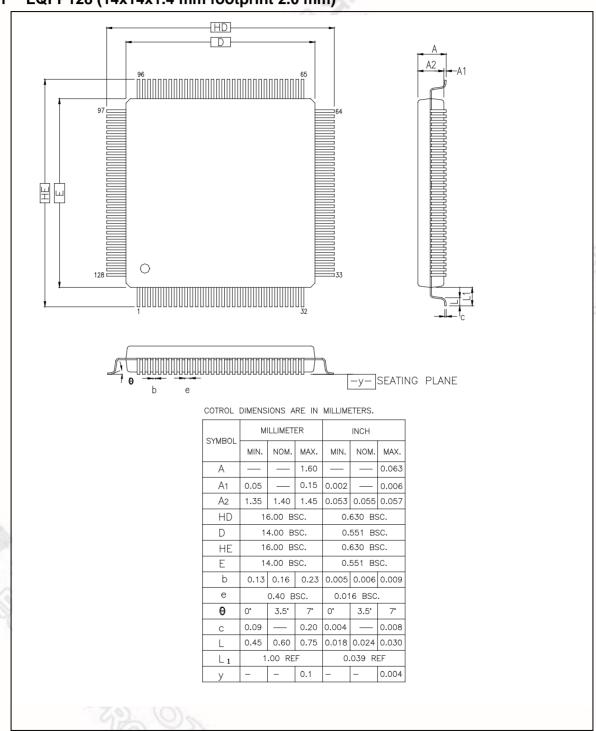


Figure 4-13 NuMicroTM Nano110 Block Diagram

4 PACKAGE DIMENSIONS

4.1 LQFP128 (14x14x1.4 mm footprint 2.0 mm)



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