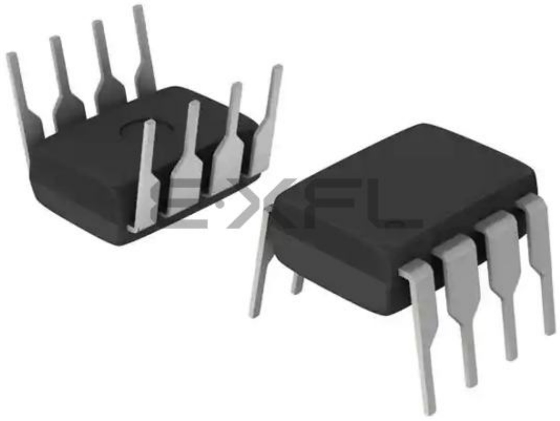
Microchip Technology - PIC10F320-E/P Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	3
Program Memory Size	448B (256 x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f320-e-p

1.0 DEVICE OVERVIEW

The PIC10(L)F320/322 are described within this data sheet. They are available in 6/8-pin packages. Figure 1-1 shows a block diagram of the PIC10(L)F320/322 devices. Table 1-2 shows the pinout descriptions.

Reference Table 1-1 for peripherals available per device.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC10(L)F320	PIC10(L)F322
Analog-to-Digital Converter (ADC)		●	●
Configurable Logic Cell (CLC)		●	●
Complementary Wave Generator (CWG)		●	●
Fixed Voltage Reference (FVR)		●	●
Numerically Controlled Oscillator (NCO)		●	●
Temperature Indicator		●	●
PWM Modules			
	PWM1	●	●
	PWM2	●	●
Timers			
	Timer0	●	●
	Timer2	●	●

REGISTER 2-1: STATUS: STATUS REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R-1/q	R-1/q	R/W-x/u	R/W-x/u	R/W-x/u
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **IRP:** Reserved(2)

bit 6-5 **RP<1:0>:** Reserved(2)

bit 4 **$\overline{\text{TO}}$:** Time-out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{\text{PD}}$:** Power-Down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z:** Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the 4th low-order bit of the result occurred
0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/$\overline{\text{Borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)(1)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

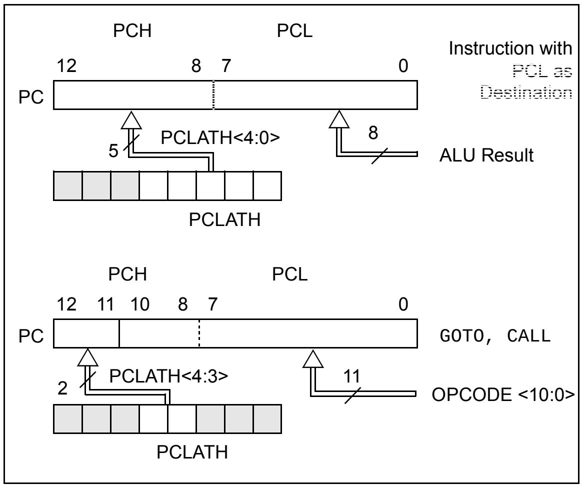
Note 1: For $\overline{\text{Borrow}}$, the polarity is reversed. A subtraction is executed by adding the two’s complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low-order bit of the source register.

2: Maintain as ‘0’.

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in Figure 2-3 shows how the PC is loaded during a `CALL` or `GOTO` instruction (PCLATH<4:3> → PCH).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<12:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper five bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 13 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

A computed `GOTO` is accomplished by adding an offset to the program counter (`ADDWF PCL`). Care should be exercised when jumping into a look-up table or program branch table (computed `GOTO`) by modifying the PCL register. Assuming that PCLATH is set to the table start address, if the table length is greater than 255 instructions or if the lower eight bits of the memory address rolls over from 0xFF to 0x00 in the middle of the table, then PCLATH must be incremented for each address rollover that occurs between the table beginning and the target location within the table.

For more information refer to Application Note AN556, "*Implementing a Table Read*" (DS00556).

2.3.2 STACK

All devices have an 8-level x 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a `CALL` instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a `RETURN`, `RETLW` or a `RETFIE` instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no Status bits to indicate Stack Overflow or Stack Underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the `CALL`, `RETURN`, `RETLW` and `RETFIE` instructions or the vectoring to an interrupt address.

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select Register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although Status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR and the IRP bit of the STATUS register, as shown in Figure 2-4.

A simple program to clear RAM location 40h-7Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        MOVLW   0x40    ;initialize pointer
        MOVWF   FSR     ;to RAM
NEXT    CLRF    INDF    ;clear INDF register
        INCF    FSR     ;inc pointer
        BTFSS   FSR,7   ;all done?
        GOTO    NEXT    ;no clear next
CONTINUE                ;yes continue
```

REGISTER 6-3: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

U-0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0
—	ADIF	—	NCO1IF	CLC1IF	—	TMR2IF	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **Unimplemented**: Read as ‘0’

bit 6 **ADIF:** A/D Converter Interrupt Flag bit
1 = The A/D conversion completed
0 = The A/D conversion is not complete

bit 5 **Unimplemented**: Read as ‘0’

bit 4 **NCO1IF:** Numerically Controlled Oscillator Interrupt Flag bit
1 = NCO1 overflow occurred (must be cleared in software)
0 = No NCO1 overflow

bit 3 **CLC1IF:** Configurable Logic Block Rising Edge Interrupt Flag bit
1 = CLC interrupt occurred (must be cleared in software)
0 = No CLC Interrupt

bit 2 **Unimplemented**: Read as ‘0’

bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
1 = TMR2 to PR2 match occurred (must be cleared in software)
0 = No TMR2 to PR2 match
Note: The match must occur the number of times specified by the TMR2 postscaler (Register 17-1).

bit 0 **Unimplemented**: Read as ‘0’

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Interrupt Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

9.0 FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation over the full VDD range. Program memory is indirectly addressed using Special Function Registers (SFRs). The SFRs used to access program memory are:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When accessing the program memory, the PMDATH:PMDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the PMADRH:PMADRL register pair forms a 2-byte word that holds the 9-bit address of the program memory location being read.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

The Flash program memory can be protected in two ways; by code protection ($\overline{\text{CP}}$ bit in Configuration Word) and write protection (WRT<1:0> bits in Configuration Word).

Code protection ($\overline{\text{CP}}$ = 0)[(1)], disables access, reading and writing, to the Flash program memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a Bulk Erase to the device, clearing all Flash program memory, Configuration bits and User IDs.

Write protection prohibits self-write and erase to a portion or all of the Flash program memory as defined by the bits WRT<1:0>. Write protection does not affect a device programmers ability to read, write or erase the device.

Note 1: Code protection of the entire Flash program memory array is enabled by clearing the $\overline{\text{CP}}$ bit of Configuration Word.

9.1 PMADRL and PMADRH Registers

The PMADRH:PMADRL register pair can address up to a maximum of 512 words of program memory. When selecting a program address value, the MSB of the address is written to the PMADRH register and the LSB is written to the PMADRL register.

9.1.1 PMCON1 AND PMCON2 REGISTERS

PMCON1 is the control register for Flash program memory accesses.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared by hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

The PMCON2 register is a write-only register. Attempting to read the PMCON2 register will return all '0's.

To enable writes to the program memory, a specific pattern (the unlock sequence), must be written to the PMCON2 register. The required unlock sequence prevents inadvertent writes to the program memory write latches and Flash program memory.

9.2 Flash Program Memory Overview

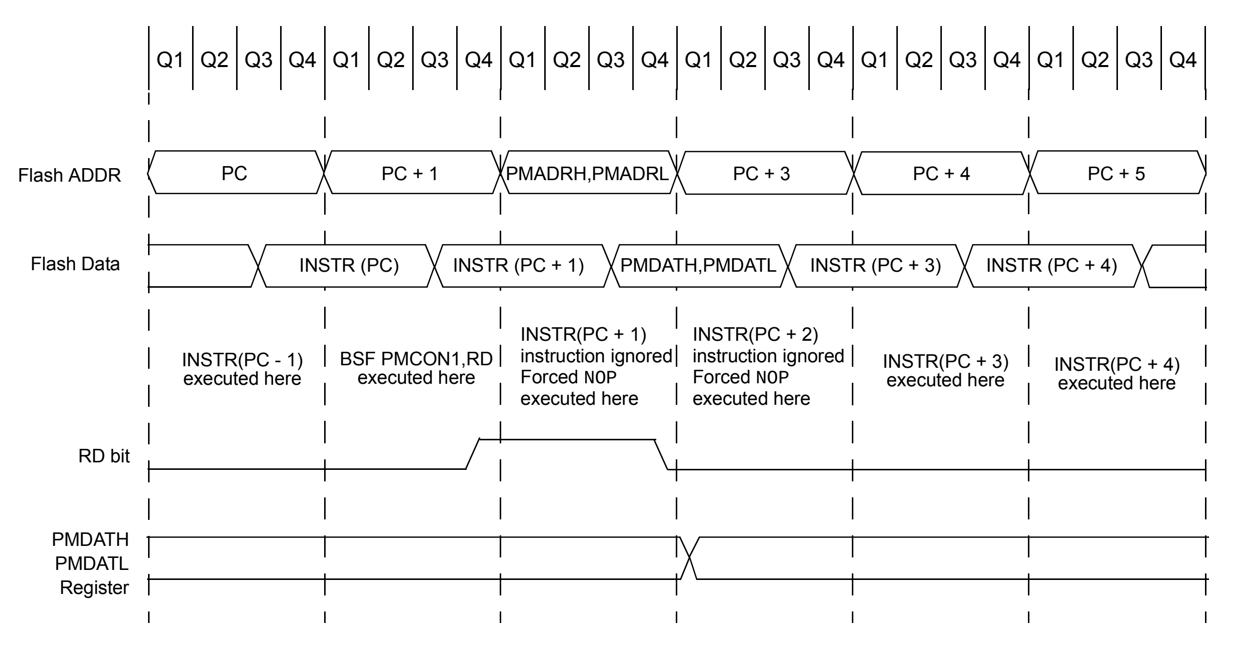
It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the PMDATH:PMDATL register pair.

Note: If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, new data and retained data can be written into the write latches to reprogram the row of Flash program memory. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations.

See Table 9-1 for Erase Row size and the number of write latches for Flash program memory.

FIGURE 9-2: FLASH PROGRAM MEMORY READ CYCLE EXECUTION


Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4 Q1 Q2 Q3 Q4
Flash ADDR
PC
PC + 1
PMADRH,PMADRL
PC + 3
PC + 4
PC + 5
Flash Data
INSTR (PC)
INSTR (PC + 1)
PMDATH,PMDATL
INSTR (PC + 3)
INSTR (PC + 4)
INSTR(PC - 1) executed here
BSF PMCON1,RD executed here
INSTR(PC + 1) instruction ignored Forced NOP executed here
INSTR(PC + 2) instruction ignored Forced NOP executed here
INSTR(PC + 3) executed here
INSTR(PC + 4) executed here
RD bit
PMDATH
PMDATL
Register

EXAMPLE 9-1: FLASH PROGRAM MEMORY READ

```
* This code block will read 1 word of program
* memory at the memory address:
    PROG_ADDR_HI: PROG_ADDR_LO
*   data will be returned in the variables;
*   PROG_DATA_HI, PROG_DATA_LO

    BANKSEL  PMADRL            ; not required on devices with 1 Bank of SFRs
    MOVLW    PROG_ADDR_LO      ;
    MOVWF    PMADRL            ; Store LSB of address
    MOVLW    PROG_ADDR_HI      ;
    MOVWF    PMADRH            ; Store MSB of address

    BCF      PMCON1,CFGS       ; Do not select Configuration Space
    BSF      PMCON1,RD         ; Initiate read
    NOP                        ; Ignored (Figure 9-2)
    NOP                        ; Ignored (Figure 9-2)

    MOVF     PMDATL,W          ; Get LSB of word
    MOVWF    PROG_DATA_LO      ; Store in user location
    MOVF     PMDATH,W          ; Get MSB of word
    MOVWF    PROG_DATA_HI      ; Store in user location
```

10.2 Register Definitions: PORTA

REGISTER 10-1: PORTA: PORTA REGISTER

U-0	U-0	U-0	U-0	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x
—	—	—	—	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented**: Read as ‘0’

bit 3-0 **RA<3:0>:** PORTA I/O Value bits (RA3 is read-only)

Note 1: Writes to PORTx are actually written to the corresponding LATx register. Reads from PORTx register return actual I/O pin values.

REGISTER 10-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	U-0	U-0	U-1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	—	—[1]	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented**: Read as ‘0’.

bit 3 **Unimplemented**: Read as ‘1’.

bit 2-0 **TRISA<2:0>:** RA<2:0> Port I/O Tri-State Control bits
1 = Port output driver is disabled
0 = Port output driver is enabled

Note 1: Unimplemented, read as ‘1’.

11.0 INTERRUPT-ON-CHANGE

The PORTA pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual PORTA pin, or combination of PORTA pins, can be configured to generate an interrupt. The Interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 11-1 is a block diagram of the IOC module.

11.1 Enabling the Module

To allow individual PORTA pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

11.2 Individual Pin Configuration

For each PORTA pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated IOCAPx bit of the IOCAP register is set. To enable a pin to detect a falling edge, the associated IOCANx bit of the IOCAN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both the IOCAPx bit and the IOCANx bit of the IOCAP and IOCAN registers, respectively.

11.3 Interrupt Flags

The IOCAFx bits located in the IOCAF register are status flags that correspond to the interrupt-on-change pins of PORTA. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx bits.

11.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 11-1: CLEARING INTERRUPT FLAGS

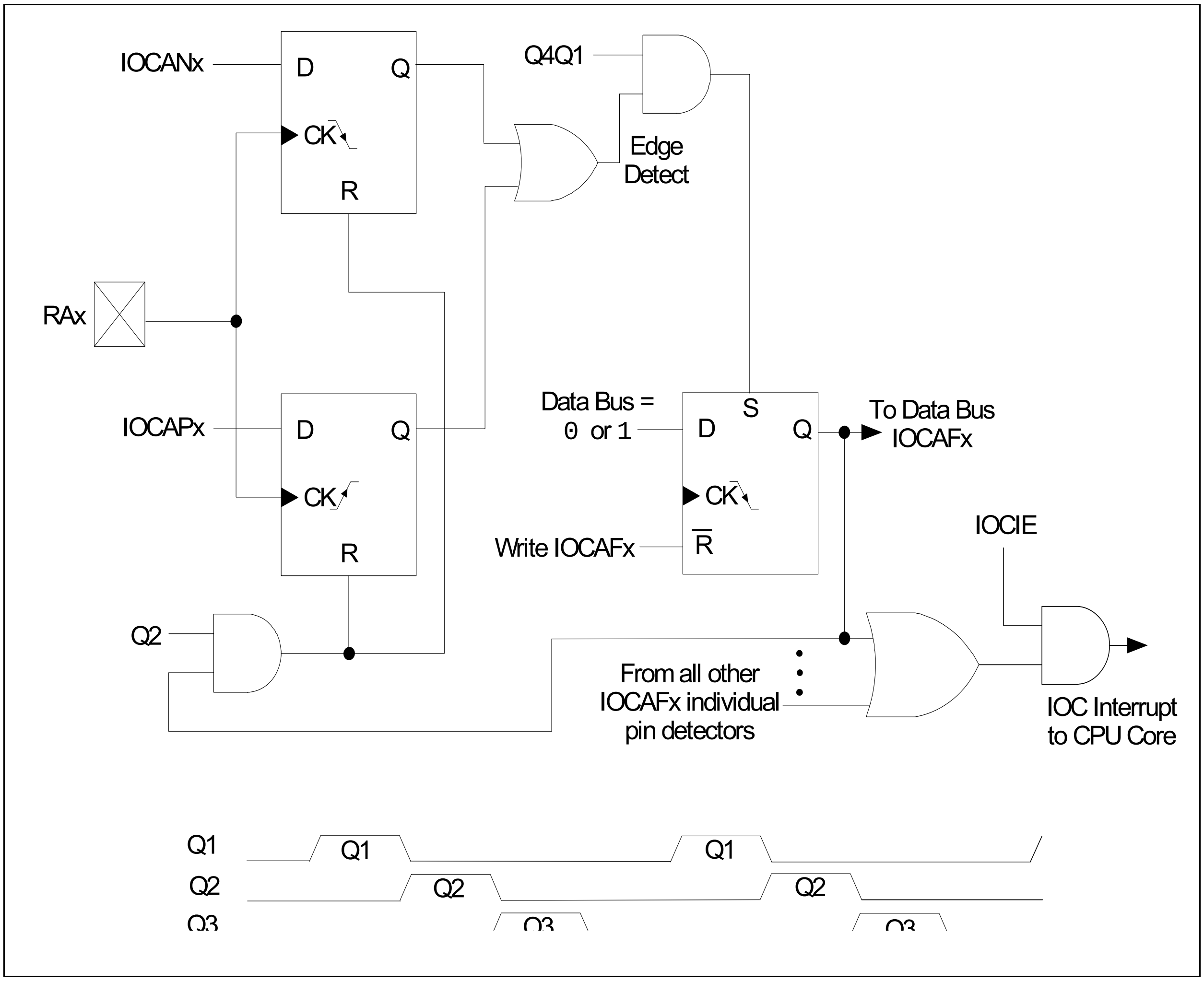
```
    MOVLW  0xff
    XORWF  IOCAF, W
    ANDWF  IOCAF, F
```

11.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCAF register will be updated prior to the first instruction executed out of Sleep.

FIGURE 11-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM



13.0 INTERNAL VOLTAGE REGULATOR (IVR)

The Internal Voltage Regulator (IVR), which provides operation above 3.6V is available on:

- PIC10F320
- PIC10F322

This circuit regulates a voltage for the internal device logic while permitting the VDD and I/O pins to operate at a higher voltage. When VDD approaches the regulated voltage, the IVR output automatically tracks the input voltage.

The IVR operates in one of three power modes based on user configuration and peripheral selection. The operating power modes are:

- High
- Low
- Power-Save Sleep mode

Power modes are selected automatically depending on the device operation, as shown in Table 13-1. Tracking mode is selected automatically when VDD drops below the safe operating voltage of the core.

Note: IVR is disabled in Tracking mode, but will consume power. See **Section 24.0 "Electrical Specifications"** for more information.

TABLE 13-1: IVR POWER MODES - REGULATED

VREGPM1 Bit	Sleep Mode	Memory Bias Power Mode	IVR Power Mode
x	No	EC Mode or INTOSC = 16 MHz (HP Bias)	High
		INTOSC = 1 to 8 MHz (MP Bias)	
		INTOSC = 31 kHz to 500 kHz (LP Bias)	Low
0	Yes	Don't Care	Low
1	Yes	No HFINTOSC No Peripherals	Power Save[1]

Note 1: Forced to Low-Power mode by any of the following conditions:

- BOR is enabled
- HFINTOSC is an active peripheral source
- Self-write is active
- ADC is in an active conversion

15.4 A/D Acquisition Requirements

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 15-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 15-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 15-1 may be used. This equation assumes that 1/2 LSb error is used (511 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 15-1: ACQUISITION TIME EXAMPLE

Assumptions: $Temperature = 50°C$ *and external impedance of* $10k\Omega$ $5.0V$ V_{DD}

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(Temperature - 25°C)(0.05\mu s/°C)] \end{aligned}$$

The value for T_C *can be approximated with the following equations:*

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \qquad ;[1]\ V_{CHOLD} \text{ charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \qquad ;[2]\ V_{CHOLD} \text{ charge response to } V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-Tc}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \qquad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for T_C:

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/511) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.001957) \\ &= 1.12\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 1.12\mu s + [(50°C - 25°C)(0.05\mu s/°C)] \\ &= 4.37\mu s \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

REGISTER 19-7: CLCxGLS2: GATE 3 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG3D4T	LCxG3D4N	LCxG3D3T	LCxG3D3N	LCxG3D2T	LCxG3D2N	LCxG3D1T	LCxG3D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **LCxG3D4T:** Gate 3 Data 4 True (non-inverted) bit
1 = lcxd4T is gated into lcxg3
0 = lcxd4T is not gated into lcxg3

bit 6 **LCxG3D4N:** Gate 3 Data 4 Negated (inverted) bit
1 = lcxd4N is gated into lcxg3
0 = lcxd4N is not gated into lcxg3

bit 5 **LCxG3D3T:** Gate 3 Data 3 True (non-inverted) bit
1 = lcxd3T is gated into lcxg3
0 = lcxd3T is not gated into lcxg3

bit 4 **LCxG3D3N:** Gate 3 Data 3 Negated (inverted) bit
1 = lcxd3N is gated into lcxg3
0 = lcxd3N is not gated into lcxg3

bit 3 **LCxG3D2T:** Gate 3 Data 2 True (non-inverted) bit
1 = lcxd2T is gated into lcxg3
0 = lcxd2T is not gated into lcxg3

bit 2 **LCxG3D2N:** Gate 3 Data 2 Negated (inverted) bit
1 = lcxd2N is gated into lcxg3
0 = lcxd2N is not gated into lcxg3

bit 1 **LCxG3D1T:** Gate 3 Data 1 True (non-inverted) bit
1 = lcxd1T is gated into lcxg3
0 = lcxd1T is not gated into lcxg3

bit 0 **LCxG3D1N:** Gate 3 Data 1 Negated (inverted) bit
1 = lcxd1N is gated into lcxg3
0 = lcxd1N is not gated into lcxg3

REGISTER 19-8: CLCxGLS3: GATE 4 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG4D4T	LCxG4D4N	LCxG4D3T	LCxG4D3N	LCxG4D2T	LCxG4D2N	LCxG4D1T	LCxG4D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **LCxG4D4T:** Gate 4 Data 4 True (non-inverted) bit
1 = lcxd4T is gated into lcxg4
0 = lcxd4T is not gated into lcxg4

bit 6 **LCxG4D4N:** Gate 4 Data 4 Negated (inverted) bit
1 = lcxd4N is gated into lcxg4
0 = lcxd4N is not gated into lcxg4

bit 5 **LCxG4D3T:** Gate 4 Data 3 True (non-inverted) bit
1 = lcxd3T is gated into lcxg4
0 = lcxd3T is not gated into lcxg4

bit 4 **LCxG4D3N:** Gate 4 Data 3 Negated (inverted) bit
1 = lcxd3N is gated into lcxg4
0 = lcxd3N is not gated into lcxg4

bit 3 **LCxG4D2T:** Gate 4 Data 2 True (non-inverted) bit
1 = lcxd2T is gated into lcxg4
0 = lcxd2T is not gated into lcxg4

bit 2 **LCxG4D2N:** Gate 4 Data 2 Negated (inverted) bit
1 = lcxd2N is gated into lcxg4
0 = lcxd2N is not gated into lcxg4

bit 1 **LCxG4D1T:** Gate 4 Data 1 True (non-inverted) bit
1 = lcxd1T is gated into lcxg4
0 = lcxd1T is not gated into lcxg4

bit 0 **LCxG4D1N:** Gate 4 Data 1 Negated (inverted) bit
1 = lcxd1N is gated into lcxg4
0 = lcxd1N is not gated into lcxg4

20.8 NCOx Control Registers

REGISTER 20-1: NCOxCON: NCOx CONTROL REGISTER

R/W-0/0	R/W-0/0	R-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0
NxEN	NxOE	NxOUT	NxPOL	—	—	—	NxPFM
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **NxEN:** NCOx Enable bit
1 = NCOx module is enabled
0 = NCOx module is disabled

bit 6 **NxOE:** NCOx Output Enable bit
1 = NCOx output pin is enabled
0 = NCOx output pin is disabled

bit 5 **NxOUT:** NCOx Output bit
1 = NCOx output is high
0 = NCOx output is low

bit 4 **NxPOL:** NCOx Polarity bit
1 = NCOx output signal is active-low (inverted)
0 = NCOx output signal is active-high (non-inverted)

bit 3-1 **Unimplemented**: Read as ‘0’.

bit 0 **NxPFM:** NCOx Pulse Frequency mode bit
1 = NCOx operates in Pulse Frequency mode
0 = NCOx operates in Fixed Duty Cycle mode

REGISTER 20-2: NCOxCLK: NCOx INPUT CLOCK CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
NxPWS<2:0>[(1,2)]			—	—	—	NxCKS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **NxPWS<2:0>:** NCOx Output Pulse Width Select bits[(1, 2)]
111 = 128 NCOx clock periods
110 = 64 NCOx clock periods
101 = 32 NCOx clock periods
100 = 16 NCOx clock periods
011 = 8 NCOx clock periods
010 = 4 NCOx clock periods
001 = 2 NCOx clock periods
000 = 1 NCOx clock periods

bit 4-2 **Unimplemented:** Read as ‘0’

bit 1-0 **NxCKS<1:0>:** NCOx Clock Source Select bits
11 = LC1OUT
10 = HFINTOSC (16 MHz)
01 = FOSC
00 = NCO1CLK pin

Note 1: NxPWS applies only when operating in Pulse Frequency mode.
2: If NCOx pulse width is greater than NCOx overflow period, operation is undefined.

MOVF	Move f
Syntax:	[*label*] MOVF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f) → (dest)
Status Affected:	Z
Description:	The contents of register ‘f’ is moved to a destination dependent upon the status of ‘d’. If d = 0, destination is W register. If d = 1, the destination is file register ‘f’ itself. d = 1 is useful to test a file register since Status flag Z is affected.
Words:	1
Cycles:	1

Example:	`MOVF FSR, 0`
	After Instruction
	W = value in FSR register
	Z = 1

MOVLW	Move literal to W
Syntax:	[*label*] MOVLW k
Operands:	$0 \le k \le 255$
Operation:	k → (W)
Status Affected:	None
Description:	The 8-bit literal ‘k’ is loaded into W register. The “don’t cares” will assemble as ‘0’s.
Words:	1
Cycles:	1

Example:	`MOVLW 0x5A`
	After Instruction
	W = 0x5A

MOVWF	Move W to f
Syntax:	[*label*] MOVWF f
Operands:	$0 \le f \le 127$
Operation:	(W) → (f)
Status Affected:	None
Description:	Move data from W register to register ‘f’.
Words:	1
Cycles:	1

Example:	`MOVW OPTION_REG`
	`F`
	Before Instruction
	OPTION_REG = 0xFF
	W = 0x4F
	After Instruction
	OPTION_REG = 0x4F
	W = 0x4F

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

24.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: VDDMIN ≤ VDD ≤ VDDMAX
Operating Temperature: TA_MIN ≤ TA ≤ TA_MAX

VDD — Operating Supply Voltage[1]

PIC10LF320/322

VDDMIN (Fosc ≤ 16 MHz)	+1.8V
VDDMIN (16 MHz < Fosc ≤ 20 MHz)	+2.5V
VDDMAX	+3.6V

PIC10F320/322

VDDMIN (Fosc ≤ 16 MHz)	+2.3V
VDDMIN (16 MHz < Fosc ≤ 20 MHz)	+2.5V
VDDMAX	+5.5V

TA — Operating Ambient Temperature Range

Industrial Temperature

TA_MIN	-40°C
TA_MAX	+85°C

Extended Temperature

TA_MIN	-40°C
TA_MAX	+125°C

Note 1: See Parameter D001, DC Characteristics: Supply Voltage.

TABLE 24-2: SUPPLY VOLTAGE (IDD)$^{(1,2)}$

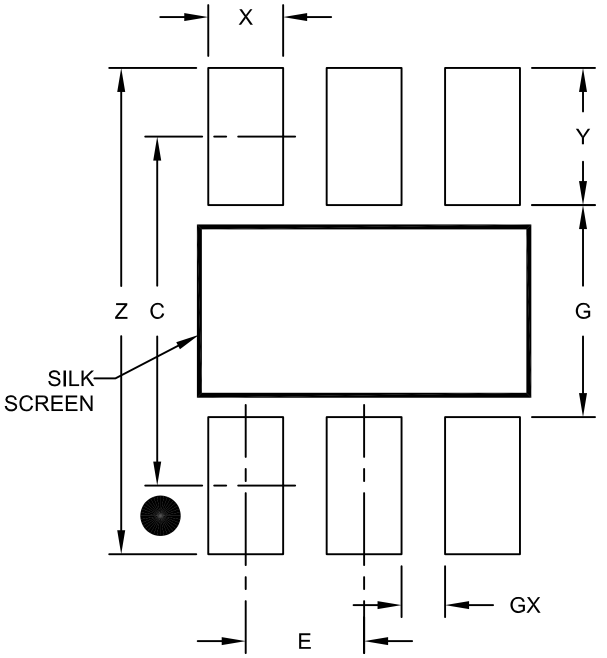
PIC10LF320/322			Standard Operating Conditions (unless otherwise stated)				
PIC10F320/322							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						VDD	Note
D013		—	34	45	µA	1.8	FOSC = 500 kHz EC mode
		—	60	105	µA	3.0	
D013		—	76	101	µA	2.3	FOSC = 500 kHz EC mode
		—	110	148	µA	3.0	
		—	153	211	µA	5.0	
D014		—	190	290	µA	1.8	FOSC = 8 MHz EC mode
		—	350	500	µA	3.0	
D014		—	290	430	µA	2.3	FOSC = 8 MHz EC mode
		—	395	600	µA	3.0	
		—	480	775	µA	5.0	
D015		—	0.8	1.3	mA	3.0	FOSC = 20 MHz EC mode
		—	1.1	1.8	mA	3.6	
D015		—	0.8	1.4	mA	3.0	FOSC = 20 MHz EC mode
		—	1.1	1.8	mA	5.0	
D016		—	2.2	4.1	µA	1.8	FOSC = 32 kHz LFINTOSC mode, 85°C
		—	3.9	6.5	µA	3.0	
D016		—	31	44	µA	2.3	FOSC = 32 kHz LFINTOSC mode, 85°C
		—	40	57	µA	3.0	
		—	71	117	µA	5.0	
D016A		—	3.2	4.5	µA	1.8	FOSC = 32 kHz LFINTOSC mode, 125°C
		—	4.8	7.0	µA	3.0	
D016A		—	31	44	µA	2.3	FOSC = 32 kHz LFINTOSC mode,125°C
		—	40	57	µA	3.0	
		—	71	117	µA	5.0	

Note 1: The test conditions for all IDD measurements in active operation mode are: CLKIN = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; $\overline{\text{MCLR}}$ = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

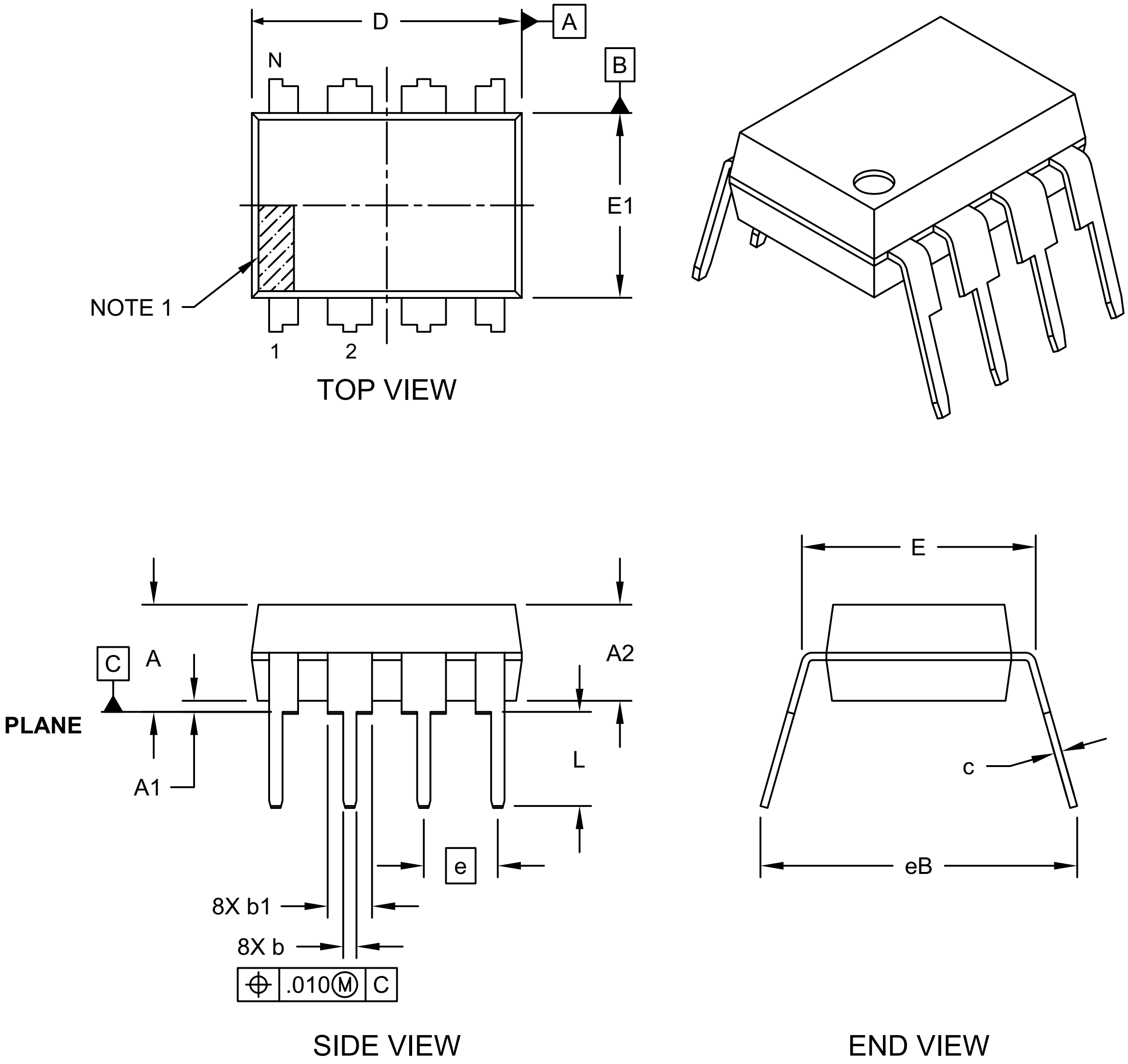
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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