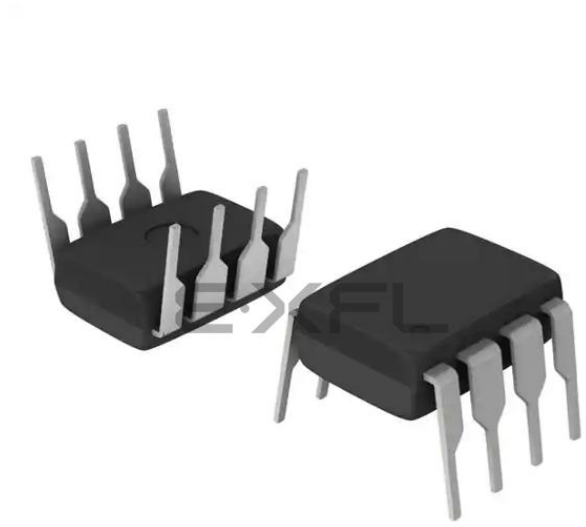

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	3
Program Memory Size	896B (512 x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic10f322-i-p

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TABLE 1-2: PIC10(L)F320/322 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/PWM1/CLC1IN0/CWG1A/ AN0/ICSPDAT	RA0	TTL	CMOS	General purpose I/O with IOC and WPU.
	PWM1	—	CMOS	PWM output.
	CLC1IN0	ST	—	CLC input.
	CWG1A	—	CMOS	CWG primary output.
	AN0	AN	—	A/D Channel input.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RA1/PWM2/CLC1/CWG1B/AN1/ CLKIN/ICSPCLK/NCO1CLK	RA1	TTL	CMOS	General purpose I/O with IOC and WPU.
	PWM2	—	CMOS	PWM output.
	CLC1	—	CMOS	CLC output.
	CWG1B	—	CMOS	CWG complementary output.
	AN1	AN	—	A/D Channel input.
	CLKIN	ST	—	External Clock input (EC mode).
	ICSPCLK	ST	—	ICSP™ Programming Clock.
	NCO1CLK	ST	—	Numerical Controlled Oscillator external clock input.
RA2/INT/T0CKI/NCO1/CLC1IN1/ CLKR/AN2/$\overline{\text{CWG1FLT}}$	RA2	TTL	CMOS	General purpose I/O with IOC and WPU.
	INT	ST	—	External interrupt.
	T0CKI	ST	—	Timer0 clock input.
	NCO1	—	CMOS	Numerically Controlled Oscillator output.
	CLC1IN1	ST	—	CLC input.
	CLKR	—	CMOS	Clock Reference output.
	AN2	AN	—	A/D Channel input.
	$\overline{\text{CWG1FLT}}$	ST	—	Complementary Waveform Generator Fault 1 source input.
RA3/$\overline{\text{MCLR}}$/V_{PP}	RA3	TTL	—	General purpose input.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
	V_{PP}	HV	—	Programming voltage.
V_{DD}	V_{DD}	Power	—	Positive supply.
V_{SS}	V_{SS}	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output
TTL = CMOS input with TTL levels ST = CMOS input with Schmitt Trigger levels
HV = High Voltage

3.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Word and Device ID.

3.1 Configuration Word

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word at 2007h.

REGISTER 3-1: CONFIG: CONFIGURATION WORD (CONTINUED)

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled
10 = WDT enabled while running and disabled in Sleep
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled

bit 2-1 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = Brown-out Reset enabled; SBOREN bit is ignored
10 = Brown-out Reset enabled while running, disabled in Sleep; SBOREN bit is ignored
01 = Brown-out Reset controlled by the SBOREN bit in the BORCON register
00 = Brown-out Reset disabled; SBOREN bit is ignored

bit 0 **FOSC:** Oscillator Selection bit
1 = EC on CLKIN pin
0 = INTOSC oscillator I/O function available on CLKIN pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: Once enabled, code-protect can only be disabled by bulk erasing the device.
3: See V_{BOR} parameter for specific trip point voltages.

TABLE 8-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	IRCF<2:0>			HFIOFR	—	LFIOFR	HFIOFS	26
STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	13
WDTCON	—	—	WDTPS<4:0>					SWDTEN	48

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 8-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG	13:8	—	—	—	WRT<1:0>		BORV	LPBOR	LVP	20
	7:0	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE<1:0>		BOREN<1:0>		FOSC	

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

9.6 Flash Program Memory Control Registers

REGISTER 9-1: PMDATL: PROGRAM MEMORY DATA LOW

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PMDAT<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PMDAT<7:0>**: The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

REGISTER 9-2: PMDATH: PROGRAM MEMORY DATA HIGH

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	PMDAT<13:8>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **PMDAT<13:8>**: The value of the program memory word pointed to by PMADRH and PMADRL after a Program Memory Read command.

10.0 I/O PORT

Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

PORTA has three standard registers for its operation. These registers are:

- TRISA register (data direction)
- PORTA register (reads the levels on the pins of the device)
- LATA register (output latch)

Some ports may have one or more of the following additional registers. These registers are:

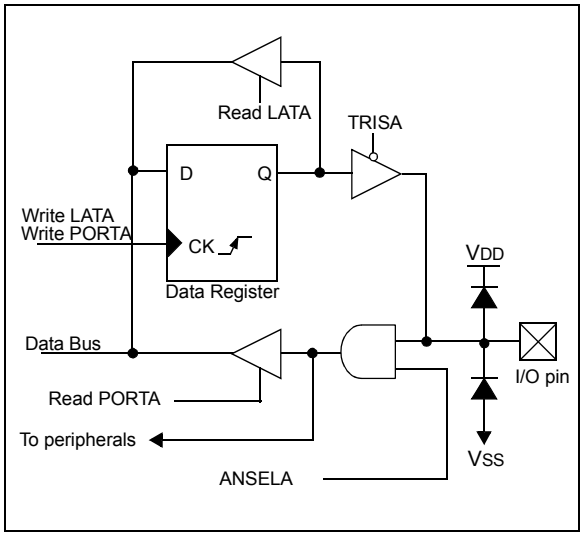
- ANSELA (analog select)
- WPUA (weak pull-up)

The Data Latch (LATA register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATA register has the same effect as a write to the corresponding PORTA register. A read of the LATA register reads of the values held in the I/O PORT latches, while a read of the PORTA register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELA register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: I/O PORT OPERATION



EXAMPLE 10-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL   PORTA          ;not required on devices with 1 Bank of SFRs
CLRF      PORTA          ;Init PORTA
BANKSEL   LATA           ;not required on devices with 1 Bank of SFRs
CLRF      LATA           ;
BANKSEL   ANSELA         ;not required on devices with 1 Bank of SFRs
CLRF      ANSELA         ;digital I/O
BANKSEL   TRISA          ;not required on devices with 1 Bank of SFRs
MOVLW     B'00000011'    ;Set RA<1:0> as inputs
MOVWF     TRISA          ;and set RA<2:3> as
                         ;outputs
```

TABLE 10-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	—	—	ANSA2	ANSA1	ANSA0	70
IOCAF	—	—	—	—	IOCAF3	IOCAF2	IOCAF1	IOCAF0	76
IOCAN	—	—	—	—	IOCAN3	IOCAN2	IOCAN1	IOCAN0	75
IOCAP	—	—	—	—	IOCAP3	IOCAP2	IOCAP1	IOCAP0	75
LATA	—	—	—	—	—	LATA2	LATA1	LATA0	70
PORTA	—	—	—	—	RA3	RA2	RA1	RA0	69
TRISA	—	—	—	—	—(1)	TRISA2	TRISA1	TRISA0	69
WPUA	—	—	—	—	WPUA3	WPUA2	WPUA1	WPUA0	71

Legend: x = unknown, u = unchanged, – = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: Unimplemented, read as '1'.

12.3 FVR Control Registers

REGISTER 12-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
FVREN	FVRRDY(1)	TSEN(3)	TSRNG(3)	—	—	ADFVR<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
1 = Fixed Voltage Reference is enabled
0 = Fixed Voltage Reference is disabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
1 = Fixed Voltage Reference output is ready for use
0 = Fixed Voltage Reference output is not ready or not enabled

bit 5 **TSEN:** Temperature Indicator Enable bit(3)
1 = Temperature Indicator is enabled
0 = Temperature Indicator is disabled

bit 4 **TSRNG:** Temperature Indicator Range Selection bit(3)
1 = $V_{OUT} = V_{DD} - 4V_T$ (High Range)
0 = $V_{OUT} = V_{DD} - 2V_T$ (Low Range)

bit 3-2 **Unimplemented**: Read as '0'

bit 1-0 **ADFVR<1:0>:** ADC Fixed Voltage Reference Selection bit
11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)
10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)
00 = ADC Fixed Voltage Reference Peripheral output is off.

Note 1: FVRRDY indicates the true state of the FVR.
2: Fixed Voltage Reference output cannot exceed V_{DD}.
3: See **Section 14.0 "Temperature Indicator Module"** for additional information.

TABLE 12-2: SUMMARY OF REGISTERS ASSOCIATED WITH FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	—	—	ADFVR<1:0>		78

Legend: Shaded cells are not used with the Fixed Voltage Reference.

TABLE 15-1: ADC CLOCK PERIOD (T_{AD}) VS. DEVICE OPERATING FREQUENCIES

ADC Clock Period (T_{AD})		Device Frequency (F_{OSC})			
ADC Clock Source	ADCS<2:0>	16 MHz	8 MHz	4 MHz	1 MHz
F_{OSC}/2	000	125 ns(1)	250 ns(1)	500 ns(1)	2.0 μs
F_{OSC}/4	100	250 ns(1)	500 ns(1)	1.0 μs	4.0 μs
F_{OSC}/8	001	0.5 μs(1)	1.0 μs	2.0 μs	8.0 μs(2)
F_{OSC}/16	101	1.0 μs	2.0 μs	4.0 μs	16.0 μs(2)
F_{OSC}/32	010	2.0 μs	4.0 μs	8.0 μs(2)	32.0 μs(2)
F_{OSC}/64	110	4.0 μs	8.0 μs(2)	16.0 μs(2)	64.0 μs(2)
FRC	x11	1.0-6.0 μs(1,3)	1.0-6.0 μs(1,3)	1.0-6.0 μs(1,3)	1.0-6.0 μs(1,3)

Legend: Shaded cells are outside of recommended range.

Note 1: These values violate the minimum required T_{AD} time.

2: For faster conversion times, the selection of another clock source is recommended.

3: The ADC clock period (T_{AD}) and total ADC conversion time can be minimized when the ADC clock is derived from the system clock F_{OSC}. However, the FRC clock source must be used when conversions are to be performed with the device in Sleep mode.

FIGURE 15-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES

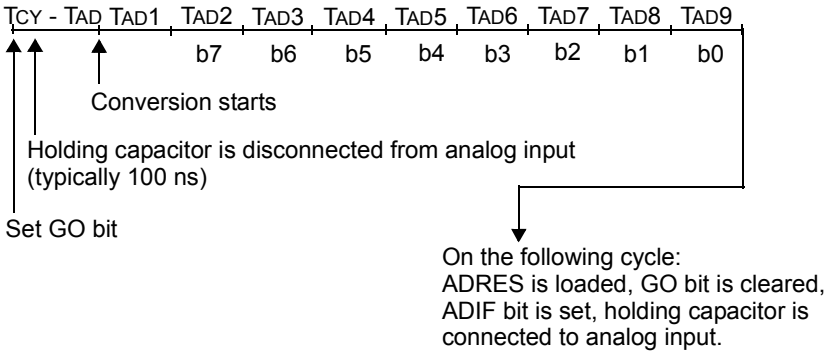
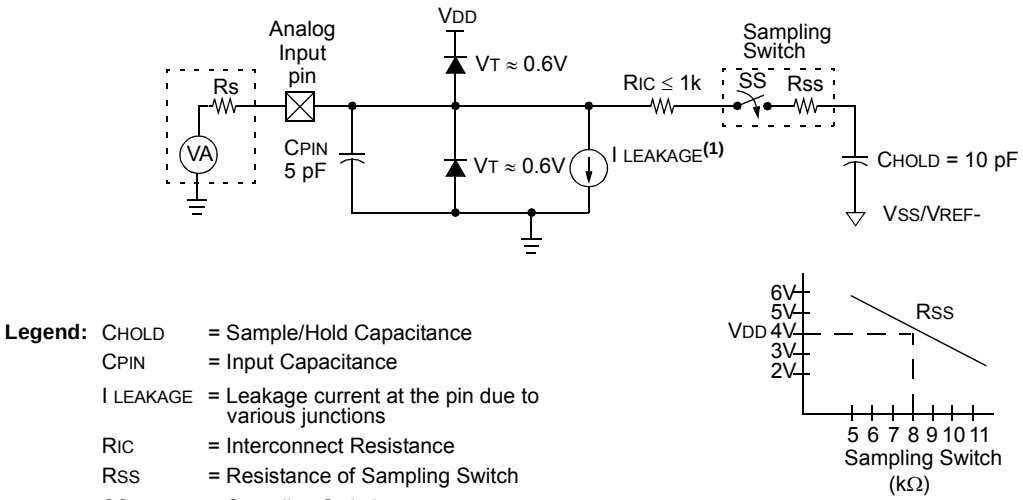


FIGURE 15-3: ANALOG INPUT MODEL



Legend: CHOLD = Sample/Hold Capacitance
CPIN = Input Capacitance
I LEAKAGE = Leakage current at the pin due to various junctions
RIC = Interconnect Resistance
RSS = Resistance of Sampling Switch
SS = Sampling Switch
VT = Threshold Voltage

Note 1: Refer to **Section 24.0 "Electrical Specifications"**.

FIGURE 15-4: ADC TRANSFER FUNCTION

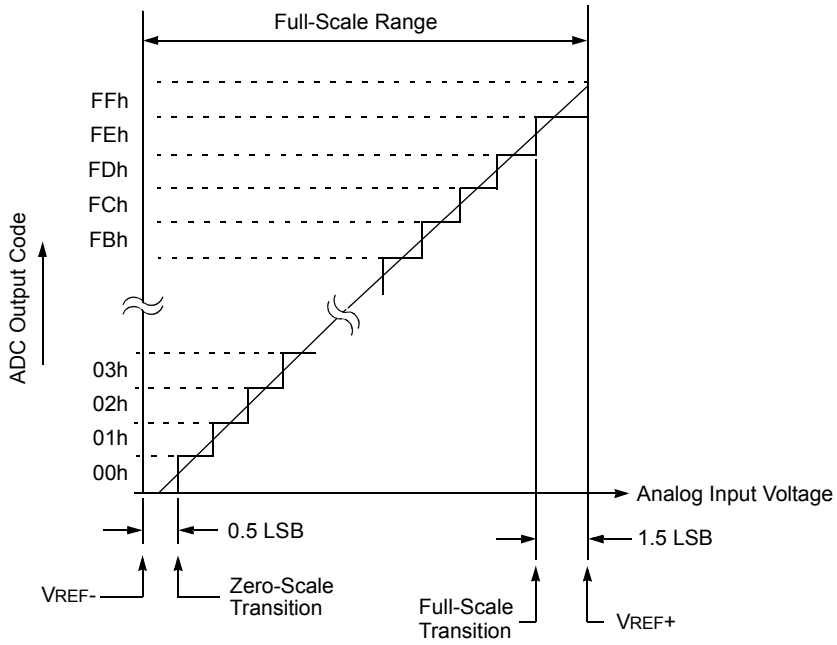
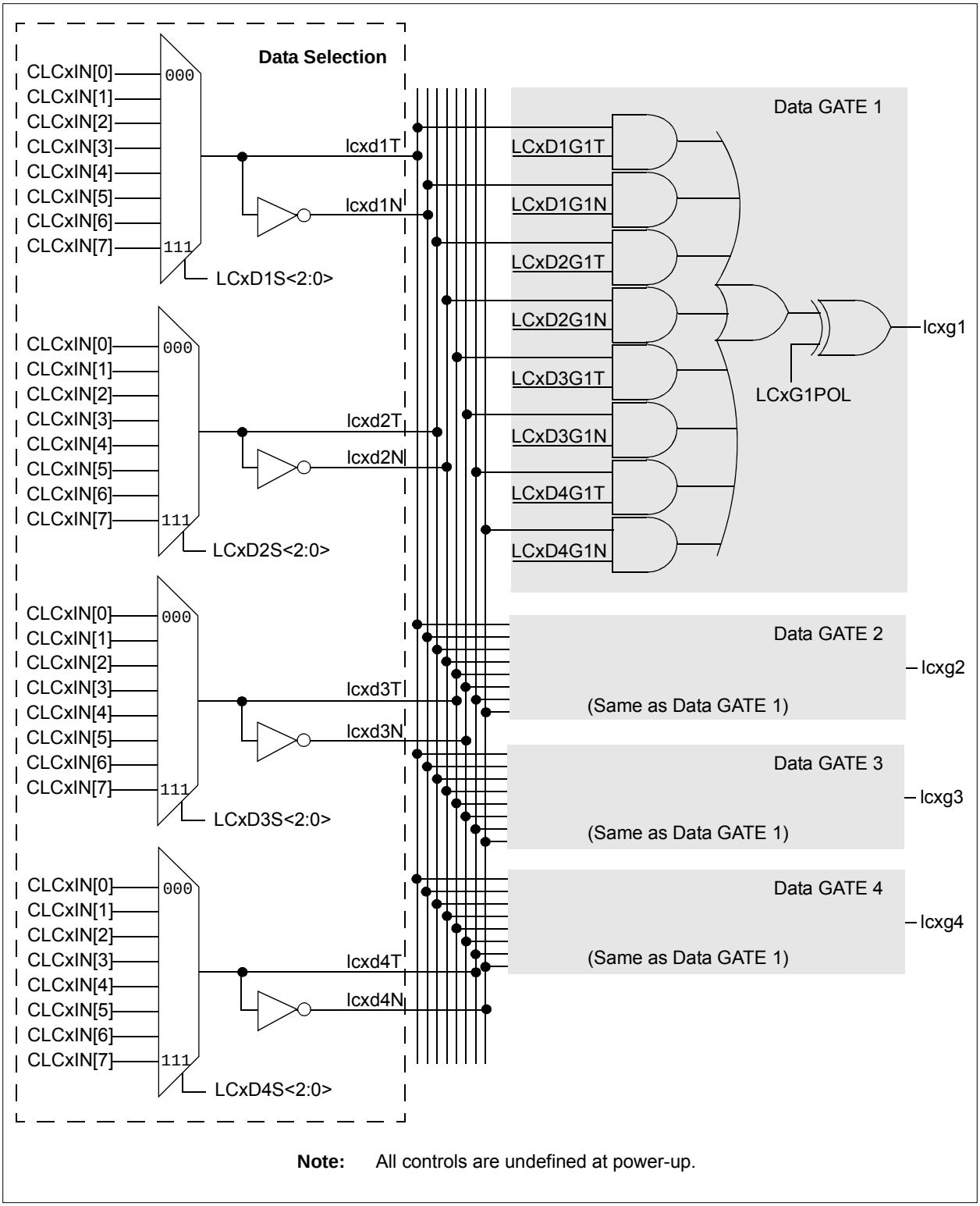


FIGURE 19-2: INPUT DATA SELECTION AND GATING



Note: All controls are undefined at power-up.

REGISTER 19-5: CLCxGLS0: GATE 1 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG1D4T	LCxG1D4N	LCxG1D3T	LCxG1D3N	LCxG1D2T	LCxG1D2N	LCxG1D1T	LCxG1D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **LCxG1D4T:** Gate 1 Data 4 True (non-inverted) bit
1 = lcxd4T is gated into lcxg1
0 = lcxd4T is not gated into lcxg1

bit 6 **LCxG1D4N:** Gate 1 Data 4 Negated (inverted) bit
1 = lcxd4N is gated into lcxg1
0 = lcxd4N is not gated into lcxg1

bit 5 **LCxG1D3T:** Gate 1 Data 3 True (non-inverted) bit
1 = lcxd3T is gated into lcxg1
0 = lcxd3T is not gated into lcxg1

bit 4 **LCxG1D3N:** Gate 1 Data 3 Negated (inverted) bit
1 = lcxd3N is gated into lcxg1
0 = lcxd3N is not gated into lcxg1

bit 3 **LCxG1D2T:** Gate 1 Data 2 True (non-inverted) bit
1 = lcxd2T is gated into lcxg1
0 = lcxd2T is not gated into lcxg1

bit 2 **LCxG1D2N:** Gate 1 Data 2 Negated (inverted) bit
1 = lcxd2N is gated into lcxg1
0 = lcxd2N is not gated into lcxg1

bit 1 **LCxG1D1T:** Gate 1 Data 1 True (non-inverted) bit
1 = lcxd1T is gated into lcxg1
0 = lcxd1T is not gated into lcxg1

bit 0 **LCxG1D1N:** Gate 1 Data 1 Negated (inverted) bit
1 = lcxd1N is gated into lcxg1
0 = lcxd1N is not gated into lcxg1

20.1 NCOx OPERATION

The NCOx operates by repeatedly adding a fixed value to an accumulator. Additions occur at the input clock rate. The accumulator will overflow with a carry periodically, which is the raw NCOx output. This effectively reduces the input clock by the ratio of the addition value to the maximum accumulator value. See Equation 20-1.

The NCOx output can be further modified by stretching the pulse or toggling a flip-flop. The modified NCOx output is then distributed internally to other peripherals and optionally output to a pin. The accumulator overflow also generates an interrupt.

The NCOx output creates an instantaneous frequency, which may cause uncertainty. This output depends on the ability of the receiving circuit (i.e., CWG or external resonant converter circuitry) to average the instantaneous frequency to reduce uncertainty.

20.1.1 NCOx CLOCK SOURCES

Clock sources available to the NCOx include:

- HFINTOSC
- FOSC
- LC1OUT
- NCO1CLK pin

The NCOx clock source is selected by configuring the NxCKS<1:0> bits in the NCOxCLK register.

20.1.2 ACCUMULATOR

The Accumulator is a 20-bit register. Read and write access to the Accumulator is available through three registers:

- NCOxACCL
- NCOxACCH
- NCOxACCU

20.1.3 ADDER

The NCOx Adder is a full adder, which operates asynchronously to the clock source selected. The addition of the previous result and the increment value replaces the accumulator value on the rising edge of each input clock.

20.1.4 INCREMENT REGISTERS

The Increment value is stored in two 8-bit registers making up a 16-bit increment. In order of LSB to MSB they are:

- NCOxINCL
- NCOxINCH

Both of the registers are readable and writable. The Increment registers are double-buffered to allow for value changes to be made without first disabling the NCOx module.

The buffer loads are immediate when the module is disabled. Writing to the MS register first is necessary because then the buffer is loaded synchronously with the NCOx operation after the write is executed on the lower increment register.

Note:	The increment buffer registers are not user-accessible.

EQUATION 20-1:

$$F_{OVERFLOW} = \frac{NCO\ Clock\ Frequency \times Increment\ Value}{2^n}$$

n = Accumulator width in bits

22.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}$/VPP
- VDD
- VSS

In Program/Verify mode the Program Memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the **"***PIC10(L)F320/322 Flash Memory Programming Specification*" (DS41572).

22.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low then raising the voltage on $\overline{MCLR}$/VPP to VIHH.

22.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

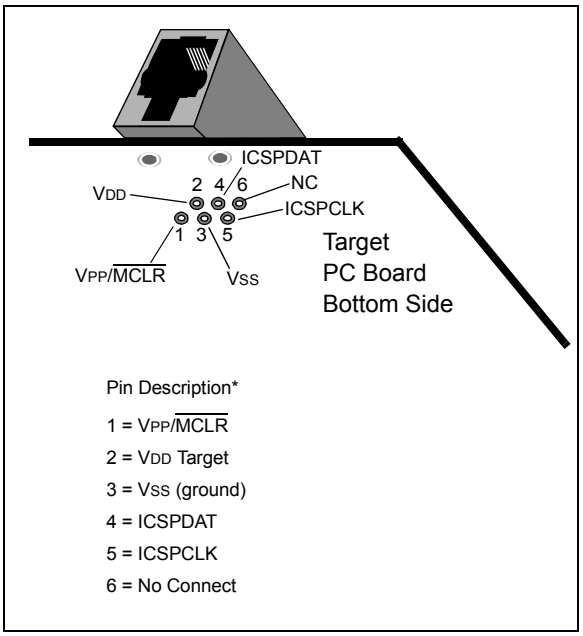
If low-voltage programming is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 5.4 "Low-Power Brown-out Reset (LPBOR)"** for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

22.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP™ header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6 connector) configuration. See Figure 22-1.

FIGURE 22-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 22-2.

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<3:0>) → (destination<7:4>),
(f<7:4>) → (destination<3:0>)

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Description: The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (destination)

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

TABLE 24-2: SUPPLY VOLTAGE (I_{DD})(1,2)

PIC10LF320/322			Standard Operating Conditions (unless otherwise stated)				
PIC10F320/322							
Param No.	Device Characteristics	Min.	Typ†	Max.	Units	Conditions	
						V_{DD}	Note
D013		—	34	45	µA	1.8	F_{OSC} = 500 kHz EC mode
		—	60	105	µA	3.0	
D013		—	76	101	µA	2.3	F_{OSC} = 500 kHz EC mode
		—	110	148	µA	3.0	
		—	153	211	µA	5.0	
D014		—	190	290	µA	1.8	F_{OSC} = 8 MHz EC mode
		—	350	500	µA	3.0	
D014		—	290	430	µA	2.3	F_{OSC} = 8 MHz EC mode
		—	395	600	µA	3.0	
		—	480	775	µA	5.0	
D015		—	0.8	1.3	mA	3.0	F_{OSC} = 20 MHz EC mode
		—	1.1	1.8	mA	3.6	
D015		—	0.8	1.4	mA	3.0	F_{OSC} = 20 MHz EC mode
		—	1.1	1.8	mA	5.0	
D016		—	2.2	4.1	µA	1.8	F_{OSC} = 32 kHz LFINTOSC mode, 85°C
		—	3.9	6.5	µA	3.0	
D016		—	31	44	µA	2.3	F_{OSC} = 32 kHz LFINTOSC mode, 85°C
		—	40	57	µA	3.0	
		—	71	117	µA	5.0	
D016A		—	3.2	4.5	µA	1.8	F_{OSC} = 32 kHz LFINTOSC mode, 125°C
		—	4.8	7.0	µA	3.0	
D016A		—	31	44	µA	2.3	F_{OSC} = 32 kHz LFINTOSC mode,125°C
		—	40	57	µA	3.0	
		—	71	117	µA	5.0	

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: CLKIN = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

TABLE 24-4: I/O PORTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
		I/O PORT:					
D032		with TTL buffer	—	—	0.8	V	$4.5V \le V_{DD} \le 5.5V$
D032A			—	—	0.15 V_{DD}	V	$1.8V \le V_{DD} \le 4.5V$
D033		with Schmitt Trigger buffer	—	—	0.2 V_{DD}	V	$2.0V \le V_{DD} \le 5.5V$
D034		$\overline{MCLR}$	—	—	0.2 V_{DD}	V	
	V_{IH}	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer	2.0	—	—	V	$4.5V \le V_{DD} \le 5.5V$
D040A			0.25 V_{DD} + 0.8	—	—	V	$1.8V \le V_{DD} \le 4.5V$
D041		with Schmitt Trigger buffer	0.8 V_{DD}	—	—	V	$2.0V \le V_{DD} \le 5.5V$
D042		$\overline{MCLR}$	0.8 V_{DD}	—	—	V	
	I_{IL}	**Input Leakage Current(2)**					
D060		I/O ports	—	± 5	± 125	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance @ 85°C
				± 5	± 1000	nA	125°C
D061		$\overline{MCLR}$	—	± 50	± 200	nA	$V_{SS} \le V_{PIN} \le V_{DD}$ @ 85°C
	I_{PUR}	**Weak Pull-up Current**					
D070*			25	100	200		V_{DD} = 3.3V, V_{PIN} = V_{SS}
			25	140	300	μA	V_{DD} = 5.0V, V_{PIN} = V_{SS}
	V_{OL}	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	I_{OL} = 8mA, V_{DD} = 5V I_{OL} = 6mA, V_{DD} = 3.3V I_{OL} = 1.8mA, V_{DD} = 1.8V
	V_{OH}	**Output High Voltage**					
D090		I/O ports	V_{DD} - 0.7	—	—	V	I_{OH} = 3.5mA, V_{DD} = 5V I_{OH} = 3mA, V_{DD} = 3.3V I_{OH} = 1mA, V_{DD} = 1.8V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

FIGURE 24-5: CLOCK TIMING

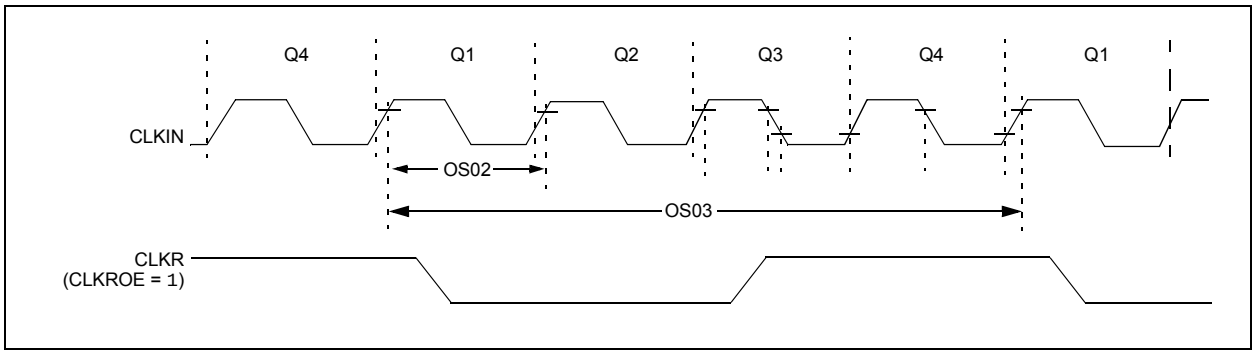


TABLE 24-6: CLOCK OSCILLATOR TIMING REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS01	FOSC	External CLKIN Frequency(1)	DC	—	20	MHz	EC mode
OS02	TOSC	External CLKIN Period(1)	31.25	—	∞	ns	EC Oscillator mode
OS03	TCY	Instruction Cycle Time(1)	200	TCY	DC	ns	TCY = 4/FOSC

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TCY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

TABLE 24-7: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**	**Freq. Tolerance**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	±3% -8 to +4%	— —	16.0 16.0	— —	MHz MHz	0°C ≤ TA ≤ +85°C, VDD ≥ 2.3V -40°C ≤ TA ≤ 125°C
OS09	LFOSC	Internal LFINTOSC Frequency	±25%	—	31	—	kHz	
OS10*	TWARM	HFINTOSC Wake-up from Sleep Start-up Time	—	—	5	8	µs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

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