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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	40
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	80-PQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p80c557e4efb-01-55

3. ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			FREQUENCY RANGE (MHz)	TEMPERATURE RANGE (°C)
	NAME	DESCRIPTION	CODE		
ROMless					
P80C557E4EBB	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	0 to +70
P80C557E4EFB	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	–40 to +85
ROM coded					
P83C557E4EBB/YYY[1]	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	0 to +70
P83C557E4EFB/YYY[1]	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	–40 to +85
FEEPROM					
P89C557E4EBB	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	0 to +70
P89C557E4EFB	QFP80	Plastic Quad Flat Pack; 80 leads	SOT318-1	3.5 to 16	–40 to +85

NOTE:
1. YYY denotes the ROM code number

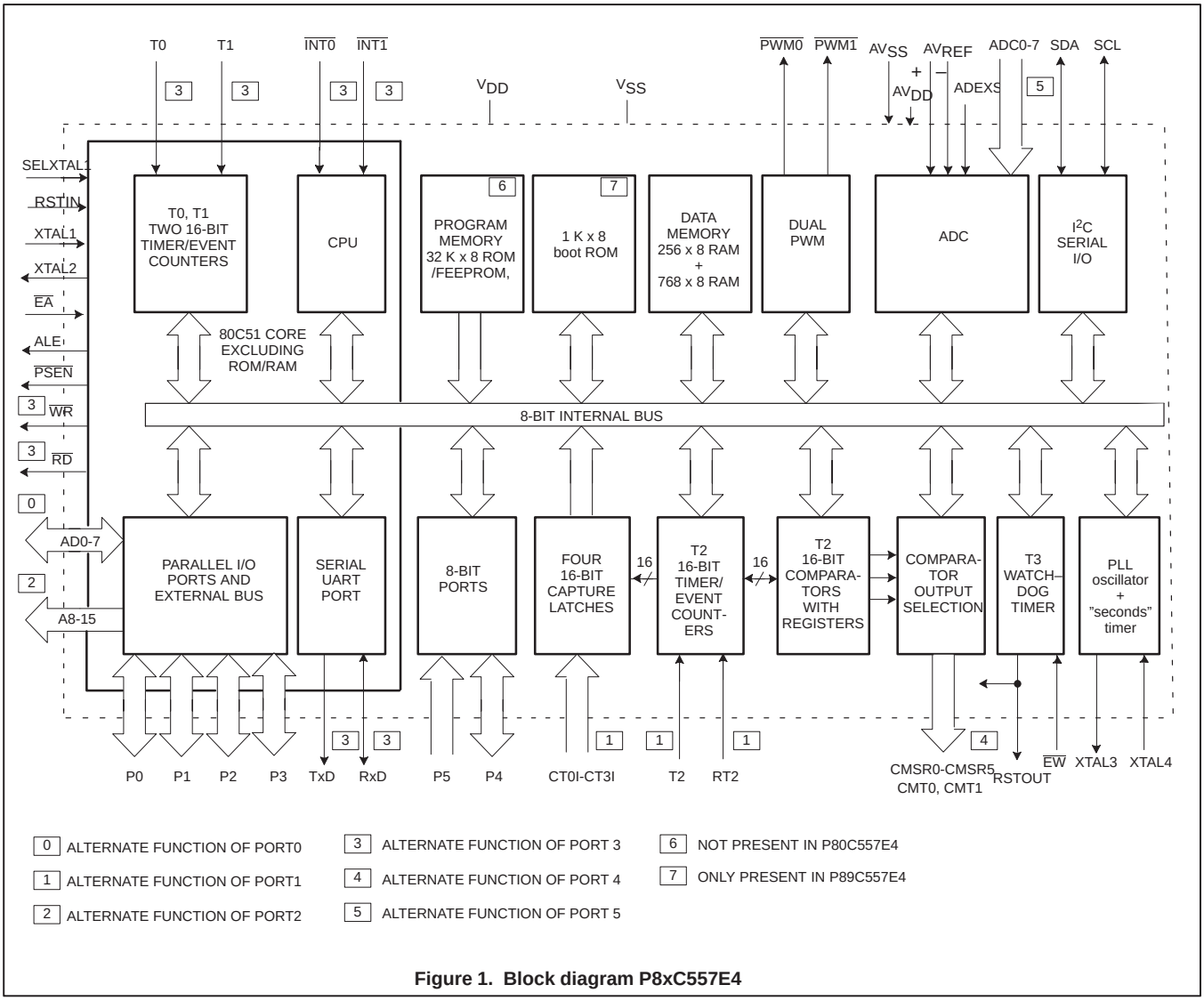


Figure 1. Block diagram P8xC557E4

4.1 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
AV_{ref-} AV_{ref+}	1 2	**Low end** of analog to digital conversion reference resistor **High end** of analog to digital conversion reference resistor.
AV_{SS1} AV_{DD1}	3 4	**Analog** ground for ADC **Analog** power supply (+5 V) for ADC
AV_{SS2} AV_{DD2}	77 76	**Analog** ground; for PLL oscillator **Analog** power supply; (+5 V) for PLL oscillator
P5.7 – P5.0	5 – 12	**Port 5** 8-bit input port Port pin — Alternative function P5.0–P5.7 — Eight input channels to ADC (ADC0–ADC7)
V_{DD1}, V_{DD2}, V_{DD3}, V_{DD4}	14, 28, 53, 66	**Digital power supply:** +5 V power supply pins during normal operation and power reduction modes. All pins must be connected.
V_{SS1}, V_{SS2} V_{SS3}, V_{SS4}	13, 29, 54, 67	**Digital ground:** circuit ground potential. All pins must be connected.
ADEXS	15	**Start ADC operation:** Input starting analog to digital conversion triggered by a programmable edge (ADC operation can also be started by software). This pin must not float
$\overline{PWM0}$	16	**Pulse width modulation** output 0
$\overline{PWM1}$	17	**Pulse width modulation** output 1
$\overline{EW}$	18	**Enable watchdog timer:** Enable for T3 watchdog timer and disable Power-down Mode.This pin must not float.
P4.0 – P4.7	19 – 22 24 – 27	**Port 4** 8-bit quasi-bidirectional I/O port Port pin — Alternative function P4.0 — CMSR0 } P4.1 — CMSR1 } P4.2 — CMSR2 } compare and set/reset P4.3 — CMSR3 } outputs on a match with timer T2 P4.4 — CMSR4 } P4.5 — CMSR5 } P4.6 — CMT0 } compare and toggle outputs P4.7 — CMT1 } on a match with timer T2
RSTIN	30	**Reset:** Input to reset the P8xC557E4.
RSTOUT	23	**Reset:** Output of the P8xC557E4 for resetting peripheral devices during initialization and Watchdog Timer overflow.
P1.0 – P1.7	31 – 38	**Port 1** 8-bit quasi-bidirectional I/O port Port pin — Alternative function P1.0 — CT0I/INT2} P1.1 — CT1I/INT3} : Capture timer inputs for P1.2 — CT2I/INT4} timer T2 or external interrupt inputs P1.3 — CT3I/INT5} P1.4 — T2 : T2 event input, rising edge triggered P1.5 — RT2 : T2 timer reset input, rising edge triggered P1.6 P1.7
SCL	39	**I^2C-bus serial clock** I/O port
SDA	40	**I^2C-bus serial data** I/O port If SCL and SDA are not used, they must be connected to V_{SS}.

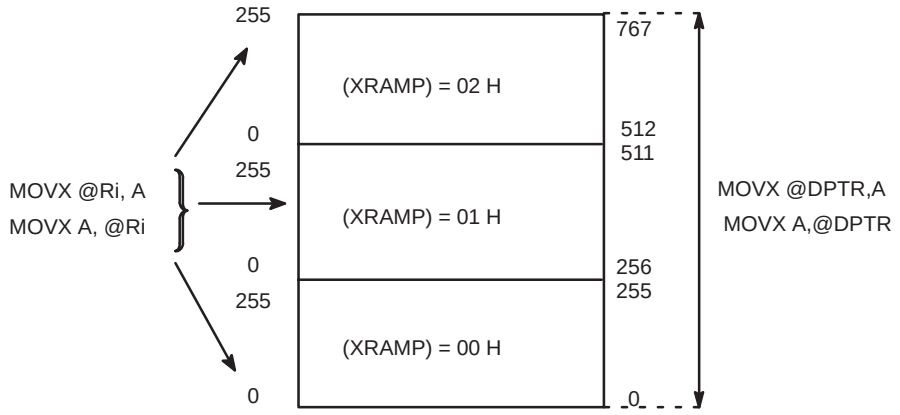


Figure 5. Indirect addressing of AUX-RAM (768 Bytes), ARD bit in PCON = 0

6.2.2.1 AUX-RAM Page Register XRAMP

The AUX-RAM Page Register is used to select one of three 256 bytes pages of the internal 768 bytes AUX-RAM for MOVX-accesses via R0 or R1. Its reset value is (XXXXXX00).

	7	6	5	4	3	2	1	0
XRAMP (FAH)	x	x	x	x	x	x	XRAMP1	XRAMP0

x: undefined during read, a write operation must write “0” to these locations

Figure 6. AUX-RAM page register.

Table 3. Description of XRAMP Bits

BIT	SYMBOL	FUNCTION
XRAMP.2–7	XRAMPx	reserved for future use
XRAMP.1	XRAMP1	AUX-RAM page select bit 1
XRAMP.0	XRAMP0	AUX-RAM page select bit 0

Table 4. Memory Locations for All Possible MOVX Accesses

ARD[1]	XRAMP1	XRAMP0	MOVX @Ri,A and MOVX A,@Ri instructions access:
0	0	0	AUX-RAM locations 0 .. 255 (reset condition)
0	0	1	AUX-RAM locations 256 .. 511
0	1	0	AUX-RAM locations 512 .. 767
0	1	1	no valid memory access; reserved for future use
1	X	X	External RAM locations 0 .. 255
			MOVX @DPTR,A and MOVX A,@DPTR instructions access:
0	X	X	AUX-RAM locations 0 .. 767 (reset condition) External RAM locations 768 .. 65535
1	X	X	External RAM locations 0 .. 65535

NOTE:
1. ARD (AUX-RAM Disable) is a bit in the Special Function Register PCON

Digital Input Port Register P5

Port 5 Special Function Register P5 always represents the binary value of the logic level at input pins P5.0/ADC0...P5.7/ADC7. P5 is not affected by chip reset. P5 is a read only register. Its hardware address is C7H. P5 is not bit addressable.

Reading Special Function Register P5 does not affect A/D conversions. But it is recommended to use the digital input port function of the hardware Port 5 only as an alternative to analog input voltage conversions. Simultaneous mixed operation is discouraged for the sake of A/D conversion result reliability and accuracy.

For further information on Port 5, refer to the “I/O facilities” section.

For further information on A/D Special Function Registers, refer to the “Internal Data Memory” section.

	7	6	5	4	3	2	1	0
P5 (C7H)	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0

Figure 18. Digital input port register P5.

Reset

After a RESET of the microcontroller the ADCON and ADPSS register bits are initialized to zero. Registers ADRSLn and ADRSH are not initialized by a RESET.

Idle and Power-down Mode

The A/D Converter is active only when the microcontroller is in normal operating mode. If the Idle or Power-down Mode is activated, then the ADC is switched off and put into a power saving idle state – a conversion in progress is aborted, a previously set ADSST flag is cleared and the internal clock is halted. The conversion result registers are not affected.

The interrupt flag ADINT will not be set by activation of Idle or Power-down Mode. A previously set flag ADINT will not be cleared by the hardware. (Note: ADINT cannot be cleared by hardware at all, except for a RESET – it must be cleared by the user software.)

After a wakeup from Idle or Power-down Mode a set flag ADINT indicates that at least one autoscan loop was finished completely before the microcontroller was put into the respective power reduction mode and it indicates that the stored result data may be fetched now – if desired.

For further information on Idle and Power-down Mode, refer to the “Power reduction modes” section.

Timing

A programmable prescaler is controlled by the bits ADPR1 and ADPR0 in register ADCON to adapt the conversion time for different microcontroller clock frequencies.

Table 11 shows conversion times (tconv) for one A/D conversion at some convenient system clock frequencies (fclk) and ADC prescaler divisors (m), which are user selectable by the bits ADCON.7/ADPR1 and ADCON.6/ADPR0.

For conversion times outside the limits for tconv the specified ADC characteristics are not guaranteed; (prohibited conversion times are put in brackets):

Table 11. Conversion time configuration examples (tconv/μs)

m	f_{CLK}			
	6 MHz	8 MHz	12 MHz	16 MHz
2	26	19.5	[13]	[9.75]
4	50	37.5	25	18.75
6	[74]	[55.5]	37	27.75
8	[98]	[73.5]	49	36.75

Conversion time tconv = (6 m + 1) machine cycles

A conversion time tconv consists of one sample time period (which equals two bit conversion times), 10 bit conversion time periods and one machine cycle to store the result.

After result storage an extra initializing time period follows to select the next analog input channel (according to the contents of SFR ADPSS), before the input signal is sampled.

Thus the time period between two adjacent conversions within an autoscan loop is larger than the pure time tconv. This autoscan cycle time is (7 m) machine cycles.

At the start of an autoscan conversion the time between writing to SFR ADCON and the first analog input signal sampling depends on the current prescaler value (m) and the relative time offset between this write operation and the internal (divided) ADC clock. This gives a variation range for the A/D conversion start time of (m / 2) machine cycles.

6.6.2 Configuration and Operation

Every A/D conversion is an autoscan conversion. The two user selectable general operation modes are continuous scan and one-time scan mode.

The desired analog input port channel/s for conversion is/are selected by programming A/D input port scan-select bits in SFR ADPSS. An analog input channel is included in the autoscan loop if the corresponding bit in ADPSS is 1, a channel is skipped if the corresponding bit in ADPSS is 0.

An autoscan is always started according to the lowest bit position of ADPSS that contains a 1.

An autoscan conversion is started by setting the flag ADSST in register ADCON either by software or by an external start signal at input pin ADEXS, if enabled. Either no edge (external start totally disabled), a rising edge or/and a falling edge of ADEXS is selectable for external conversion start by the bits ADSRE and ADSFE in register ADCON.

After completion of an A/D conversion the 10-bit result is stored in the corresponding 10-bit buffer register. Then the next analog input is selected according to the next higher set bit position in ADPSS, converted and stored, and so on. When the result of the last conversion of this autoscan loop is stored, flag ADCON.4/ADINT, the ADC interrupt flag, is set. It is not cleared by interrupt hardware – it must be cleared by software.

In continuous scan mode (ADCON.2/ADCSA=1) the ADC start and status flag ADCON.3/ADSST retains the set state and the autoscan loop restarts from the beginning. In one-time scan mode (ADCSA=0) conversions stop after the last selected analog input was converted, ADINT is set and ADSST is cleared automatically.

ADSST cannot be set (neither externally nor by software) as long as ADINT=1, i.e. as long as ADINT is set, a new conversion start – by setting flag ADSST – is inhibited; actually it is only delayed until ADINT is cleared.

(If a '1' is written to ADSST while ADINT=1, this new value is internally latched and preserved, not setting ADSST until ADCON.4/ADINT=0. In this state, a read of SFR ADCON will display ADCON.3/ADSST=0, because always the effective ADC status is read.)

Note that under software control the analog inputs can also be converted in arbitrary order, when one-time scan mode is selected and in SFR ADPSS only one bit is set at a time. In this case ADINT is set and ADSST is cleared after every conversion.

6.6.3 Resolution and Characteristics

The ADC system has its own analog supply pins AV_{DD} and AV_{SS}. It is referenced by two special reference voltage input pins sourcing the resistance ladder of the DAC: AV_{ref+} and AV_{ref-}. The voltage between AV_{REF+} and AV_{REF-} defines the full-scale range. Due to the 10-bit resolution the full scale range is divided into 1024 unit steps. The unit step voltage is 1 LSB, which is typically 5 mV (AV_{ref+} = 5.12 V, AV_{ref-} = 0 V = AV_{SS}).

The DAC's resistance ladder has 1023 equally spaced taps, separated by a unit resistance 'R'. The first tap is located 0.5 x R above AV_{ref-}, the last tap is located 1.5 x R below AV_{ref+}. This results in a total ladder resistance of 1024 x R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error. For input voltages between AV_{ref-} and (AV_{ref-} + 1/2 LSB) the 10-bit conversion result code will be 00 0000 0000 B = 000H = 0D. For input voltages between (AV_{ref+} – 3/2 LSB) and AV_{ref+} the 10-bit conversion result code will be 11 1111 1111 B = 3FFH = 1023D.

The result code corresponding to an analog input voltage (AV_{in}) can be calculated from the formula:

$$\text{ResultCode} = 1024 \times \frac{AV_{IN} - AV_{ref-}}{AV_{ref+} - AV_{ref-}}$$

The analog input voltage should be stable when it is sampled for conversion. At any times the input voltage slew rate must be less than 10 V/ms (5 V conversion range) in order to prevent an undefined result.

This maximum input voltage slew rate can be ensured by an RC low pass filter with R = 2k2 and C = 100 nF. The capacitor between analog input pin and analog ground pin shall be placed close to the pins in order to have maximum effect in minimizing input noise coupling.

6.7 Timer/Counters

The P8xC557E4 contains three 16-bit timer/event counters: Timer 0, Timer 1 and Timer T2 and one 8-bit timer, T3. Timer 0 and Timer 1 may be programmed to carry out the following functions:

- Measure time intervals and pulse durations
- Count events
- Generate interrupt requests

6.7.1 Timer 0 and Timer 1

Timers 0 and 1 each have a control bit in SFR TMOD that selects the timer or counter function of the corresponding timer.

In the timer function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the counter function, the register is incremented in response to a 1-to-0 transition at the corresponding external input pin, T0 or T1. In this function, the external input is sampled during S5P2 of every machine cycle. When the samples show a HIGH in one cycle and a LOW in the next cycle, the counter is incremented. Thus, it takes two machine cycles (24 oscillator periods) to recognize a 1-to-0 transition. There are no restrictions on the duty cycle of the external input signal, but to insure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 0 and Timer 1 can be programmed independently to operate in one of four modes:

- **Mode 0:**
  8-bit timer or 8-bit counter each with divide-by-32 prescaler
- **Mode 1:**
  16-bit time-interval or event counter
- **Mode 2:**
  8-bit time-interval or event counter with automatic reload upon overflow
- **Mode 3:**
  –Timer 0: one 8-bit time-interval or event counter and one 8-bit time-interval counter
  –Timer 1: stopped

	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0

Figure 22. T2 control register (TM2CON).

Table 15. Description of TM2CON bits

SYMBOL	BIT	FUNCTION
T2IS1	TM2CON.7	Timer T2 16-bit overflow interrupt select
T2IS0	TM2CON.6	Timer T2 byte overflow interrupt select
T2ER	TM2CON.5	Timer T2 external reset enable. When this bit is set, Timer T2 may be reset by a rising edge on RT2 (P1.5).
T2BO	TM2CON.4	Timer T2 byte overflow interrupt flag
T2P1	TM2CON.3	Timer T2 prescaler select
T2P0	TM2CON.2	
T2MS1	TM2CON.1	Timer T2 mode select
T2MS0	TM2CON.0	

Table 16. Timer 2 prescaler select

T2P1	T2P0	TIMER T2 CLOCK
0	0	Clock source
0	1	Clock source/2
1	0	Clock source/4
1	1	Clock source/8

Table 17. Timer 2 mode select

T2MS1	T2MS0	MODE SELECTED
0	0	Timer T2 halted (off)
0	1	T2 clock source = $f_{CLK}/12$
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

	7	6	5	4	3	2	1	0
CTCON (EBH)	CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN0	CTP0

Figure 23. Capture control register (CTCON).

Table 18. Description of CTCON bits

SYMBOL	BIT	FUNCTION
CTN3	CTCON.7	Capture Register 3 triggered by a falling edge on CT3I
CTP3	CTCON.6	Capture Register 3 triggered by a rising edge on CT3I
CTN2	CTCON.5	Capture Register 2 triggered by a falling edge on CT2I
CTP2	CTCON.4	Capture Register 2 triggered by a rising edge on CT2I
CTN1	CTCON.3	Capture Register 1 triggered by a falling edge on CT1I
CTP1	CTCON.2	Capture Register 1 triggered by a rising edge on CT1I
CTN0	CTCON.1	Capture Register 0 triggered by a falling edge on CT0I
CTP0	CTCON.0	Capture Register 0 triggered by a rising edge on CT0I

The contents of the Compare Registers CM0, CM1 and CM2 are continuously compared with the counter value of Timer T2. When a match occurs, an interrupt may be invoked. A match of CM0 sets the bits 0–5 of Port 4, a CM1 match resets these bits and a CM2 match toggles bits 6 and 7 of Port 4, provided these functions are enabled by the STE respectively RTE registers. A match of CM0 and CM1 at the same time results in resetting bits 0–5 of Port 4. CM0, CM1 and CM2 are reset by the RSTIN signal.

	7	6	5	4	3	2	1	0
TM2IR (C8H)	T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0

Figure 24. Interrupt flag register (TM2IR).

Table 19. Description of TM2IR bits

SYMBOL	BIT	FUNCTION
T2OV	TM2IR.7	Timer T2 16-bit overflow interrupt flag
CMI2	TM2IR.6	CM2 interrupt flag
CMI1	TM2IR.5	CM1 interrupt flag
CMI0	TM2IR.4	CM0 interrupt flag
CTI3	TM2IR.3	CT3 interrupt flag
CTI2	TM2IR.2	CT2 interrupt flag
CTI1	TM2IR.1	CT1 interrupt flag
CTI0	TM2IR.0	CT0 interrupt flag

6.8 Watchdog Timer T3

In addition to Timer T2 and the standard timers, a watchdog timer (T3) consisting of an 11-bit prescaler and an 8-bit timer is also incorporated (see Figure 27).

The timer is incremented every 1.5 ms, derived from the system clock frequency of 16 MHz by the following:

$$f_{timer} = \frac{f_{CLK}}{12 \times 2048}$$

When a timer overflow occurs, the microcontroller is reset and a reset output pulse is generated at pin RSTOUT. Also the PLL control register is reset.

To prevent a system reset the timer must be reloaded in time by the application software. If the processor suffers a hardware/software malfunction, the software will fail to reload the timer. This failure will produce a reset upon overflow thus preventing the processor running out of control.

The watchdog timer can only be reloaded if the condition flag WLE = PCON.4 has been previously set by software.

At the moment the counter is loaded the condition flag is automatically cleared.

The time interval between the timer's reloading and the occurrence of a reset depends on the reloaded value. For example, this may range from 1.5 ms to 0.375 s when using an oscillator frequency of 16 MHz.

In the Idle state the watchdog timer and reset circuitry remain active.

The watchdog timer is controlled by the watchdog enable pin ($\overline{EW}$). A LOW level enables the watchdog timer and disables the Power-down Mode. A HIGH level disables the watchdog timer and enables the Power-down Mode.

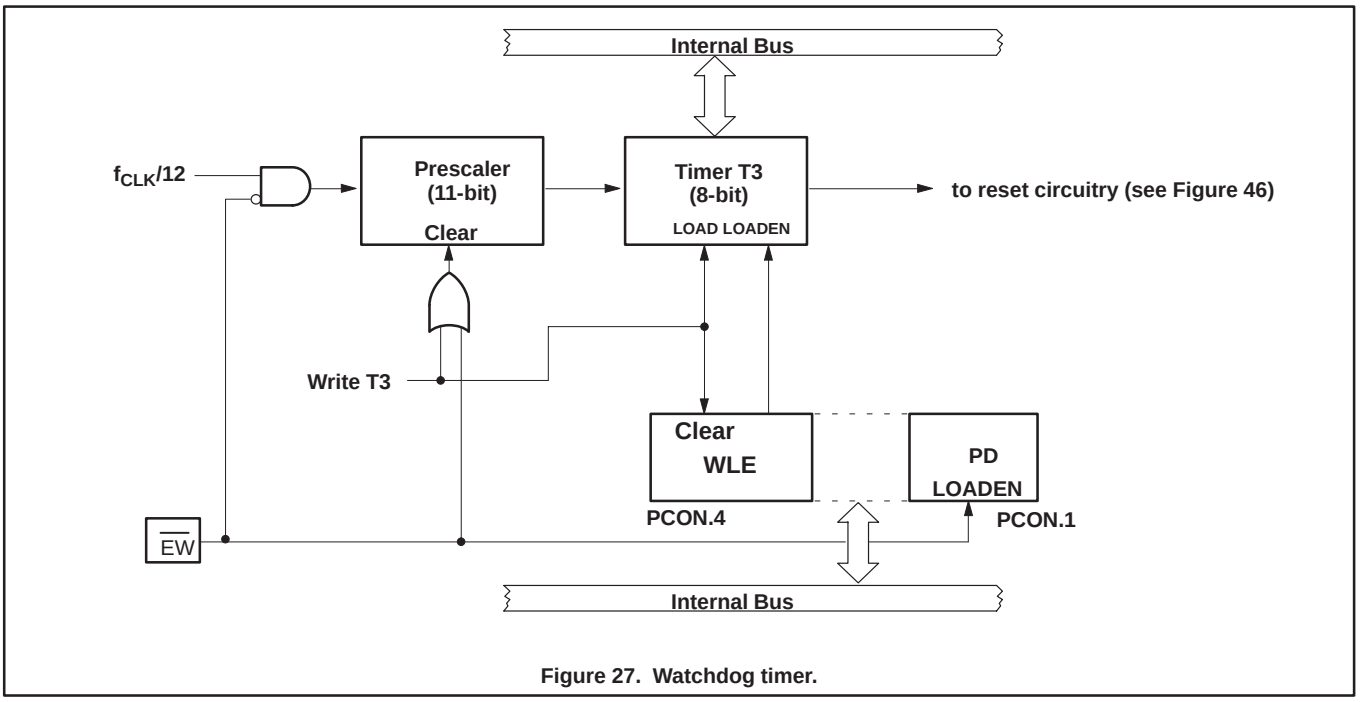


Figure 27. Watchdog timer.

6.9 Serial I/O

The P8xC557E4 is equipped with two independent serial ports: SIO0 and SI01. SIO0 is the full duplex UART port, identical to the PCB80C51 serial port. SIO1 is an I^2C-bus serial I/O interface with byte oriented master and slave functions.

6.9.1 SIO0 (UART)

SIO 0 is a full duplex serial I/O port – it can transmit and receive simultaneously. This serial port is also receive-buffered. It can commence reception of a second byte before the previously received byte has been read from the receive register. If, however, the first byte has still not been read by the time reception of the second byte is complete, one of the bytes will be lost. The SIO0 receive and transmit registers are both accessed via the S0BUF special function register. Writing to S0BUF loads the transmit register, and reading S0BUF accesses to a physically separate receive register. SIO0 can operate in 4 modes:

Mode 0: Serial data is transmitted and received through RXD. TXD outputs the shift clock. 8 data bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 of the oscillator frequency. A write into S0CON should be avoided during a transmission to avoid spikes on RXD/TXD.

Mode 1: 10 bits are transmitted via TXD or received through RXD: a start bit (0), 8 data bits (LSB first), and a stop bit(1). On receive, the stop bit is put into RB8 (S0CON special function register). The baud rate is variable.

Mode 2: 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On transmit, the 9th data bit (TB8 in S0CON) can be assigned the value of 0 or 1. With nominal software, TB8 can be the parity bit (P in PSW). During a receive, the 9th data bit is stored in RB8 (S0CON), and the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 of the oscillator frequency.

Mode 3: 11 bits are transmitted through TXD or received through RXD: a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). Mode 3 is the same as Mode 2 except the baud rate which is variable in Mode 3.

In all four modes, transmission is initiated by any instruction that writes to the S0BUF function register. Reception is initiated in Mode 0 when RI = 0 and REN = 1. In the other three modes, reception is initiated by the incoming start bit provided that REN = 1.

Modes 2 and 3 are provided for multiprocessor communications. In these modes, 9 data bits are received with the 9th bit written to RB8. The 9th bit is followed by the stop bit. The port can be programmed so that with receiving the stop bit, the serial port interrupt will be activated if, and only if RB8 = 1.

This feature is enabled by setting bit SM2 in S0CON. This feature may be used in multiprocessor systems.

For more information about how to use the UART in combination with the registers S0CON, PCON, IEN0, S0BUF and Timer register refer to the 80C51 Data Handbook IC20.

	7	6	5	4	3	2	1	0
S0CON (98H)	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Figure 28. Serial port control (S0CON) register.

Table 22. Description of S0CON bits

SYMBOL	BIT	FUNCTION
SM0	S0CON.7	This bit is used to select the serial port mode. See Table 23.
SM1	S0CON.6	This bit is used to select the serial port mode. See Table 23.
SM2	S0CON.5	Enables the multiprocessor communication feature in modes 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0.
REN	S0CON.4	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	S0CON.3	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	S0CON.2	In modes 2 and 3, RB8 is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	S0CON.1	The transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	S0CON.0	The receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

The polling cycle is repeated with every machine cycle, and the values polled are the values present at S5P2 of the previous machine cycle. Note that if an interrupt flag is active but is not being responded to because of one of the above conditions, and if the flag is inactive when the blocking condition is removed, then the blocked interrupt will not be serviced. Thus, the fact that the interrupt flag was once active but not serviced is not remembered. Every polling cycle is new.

The processor acknowledges an interrupt request by executing a hardware-generated LCALL to the appropriate service routine. In some cases it also clears the flag which generated the interrupt, and in others it does not. It clears the Timer 0, Timer 1, and external interrupt flags. An external interrupt flag (IE0 or IE1) is cleared only if it was transition-activated. All other interrupt flags are not cleared by hardware and must be cleared by the software. The LCALL pushes the contents of the program counter on to the stack (but it does not save the PSW) and reloads the PC with an address that depends on the source of the interrupt being vectored to as shown in Table 38.

Execution proceeds from the vector address until the RETI instruction is encountered. The RETI instruction clears the “priority level active” flip-flop that was set when this interrupt was acknowledged. It then pops the top two bytes from the stack and reloads the program counter. Execution of the interrupted program continues from where it was interrupted.

	7	6	5	4	3	2	1	0
IEN0 (A8H)	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0

Figure 34. Interrupt enable register (IEN0).

Table 33. Description of IEN0 bits

SYMBOL	BIT	FUNCTION
EA	IEN0.7	Global enable/disable control 0 = No interrupt is enabled 1 = Any individually enabled interrupt will be accepted
EAD	IEN0.6	Enable ADC interrupt
ES1	IEN0.5	Enable SIO1 (I^2C) interrupt
ES0	IEN0.4	Enable SIO0 (UART) interrupt
ET1	IEN0.3	Enable Timer 1 interrupt
EX1	IEN0.2	Enable External interrupt 1 / Seconds interrupt
ET0	IEN0.1	Enable Timer 0 interrupt
EX0	IEN0.0	Enable External interrupt 0

	7	6	5	4	3	2	1	0
PCON (87H)	SMOD	ARD	RFI	WLE	GF1	GF0	PD	IDL

Figure 39. Power control register (PCON).

Table 39. Description of PCON bits

SYMBOL	BIT	FUNCTION
SMOD	PCON.7	Double Baud rate bit. When set to logic 1 the baud rate is doubled when the serial port SIO0 is being used in modes 1, 2, or 3.
ARD	PCON.6	AUX-RAM disable bit. When set to a 1 the internal 768 bytes AUX-RAM is disabled, so that all MOVX-Instructions access the external data memory – as it is with the standard PCB80C51.
RFI	PCON.5	Reduced radio frequency interference bit. When set to a 1 the toggling of ALE pin is prohibited. This bit is cleared on RESET (see also sections Features (EMC) and Pinning).
WLE	PCON.4	Watchdog load enable. This flag must be set by software prior to loading timer T3 (watchdog timer). It is cleared when timer T3 is loaded.
GF1	PCON.3	General-purpose flag bit
GF0	PCON.2	General-purpose flag bit
PD	PCON.1	Power-down bit. Setting this bit activates the power-down mode. It can only be set if input $\overline{EW}$ is high.
IDL	PCON.0	Idle Mode bit. Setting this bit activates the Idle Mode.

6.11 Power Reduction Modes

Two software-selectable modes of reduced power consumption are implemented. These are the Idle Mode and the Power-down Mode.

Idle Mode operation permits the interrupt, serial ports and timer blocks T0, T1 and T3 to function while the CPU is halted. The following functions are switched off when the microcontroller enters the Idle Mode:

- CPU (halted)
- Timer 2 (stopped and reset)
- PWM0, PWM1 (reset, output = HIGH)
- ADC (aborted if conversion in progress)

The following functions remain active during Idle Mode. These functions may generate an interrupt or reset and thus terminate the Idle Mode:

- Timer 0, Timer 1, Timer 3 (Watchdog timer)
- UART
- I^2C
- External interrupt
- Seconds Timer

In Power-down Mode the system clock is halted. If the PLL oscillator is selected (SELXTAL1 = 0) and the RUN32 bit is set, the 32 kHz oscillator keeps running, otherwise it is stopped. If the HF-oscillator (SELXTAL1 = 1) is selected, it is stopped after setting the bit PD in the PCON register.

Table 40. External Pin Status During Idle and Power-Down Modes

MODE	MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	SCL/SDA	$\overline{PWM0}$/$\overline{PWM1}$
Idle	Internal	1	1	data	data	data	data	data	operative (1)	HIGH
Idle	External	1	1	high-Z	data	address	data	data	operative (1)	HIGH
Power-down	Internal	0	0	data	data	data	data	data	high-Z	HIGH
Power-down	External	0	0	high-Z	data	data	data	data	high-Z	HIGH

NOTE:
1. In Idle Mode SCL and SDA can be active as outputs only if SIO1 is enabled; if SIO1 is disabled (S1CON.6/ENS1 = 0) these pins are in a high-impedance state.

6.14 Reset Circuitry

The reset input pin RSTIN is connected to a Schmitt trigger for noise reduction (see Figure 46). Is the HF-oscillator selected a Reset is accomplished by holding the RSTIN pin HIGH for at least 2 machine cycles (24 system clock periods). Is the PLL-oscillator selected the RSTIN-pulse must have a width of 1 µs at least, independent of the 32 kHz-oscillator is running or not (see PLL description). The CPU responds by executing an internal reset. The RSTOUT pin represents the signal resetting the CPU and can be used to reset peripheral devices.

The RSTOUT level also could be high due to a Watchdog timer overflow.

The length of the output pulse from T3 is 3 machine cycles. A pulse of such short duration is necessary in order to recover from a processor or system fault as fast as possible.

During Reset, ALE and $\overline{PSEN}$ output a HIGH level. In order to perform a correct reset, this level must not be affected by external elements.

A Reset leaves the internal registers as shown in Table 5.

The internal RAM is not affected by Reset. At power-on, the RAM content is indeterminate.

6.15 Power-on Reset

An automatic Reset can be obtained by switching on V_{DD}, if the RSTIN pin is connected to V_{DD} via a capacitor, as shown in Figure 47.

Is the HF oscillator selected the V_{DD} rise time must not exceed 10 ms and the capacitor should be at least 2.2 µF. The decrease of the RSTIN pin voltage depends on the capacitor and the internal resistor R_{RST}. That voltage must remain above the lower threshold for at minimum the HF-oscillator start-up time plus 2 machine cycles. Is the PLL-oscillator selected a 0.1 µF capacitor is sufficient to obtain an automatic reset.

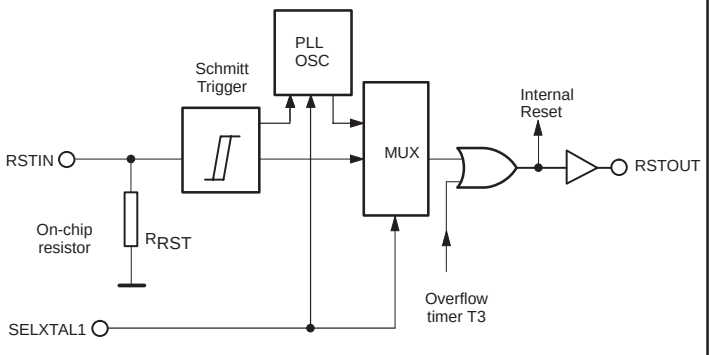


Figure 46. On-chip Reset Configuration

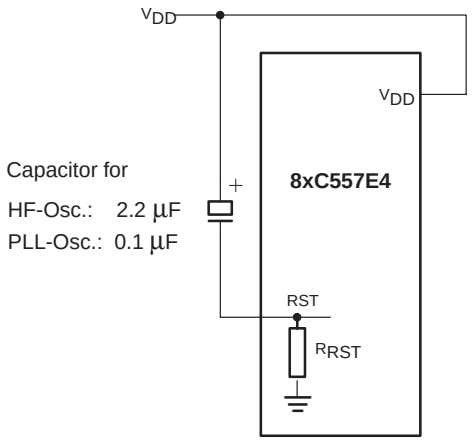


Figure 47. Power-on Reset

Table 43. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	CYCLES	OPCODE (HEX.)
LOGICAL OPERATIONS (Continued)					
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1	64
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1	62
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	2	63
CLR	A	Clear Accumulator	1	1	E4
CPL	A	Complement Accumulator	1	1	F4
RL	A	Rotate Accumulator left	1	1	23
RLC	A	Rotate Accumulator left through the carry	1	1	33
RR	A	Rotate Accumulator right	1	1	03
RRC	A	Rotate Accumulator right through the carry	1	1	13
SWAP	A	Swap nibbles within the Accumulator	1	1	C4
DATA TRANSFER					
MOV	A,Rn	Move register to Accumulator	1	1	E*
MOV	A,direct	Move direct byte to Accumulator	2	1	E5
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1	E6, E7
MOV	A,#data	Move immediate data to Accumulator	2	1	74
MOV	Rn,A	Move Accumulator to register	1	1	F*
MOV	Rn,direct	Move direct byte to register	2	2	A*
MOV	RN,#data	Move immediate data to register	2	1	7*
MOV	direct,A	Move Accumulator to direct byte	2	1	F5
MOV	direct,Rn	Move register to direct byte	2	2	8*
MOV	direct,direct	Move direct byte to direct	3	2	85
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2	86, 87
MOV	direct,#data	Move immediate data to direct byte	3	2	75
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1	F6, F7
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2	A6, A7
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1	76, 77
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	2	90
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to ACC	1	2	93
MOVC	A,@A+PC	Move Code byte relative to PC to ACC	1	2	83
MOVX	A,@Ri	Move AUX-RAM (8-bit addr) to ACC	1	2	E2, E3
MOVX	A,@DPTR	Move AUX-RAM (16-bit addr) to A_{CC}	1	2	E0
MOVX	@Ri,A	Move ACC to AUX-RAM (8-bit addr)	1	2	F2, F3
MOVX	@DPTR,A	Move ACC to AUX-RAM (16-bit addr)	1	2	F0
PUSH	direct	Push direct byte onto stack	2	2	C0
POP	direct	Pop direct byte from stack	2	2	D0
XCH	A,Rn	Exchange register with Accumulator	1	1	C*
XCH	A,direct	Exchange direct byte with Accumulator	2	1	C5
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1	C6, C7
XCHD	A,@Ri	Exchange low-order digit indirect RAM with ACC	1	1	D6, D7

8. FLASH EEPROM

8.1 General

- 32 Kbytes electrically erasable internal program memory with Block-and Page-Erase option (”Flash Memory”).
- Internal fixed boot ROM.
- Up to 32 Kbytes external program memory in combination with the internal FEEPROM ($\overline{EA}$=1).
- Up to 64 Kbytes external program memory if the internal program memory is switched off ($\overline{EA}$=0).

The FEEPROM can be read and written byte-wise. Full Erase, Block Erase, and Page erase will erase 32 Kbytes, 256 bytes and 32 bytes respectively. In-circuit programming and out-of-circuit programming is possible. On-chip erase and write timing generation and on chip high voltage generation contribute to a user friendly interface.

8.2 Features

- Read:
  byte-wise
- Write:
  byte-wise within 2.5 ms.
  (previously erased by a page, block or full erase).
- Erase:
  Page Erase (32 bytes) within 5 ms.
  Block Erase (256 bytes) within 5 ms.
  Full Erase (32 Kbytes) within 5 ms.
  Erased bytes contain FFH.
- Endurance:
  100 erase and write cycles each byte at T_{amb} = 22°C
- Retention:
  10 years
- Out-of-circuit programming:
  Parallel programming with 87C51 compatible hardware Interface to programmer.
- In-circuit programming:
  Serial programming via RS232 interface under boot ROM program control. Auto baud rate selection.
  Intel Hex Object file Format.
  The user program can call routines in the boot ROM for erase, write and verify of the FEEPROM.
- High programming voltage generation: on chip
- Zero point on-chip oscillator and timer to generate the write and erase time durations.
- Programmable security for the code in the FEEPROM to prevent software piracy. The Security Byte is located in the highest address (7FFFH) of the FEEPROM.
- Supply voltage monitoring circuit on-chip to prevent loss of information in the FEEPROM during power-on and power-off.

8.3 Memory Map

Figure 48 shows the memory map of the user program memory and the boot ROM. They are located in the same program address space. Two bits UBS1 and UBS0 of the FEEPROM control special function register FMCON select between the two memory blocks.

User program memory selection
If UBS1 and UBS0 are both 0, then the user program memory is mapped into the 64 K program memory space and the boot ROM cannot be selected. This is the situation after a reset when $\overline{PSEN}$ and ALE have not been pulled down during reset. Program execution starts at 0000H in the internal FEEPROM or in the external program memory dependent on the level of $\overline{EA}$ during reset.

Boot ROM selection
After a reset program execution starts in the boot ROM when during reset $\overline{PSEN}$ and $\overline{EA}$ are pulled down while ALE stay high. The boot ROM size is 1 Kbyte. Besides the serial in-circuit programming routine the boot ROM contains the routines for erase, write and verify of the FEEPROM, which can be called by the user program (LCALL to the address space between 63 K and 64 K).

Switching between user program memory and boot ROM
Switching between user program memory (internal or external) and boot ROM is possible if UBS1 and UBS0 are 0,1. Then in the program memory address space between 0 and 63k the user program memory is selected and in the memory space between 63 K and 64 K the boot ROM is selected.

To switch from user program memory to boot ROM first UBS0 must be set (UBS1 stay 0) and a jump or call instruction to a location >63 K must be executed.

At the moment of crossing the 63 K address border by a return instruction the switching from boot ROM to user memory (internal or external) is performed. After crossing the 63 K address border UBS1 and UBS0 are cleared and the total 64 K memory space is mapped as user program memory. By clearing UBS1 and UBS0, no special requirements to the user program are necessary to do that after a read or erase or write routine.

A small restriction for memory switching is that no memory switching is allowed from or to the address space between 63 K and 64 K of the user program memory because the UBS bits must stay 0 in this range. This restriction can be avoided if the memory switching is always done by a subroutine in the address range between 0 and 63 K.

Description

The user program code in the FEEPROM is executed as in the standard 80C51 microcontroller. Erase and write cycles in the FEEPROM are always performed under control of the boot program in the boot ROM in the address space between 63 K and 64 K. Address and data parameters are passed via DPTR and accumulator A respectively. During an erase or write cycle in the FEEPROM no other access or program execution in the FEEPROM is possible. All interrupts must be disabled when the user program calls a user routine in the boot ROM.

The boot routine for serial programming takes care of addressing, data transfer, verify, high voltage control, error message and return to the user program memory. It also contains the serial communication routine.

The FEEPROM control register FMCON is a special function register. It contains the control bits for verify, write, erase and boot ROM switching.

	7	6	5	4	3	2	1	0
FMCON (FB)	UBS1	UBS0	HV	– [1)]	FCB3	FCB2	FCB1	FCB0

Figure 49. FEEPROM control register.

NOTE:
1. Reserved for future use; a write operation must write “0” to the location.

Table 45. Description of FMCON bits

UBS1	**UBS0**	**User - Boot selection bits**
0	0	User memory mapped from 0 to 64 K.
0	1	User memory mapped from 0 to 63 K. Boot ROM mapped from 63 K to 64 K.
1	0	User memory mapped from 0 to 63 K, but UBS1 bit cleared by hardware in this user address range. Boot ROM mapped from 63 K to 64 K. User software should not write “1” UBS1.
1	1	Boot ROM mapped from 0 to 64 K. User software should not write “1” UBS1.

HV	**High voltage indication bit.** Read only. Is “1” as long as the high voltage for an erase or write operation is present.

FCB3	**FCB2**	**FCB1**	**FCB0**	**Function Code Bits**
0	0	0	0	Value after Reset.
0	1	0	1	Byte Write or byte read (verify)
1	1	0	0	Page Erase (32 bytes boundaries).
0	0	1	1	Block Erase (256 bytes boundaries).
1	0	1	0	Full Erase (32 Kbytes).

The four FCB bits are write protected if the security feature is activated. Then only instructions in the internal program memory (FEEPROM) are able to write FCB (3–0), boot ROM and external program memory instructions cannot change FCB (3–0) except the full erase code can be loaded.

The duration of a write or erase operation is determined by the FEEPROM timer. This timer includes a zero point RC oscillator and cannot be controlled by software.

For calling a user routine in the boot ROM first all interrupts must be disabled and the DPTR and A have to be loaded with the desired values. After setting UBS0 = 1 and UBS1 = 0 and selecting the function via FCB-bits the respective user routine has to be called.

The table below lists the boot ROM user routines, which can be called by the user program. The content of FMCON, A and DPTR before the call is described by “(IN)” and the contents after the return is described by “(OUT)”. The boot ROM user routines do not change other registers or Data memory.

BOOT-ROM ROUTINE	**CALL ADDRESS**	**FMCON (IN)**	**FMCON (OUT)**	**ACC (IN)**	**ACC (OUT)**	**DPTR (IN)**	**DPTR (OUT)**
BYTE_READ	FFBAH	45H	15H	XXH	BYTE	BYTE ADDRESS	BYTE ADDRESS
BYTE_WRITE	FFADH	45H	15H	BYTE	BYTE [(V)]	BYTE ADDRESS	BYTE ADDRESS
PAGE_ERASE	FFAAH	4CH	1CH	XXH	08H	PAGE ADDRESS [1)]	PAGE ADDRESS [2)]
BLOCK_ERASE	FFA5H	43H	13H	XXH	02H	BLOCK ADDRESS [3)]	BLOCK ADDRESS [4)]
FULL_ERASE	FFA0H	4AH	1AH	XXH	0AH	XXXXH	0018H

X = don’t care or not defined
V = verified byte (read back)
1) = 5 LSB’s of DPTR are don’t care
2) = 5 LSB’s of DPTR are “0”
3) = 8 LSB’s of DPTR are don’t care
4) = 8 LSB’s of DPTR contain 08H.

Example of user software (internal or external) that calls the **Page Erase** routine in the boot ROM to erase a page in the FEEPROM (32 bytes) starting at address location 1260H.

```
CLR EA                  ; Disable all interrupts
MOV DPTR, # 1260H       ; Load page-address
MOV FMCON, # 4CH        ; Load Page-Erase code
LCALL 0FFAAH            ; Call Page-Erase routine
                        ; in boot ROM (inherent delay
                          5 ms)
MOV FMCON, #00H         ; Clear FMCON for security
SETB EA                 ; Enable interrupts again
```

Example of user software (internal or external) that calls the **Byte-Write** routine in the boot ROM to write the content of R5 into the FEEPROM address location 1263H.

```
CLR EA                  ; Disable all interrupts
MOV DPTR, # 1263H       ; Load byte address
MOV A, R5               ; Load byte to be written
MOV FMCON, # 45H        ; Load byte-write code
LCALL 0FFADH            ; Call byte-write routine
                        ; in boot ROM (inherent
                          delay 2.5 ms)
MOV FMCON, #00H         ; Clear FMCON for security
SETB EA                 ; Enable interrupts again
XRL A, R5               ; Compare the “read-back” byte
JNZ ERROR               ; Jump if verify error
```

8.4 Security

The security feature protects against software piracy and prevents that the content of the FEEPROM can be read undesirable. The Security Byte is located in the highest address location 7FFFH of the FEEPROM.

The Security Byte should be 50H to activate and 00H or FFH to deactivate the security feature. This security code is chosen in such a way that single bit failures will not deactivate the security feature.

If the security feature is deactivated, then there are no access restrictions to the FEEPROM.

If the security feature is activated, then the external program memory has no access to the FEEPROM with the MOVC instructions. Also bits FCB (3–0) of FMCON cannot be written by external program code or boot ROM code. This prevents in-circuit programming and verification. Only the Full Erase code can be written to FCB (0–3) of FMCON. Note that for the internal program code no restrictions exist if the security feature is activated. At the end of a full erase operation the security feature is deactivated. Also parallel programming and verify is inhibited if the security feature is activated, only a full erase is possible. Note that the security mode does not change immediately when the security code is written into the security byte 7FFFH, but after a reset or power-on. This allows the verification of the loaded code in the FEEPROM, including the Security Byte.

8.5 Parallel Programming

Unlike standard EPROM programming, no high programming supply voltage must be applied to the $\overline{EA}$ pin and only one programming pulse must be applied to the ALE/$\overline{WE}$ pin. The parallel programming mode is entered with the steady signals RST=1, PSEN=0, $\overline{EA}$=1 and SELXTAL1 = 1. The XTAL1,2 clock must have a frequency between 4 and 6MHz. The following table shows the logic levels for programming, erasing, verifying and read signature.

MODE	ALE/$\overline{WE}$	P2.7	P2.6	P3.7	P3.6
Full erase	⊓	1	1	0	1
Program FEEPROM	⊓	1	0	1	1
Verify FEEPROM	1	0	0	1	1
Read signature	1	0	0	0	0

ALE/$\overline{WE}$ Write Enable signal (program/erase), active low
P2.6, P2.7, P3.6, P3.7 control signals

Data and address bits:

P0.0 – P0.7	:	D0 – D7	Program data input / verify or read data output
P1.0 – P1.7	:	A0 – A7	Input low order address bits.
P2.0 – P2.5, P3.4	:	A8 – A14	Input high order address bits.

The P89C557E4 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. These bytes are read by the same procedure as for a normal verification of locations 30H and 31H, except that P3.6 and P3.7 need to be pulled to LOW.

ADDRESS	CONTENT	MEANING
30H	15H	Philips
31H	B5H	P89C557E4

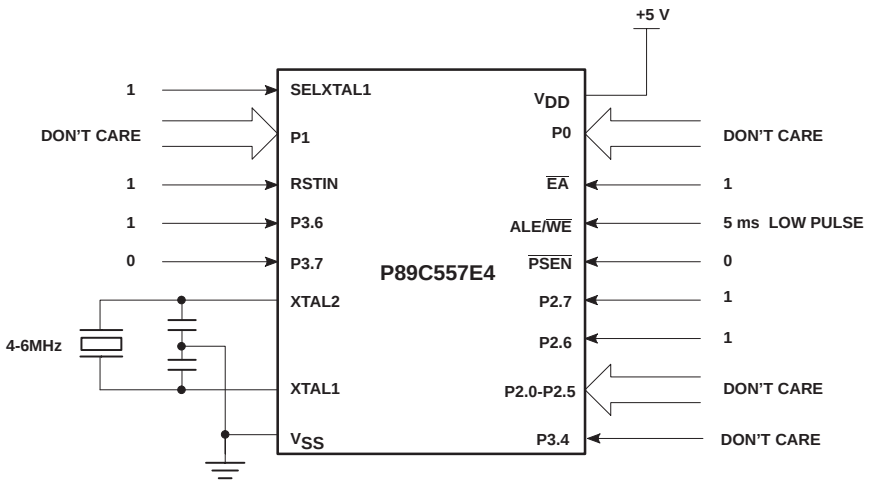


Figure 50. Erase Configuration

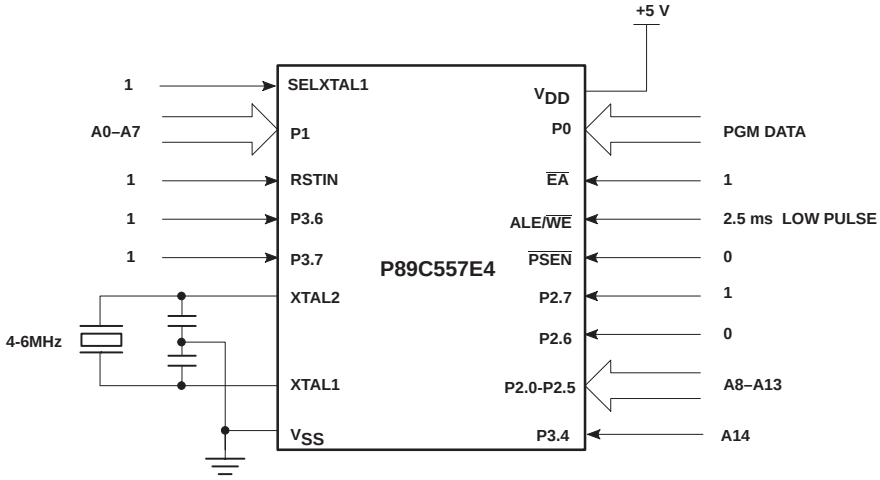


Figure 51. Programming Configuration

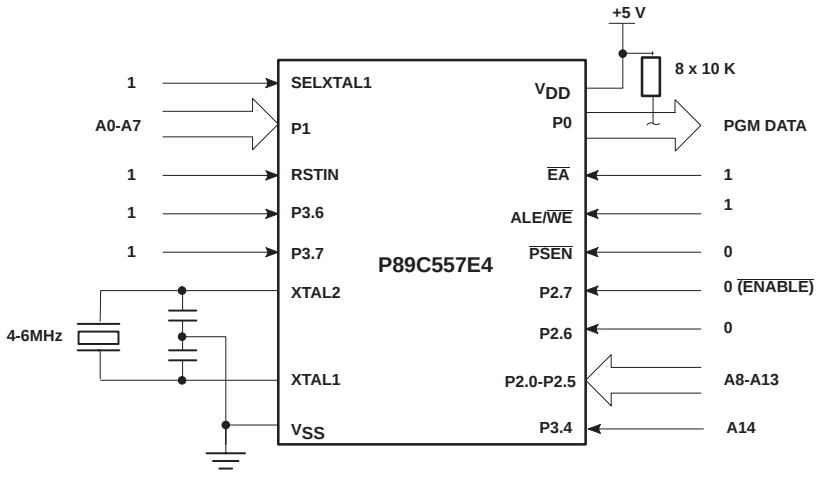
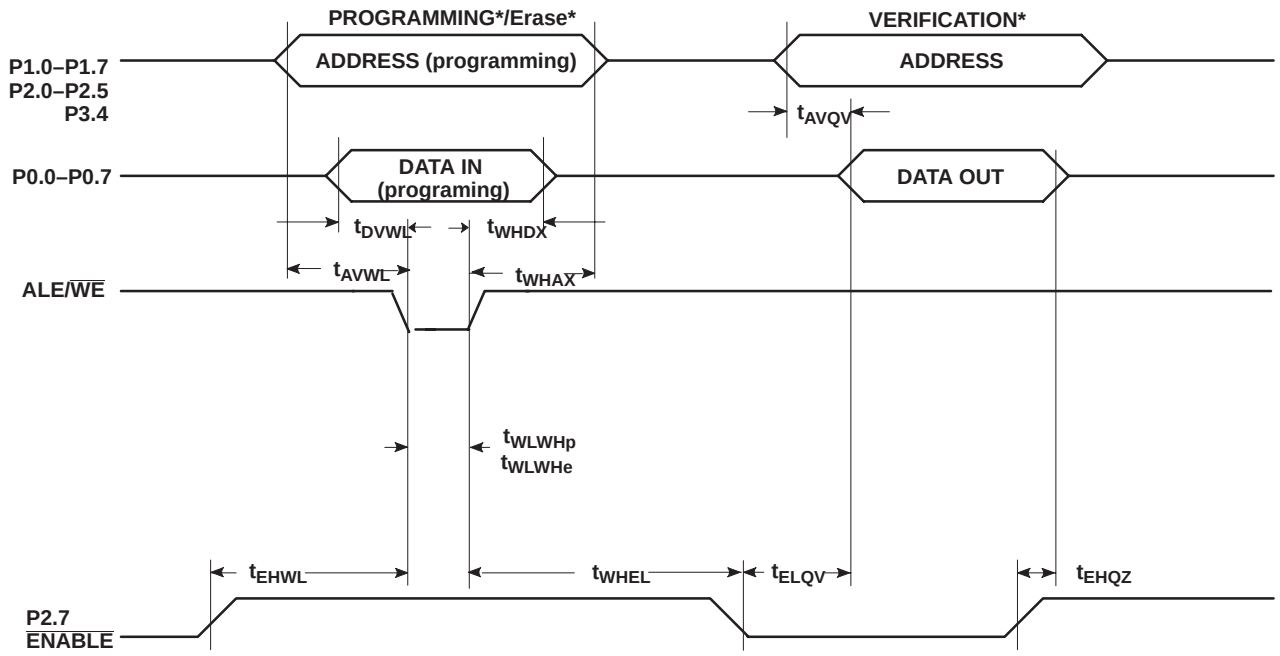


Figure 52. Program Verification

FEEPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = –40 °C to +85 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V (see Figure 53)

SYMBOL	PARAMETER	MIN	MAX	UNIT
$1/t_{CLK}$	System clock frequency (standard oscillator)	4	6	MHz
t_{AVWL}	Address setup to $\overline{WE}$ LOW	$48t_{CLK}$	–	
t_{WHAX}	Address hold after $\overline{WE}$ HIGH	$48t_{CLK}$	–	
t_{DVWL}	Data setup to $\overline{WE}$ LOW	$48t_{CLK}$	–	
t_{WHDX}	Data hold after $\overline{WE}$ HIGH	$48t_{CLK}$	–	
t_{EHWL}	P2.7 ($\overline{ENABLE}$) HIGH to $\overline{WE}$ LOW	$48t_{CLK}$	–	
t_{WHEL}	$\overline{WE}$ HIGH to P2.7 ($\overline{ENABLE}$) LOW	$48t_{CLK}$	–	
t_{WLWHp}	$\overline{WE}$ width (programming)	2.25	2.75	ms
t_{WLWHe}	$\overline{WE}$ width (erase)	4.5	5.5	ms
t_{AVQV}	Address to data valid	–	$48t_{CLK}$	
t_{ELQV}	P2.7 ($\overline{ENABLE}$) Low to data valid	–	$48t_{CLK}$	
t_{EHQZ}	Data float after P2.7 ($\overline{ENABLE}$) HIGH	0	$48t_{CLK}$	



* For ERASE conditions see Figure 50.
For PROGRAM conditions see Figure 51.
For VERIFY conditions see Figure 52.

Figure 53. FEEPROM Programming/Erase and Verification Waveforms

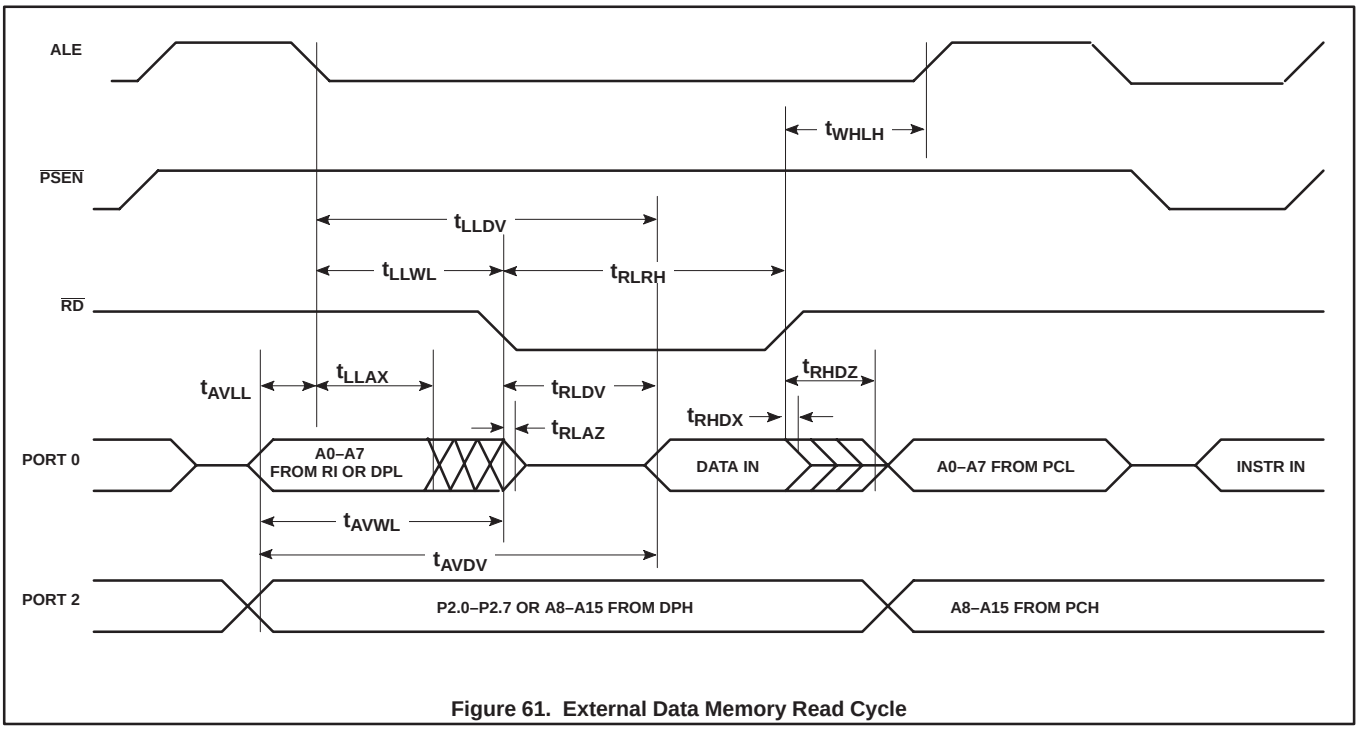


Figure 61. External Data Memory Read Cycle

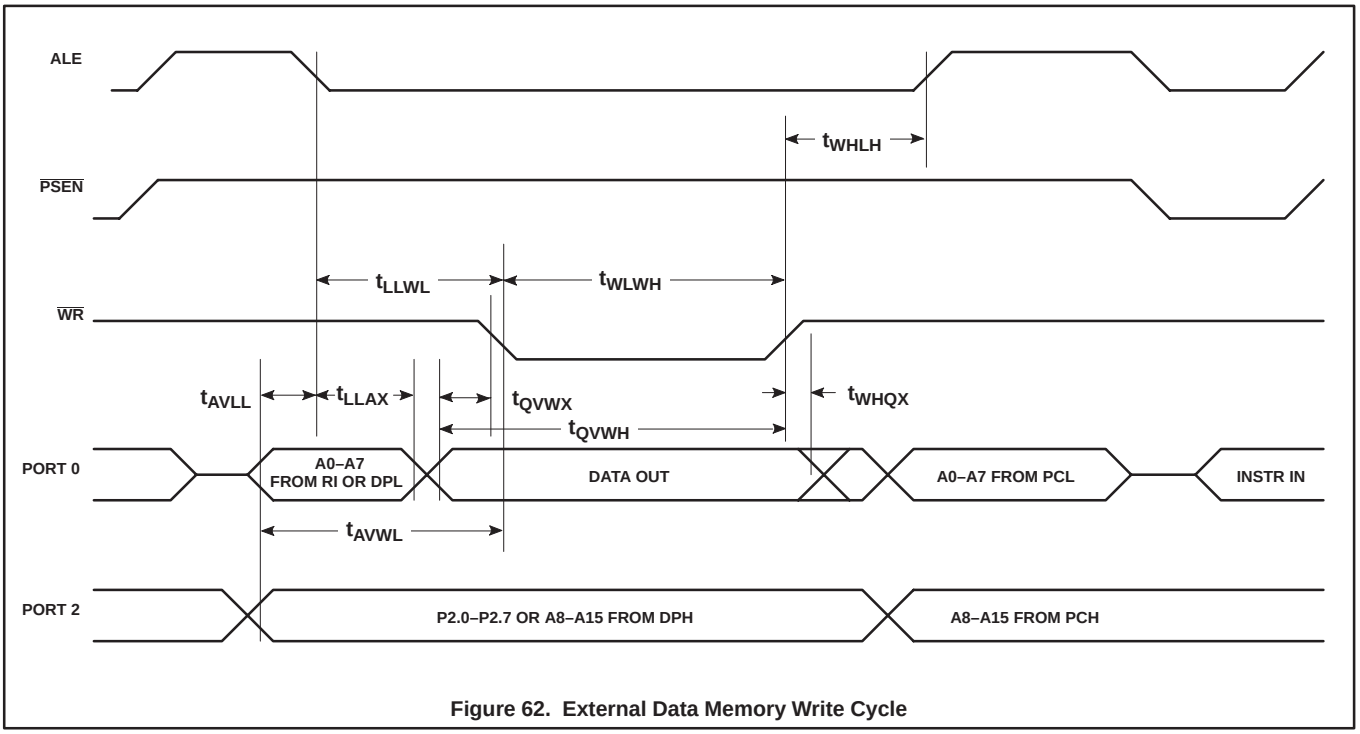


Figure 62. External Data Memory Write Cycle

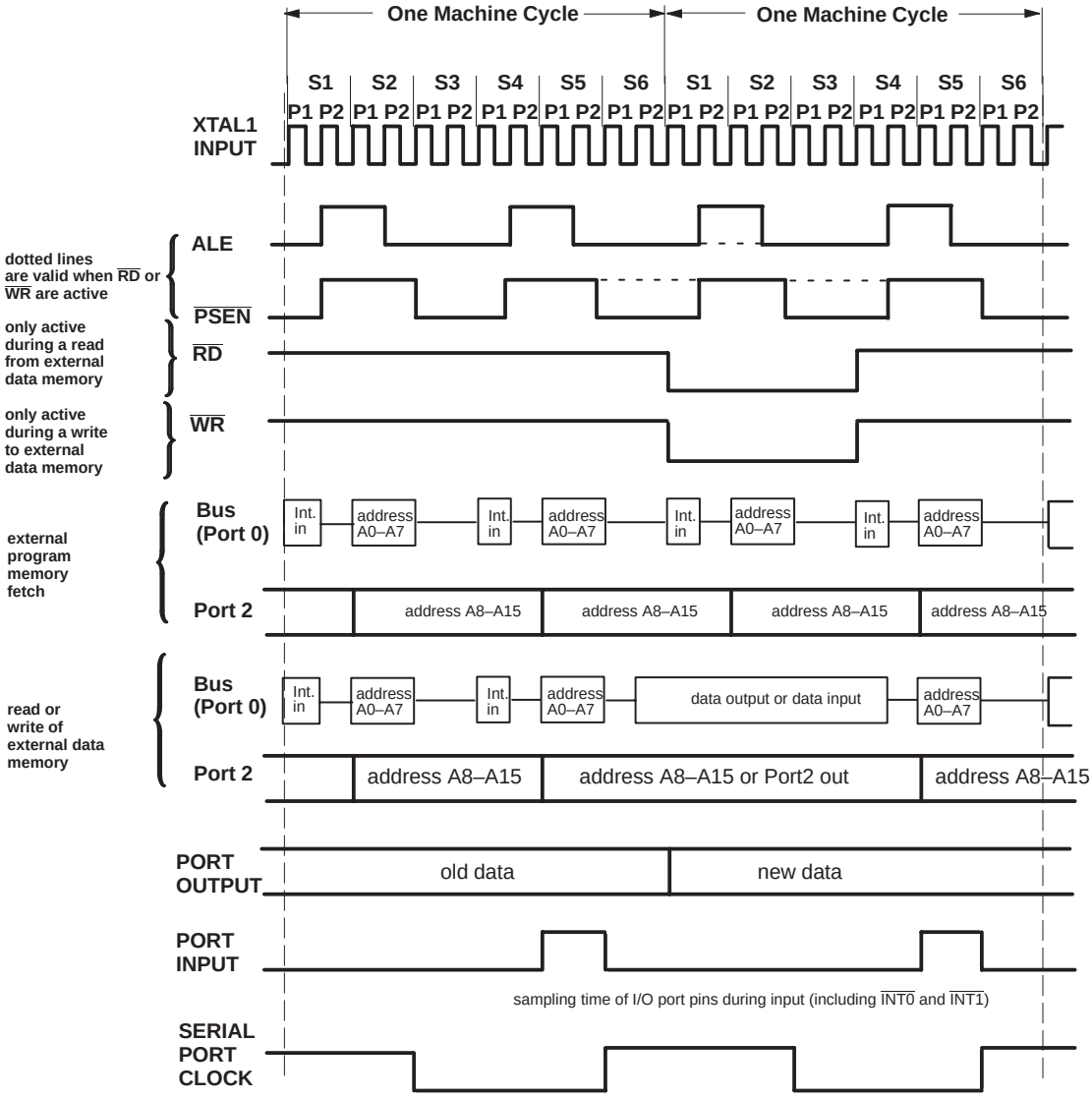


Figure 65. Instruction cycle timing

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.