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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6d5eym12ae

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST® data network, using the standardized MediaLB protocol (up to 150 Mbps). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Supports 16/32/64-bit DDR3 / DDR3L or LPDDR2 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Supports up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRAM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controllers.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply input voltage (LDO enabled)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.6	V
Core supply input voltage (LDO bypass)	VDD_ARM_IN VDD_ARM23_IN VDD_SOC_IN	-0.3	1.4	V
Core supply output voltage (LDO enabled)	VDD_ARM_CAP VDD_SOC_CAP VDD_PU_CAP NVCC_PLL_OUT	-0.3	1.4	V
VDD_HIGH_IN supply voltage	VDD_HIGH_IN	-0.3	3.7	V
DDR I/O supply voltage	NVCC_DRAM	-0.4	1.975 (See note 1)	V
GPIO I/O supply voltage	NVCC_CSI NVCC_EIM NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NAND NVCC_SD NVCC_JTAG	-0.5	3.7	V
HDMI, PCIe, and SATA PHY high (VPH) supply voltage	HDMI_VPH PCIE_VPH SATA_VPH	-0.3	2.85	V
HDMI, PCIe, and SATA PHY low (VP) supply voltage	HDMI_VP PCIE_VP SATA_VP	-0.3	1.4	V
LVDS, MLB, and MIPI I/O supply voltage (2.5V supply)	NVCC_LVDS_2P5 NVCC_MIPI	-0.3	2.85	V
PCIe PHY supply voltage	PCIE_VPTX	-0.3	1.4	V
RGMII I/O supply voltage	NVCC_RGMII	-0.5	2.725	V
SNVS IN supply voltage (Secure Non-Volatile Storage and Real Time Clock)	VDD_SNVS_IN	-0.3	3.4	V
USB I/O supply voltage	USB_H1_DN USB_H1_DP USB_OTG_DN USB_OTG_DP USB_OTG_CHD_B	-0.3	3.73	V
USB VBUS supply voltage	USB_H1_VBUS USB_OTG_VBUS	—	5.35	V
V_{in}/V_{out} input/output voltage range (non-DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.3 (See note 2)	V
V_{in}/V_{out} input/output voltage range (DDR pins)	V_{in}/V_{out}	-0.5	OVDD+0.4 (See notes1&2)	V
ESD immunity (HBM)	V_{esd_HBM}	—	2000	V
ESD immunity (CDM)	V_{esd_CDM}	—	500	V
Storage temperature range	$T_{storage}$	-40	150	°C

1 The absolute maximum voltage includes an allowance for 400 mV of overshoot on the IO pins. Per JEDEC standards, the allowed signal overshoot must be derated if NVCC_DRAM exceeds 1.575V.

2 OVDD is the I/O supply voltage.

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 20. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 μA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA must be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	100 kΩ	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

The term ‘OVDD’ in this section refers to the associated supply rail of an input or output.

4.8.1 GPIO Output Buffer Impedance

Table 34 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 34. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	260 130 90 60 50 40 33	Ω

Table 35 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	150 75 50 37 30 25 20	Ω

4.11.3 Samsung Toggle Mode AC Timing

4.11.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See Section 4.11.1, “Asynchronous Mode AC Timing (ONFI 1.0 Compatible)” for details.

4.11.3.2 Read and Write Timing

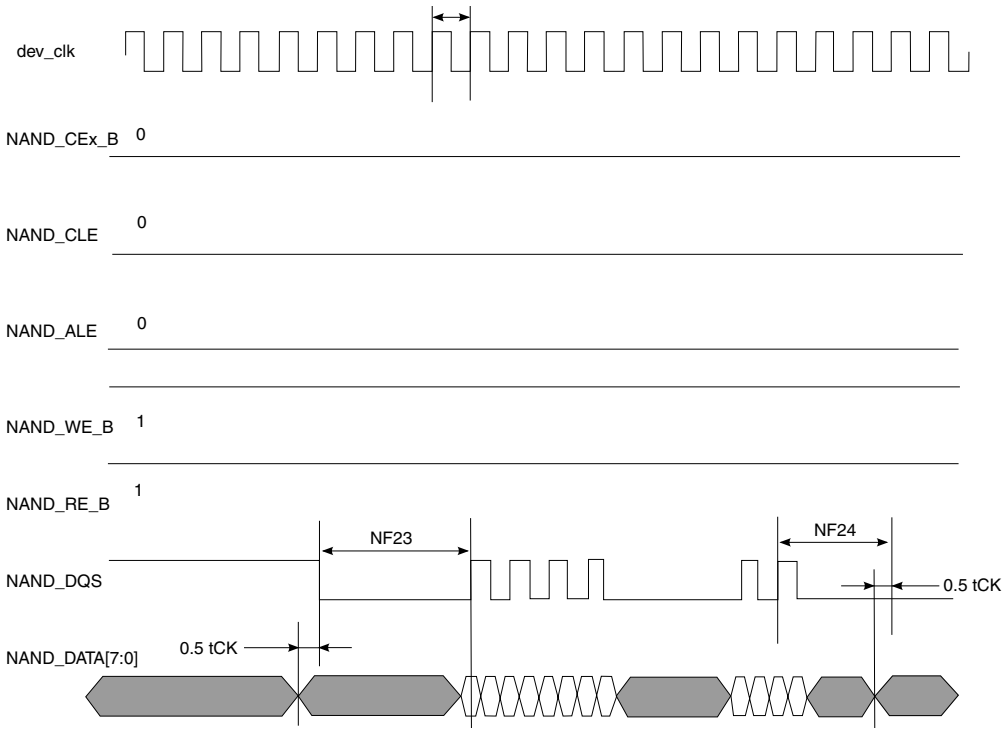

Figure 33. Samsung Toggle Mode Data Write Timing

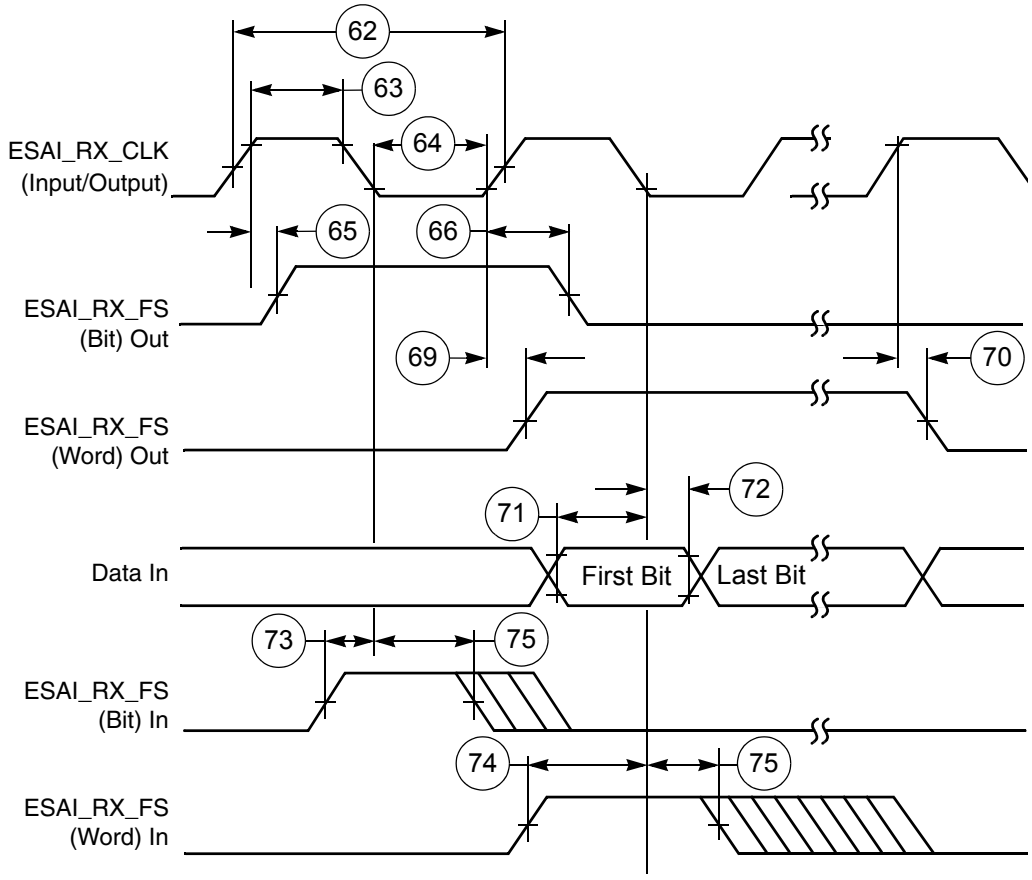

Figure 38. ESAI Receiver Timing

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 µs.

4.12.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

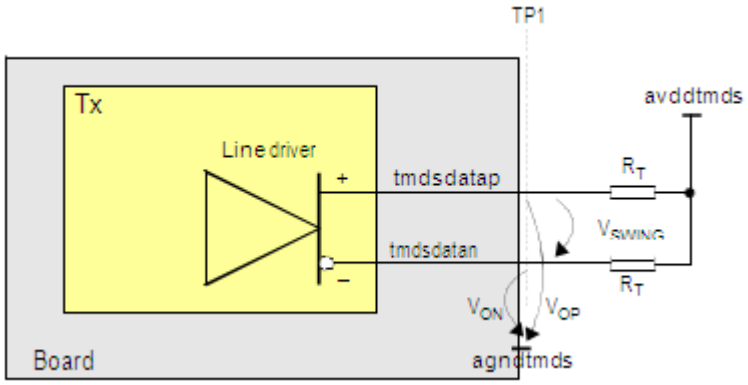

Figure 50. Driver Measuring Conditions

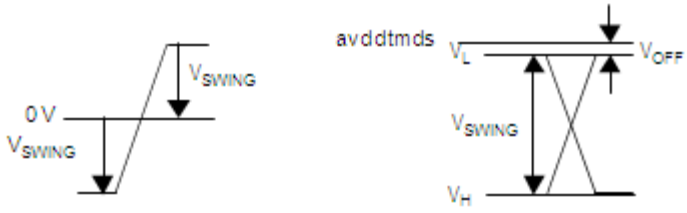

Figure 51. Driver Definitions

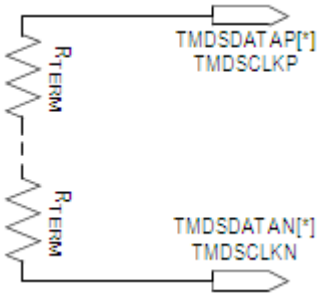

Figure 52. Source Termination

Table 59. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	—	3.15	3.3	3.45	V

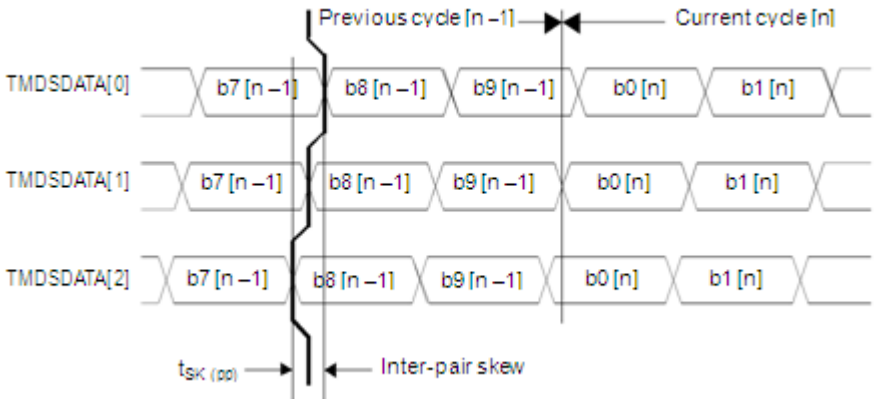

Figure 56. Inter-Pair Skew Definition

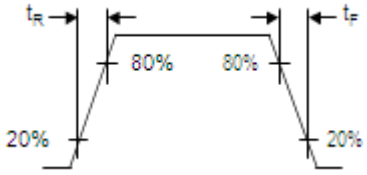

Figure 57. TMDS Output Signals Rise and Fall Time Definition

Table 60. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}$	TMDSCLK period	RL = 50 Ω See Figure 53.	2.94	—	40	ns
t_{CDC}	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 53.	40	50	60	%
t_{CPH}	TMDSCLK high time	RL = 50 Ω See Figure 53.	4	5	6	UI
t_{CPL}	TMDSCLK low time	RL = 50 Ω See Figure 53.	4	5	6	UI
—	TMDSCLK jitter[1]	RL = 50 Ω	—	—	0.25	UI
$t_{SK(p)}$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 55.	—	—	0.15	UI
$t_{SK(pp)}$	Inter-pair skew	RL = 50 Ω See Figure 56.	—	—	1	UI
t_R	Differential output signal rise time	20–80% RL = 50 Ω See Figure 57.	75	—	0.4 UI	ps

Table 64. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD						Comment[1,2]
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)					
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb[3]	16-bit YCrCb	20-bit YCrCb	
IPUx_DIx_PIN04	—						Additional frame/row synchronous signals with programmable timing
IPUx_DIx_PIN05	—						
IPUx_DIx_PIN06	—						
IPUx_DIx_PIN07	—						
IPUx_DIx_PIN08	—						
IPUx_DIx_D0_CS	—						—
IPUx_DIx_D1_CS	—						Alternate mode of PWM output for contrast or brightness control
IPUx_DIx_PIN11	—						—
IPUx_DIx_PIN12	—						—
IPUx_DIx_PIN13	—						Register select signal
IPUx_DIx_PIN14	—						Optional RS2
IPUx_DIx_PIN15	DRDY/DV						Data validation/blank, data enable
IPUx_DIx_PIN16	—						Additional data synchronous signals with programmable features/timing
IPUx_DIx_PIN17	Q						

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 Restrictions for ports IPUx_DISPx_DAT00 through IPUx_DISPx_DAT23 are as follows:
- A maximum of three continuous groups of bits can be independently mapped to the external bus. Groups must not overlap.
- The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.

3 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 64 provides information for both the DISP0 and DISP1 ports. However, DISP1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all configurations. See the IOMUXC table for details.

4.12.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.12.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

Figure 65 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 66 lists the synchronous display interface timing characteristics.

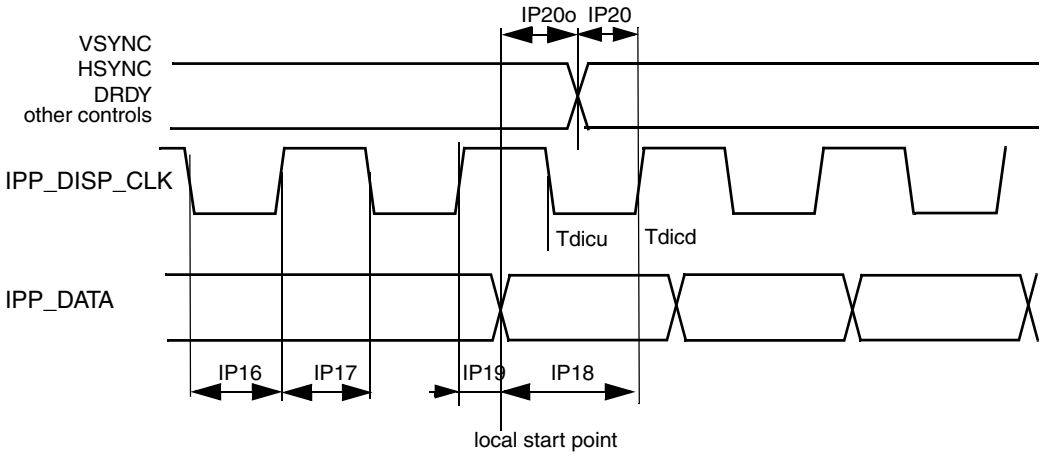

Figure 65. Synchronous Display Interface Timing Diagram—Access Level

Table 66. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd[2]-Tdicu[3]	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$\mathrm{Tdicd} = \frac{1}{2}\left(\mathrm{T_{diclk}} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP\_CLK\_DOWN}}{\mathrm{DI\_CLK\_PERIOD}}\right]\right)$$

[3] Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$\mathrm{Tdicu} = \frac{1}{2}\left(\mathrm{T_{diclk}} \times \mathrm{ceil}\left[\frac{2 \times \mathrm{DISP\_CLK\_UP}}{\mathrm{DI\_CLK\_PERIOD}}\right]\right)$$

Table 68. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage	—	—	—	550	mV
V_{IH}	Input high voltage	—	920	—	—	mV
V_{HYST}	Input hysteresis	—	25	—	—	mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold	—	200	—	450	mV

4.12.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 66 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signalling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

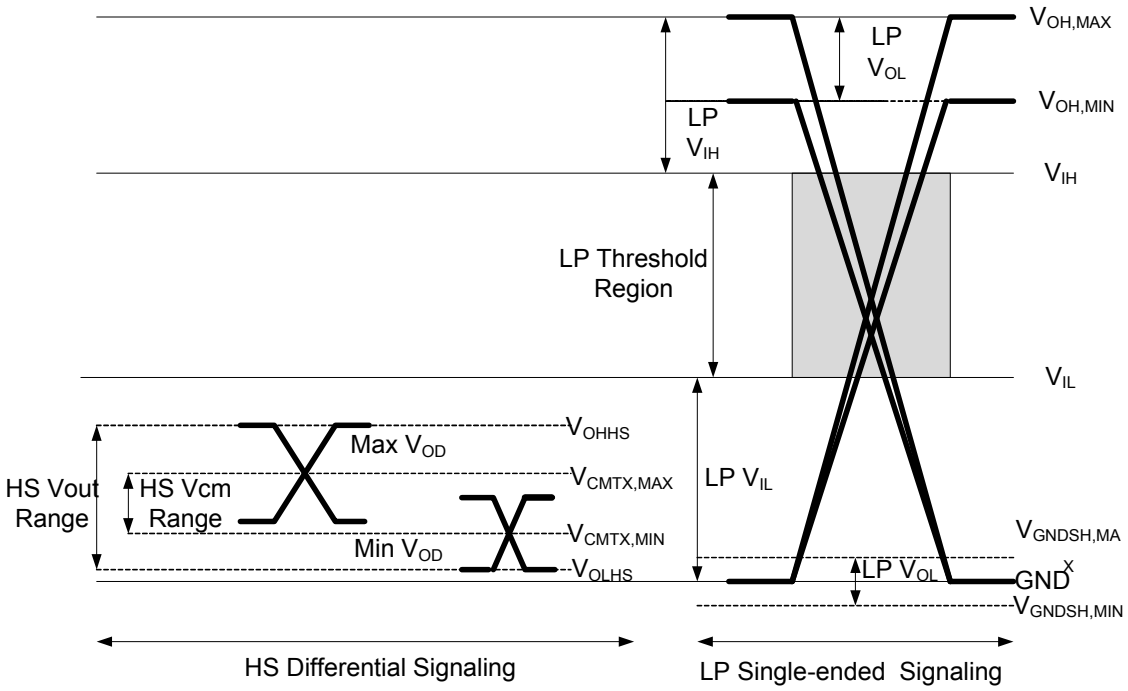

Figure 66. D-PHY Signaling Levels

Table 69. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}	—	30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—	—	—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—	—	ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF

4.12.17.1.1 SATA PHY Transmitter Characteristics

Table 77 provides specifications for SATA PHY transmitter characteristics.

Table 77. SATA PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	–0.5	—	0.5	dB

4.12.17.1.2 SATA PHY Receiver Characteristics

Table 78 provides specifications for SATA PHY receiver characteristics.

Table 78. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN\_RX\_EYE\_HEIGHT}$	175	—	—	mV
Tolerance	PPM	–400	—	400	ppm

4.12.17.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.12.18 SCAN JTAG Controller (SJC) Timing Parameters

Figure 84 depicts the SJC test clock input timing. Figure 85 depicts the SJC boundary scan timing. Figure 86 depicts the SJC test access port. Figure 87 depicts the JTAG_TRST_B timing. Signal parameters are listed in Table 79.

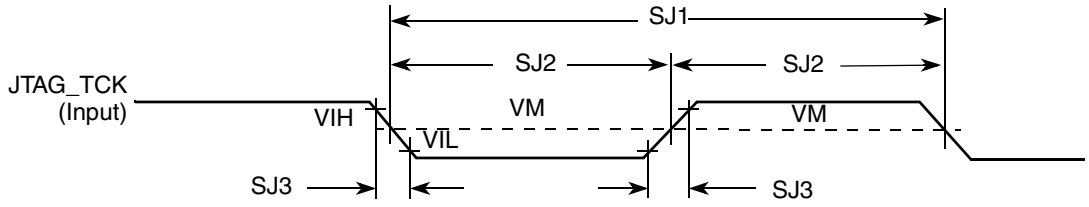

Figure 84. Test Clock Input Timing Diagram

4.12.23 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only

Table 94. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Pads During Boot	Comment
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD,SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D4, NANDF_D5, NANDF_D6, NANDF_D7, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6.2 21 x 21 mm Package Information

6.2.1 Case FCPBGA, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

6.2.1.1 21 x 21 mm Non-Lidded (Bare Die) Package

Figure 101 and Figure 101 show the top, bottom, and side views of the 21 × 21 mm bare die package.

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	PU (100K)
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO12	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO13	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO14	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO15	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN	—	—	TCU_TEST_MODE	Input	PD (100K)
USB_H1_DN	F10	VDD_USB_CAP	—	—	USB_H1_DN	—	—
USB_H1_DP	E10	VDD_USB_CAP	—	—	USB_H1_DP	—	—
USB_OTG_CHD_B	B8	VDD_USB_CAP	—	—	USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDD_USB_CAP	—	—	USB_OTG_DN	—	—
USB_OTG_DP	A6	VDD_USB_CAP	—	—	USB_OTG_DP	—	—
XTALI	A7	NVCC_PLL	—	—	XTALI	—	—
XTALO	B7	NVCC_PLL	—	—	XTALO	—	—

[1] The state immediately after reset and before ROM firmware or software has executed.

6.2.5 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 98 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	SATA_TXP	GND	SATA_RXM	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	SATA_TXM	SD3_CMD	SATA_RXP	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	SATA_REXT	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23
E	CSI_D2M	CSI_D2P	CSI_D0P	CSI_D0M	GND	GND	GND	NVCC_PLL_OUT	USB_OTG_VBUS	USB_H1_DP	TAMPER	TEST_MODE	SD3_DAT6	SD3_DAT0	NANDF_WP_B	SD4_CLK	NANDF_D6	SD4_DAT4	SD1_DAT2	SD2_DAT1	RGMII_TD2	EIM_EB2	EIM_D22	EIM_D26	EIM_D27
F	CSI_D3P	CSI_D3M	CSI_CLK0P	CSI_CLK0M	GND	GND	GND	GND	VDDUSB_CAP	USB_H1_DN	PMIC_STBY_REQ	BOOT_MODE1	SD3_DAT7	SD3_DAT1	NANDF_CS0	NANDF_D2	SD4_DAT2	SD1_DAT3	SD2_CMD	RGMII_TD1	EIM_D17	EIM_D24	EIM_EB3	EIM_A22	EIM_A24
G	DSI_D0P	DSI_D0M	GND	DSI_REXT	JTAG_TDI	JTAG_TDO	PCIE_VPH	PCIE_VPTX	VDD_SNVS_CAP	GND	VDD_SNVS_IN	SATA_VPH	SATA_VP	NVCC_SD3	NVCC_NANDF	NVCC_SD1	NVCC_SD2	NVCC_RGMII	GND	EIM_D20	EIM_D19	EIM_D25	EIM_D28	EIM_A17	EIM_A19

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	07/2015	• Added footnote to Table 1, “Example Orderable Part Numbers,” on page 3: If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz. • Section 1.2, “Features” changed Five UARTs, from *up to 4.0 Mbps*, to *up to 5.0 Mbps.* • Table 6, “Operating Ranges,” on page 23: Row: VDD_HIGH internal regulator, changed minimum parameter value from 2.8 to 2.7V. • Table 6, “Operating Ranges,” on page 23: Removed footnote: *VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM-VDDSOC/PU<50mV.* This was a duplicate footnote, renumbered footnotes accordingly. • Table 6, “Operating Ranges,” on page 23: Changed value: *Standby/DSM Mode, VDD_SOC_IN, minimum voltage, from 0.9V to 1.05V.* • Consumer: Added Table 18, “MLB PLL Electrical Parameters,” on page 37 which had erroneously been removed from previous revisions. • Table 8, “Maximum Supply Currents,” on page 27, Differentiated VDD_ARM_IN, VDD_ARM23_IN, and VDD_SOC_IN by frequency and by Power Virus/CoreMark maximum current. • Table 21, “XTALI and RTC_XTALI DC Parameters,” on page 39, Added rows: *Input capacitance*; *Startup current*; and *DC input current* and their values. • Table 41, “EIM Bus Timing Parameters,” on page 55, Changed WE4–WE17 minimum and maximum parameter values from, *0.5 t (k+1)/2-1.25*, to *0.5 x t x (k+1)-1.25.* • Table 42, “EIM Asynchronous Timing Parameters Relative to Chip Select¹,” on page 62 Added to end of formulas in the minimum, typical, and maximum parameter values for WE31–WE42 and WE45–WE46, *×t*. For example from *3-CSN*, to *3-CSN×t*. Also added maximum value to MAXDTI of 10. • Table 58, “DDR3/DDR3L Write Cycle,” on page 90, Changed minimum parameter value of DDR17 from 240 to 125; and of DDR18 from 240 to 150. • Figure 29, “LPDDR2 Command and Address Timing Diagram,” on page 91, LP2 signal cycle reduced. • Table 62, “LPDDR2 Write Cycle,” on page 93, Changed LP21 minimum and maximum parameter value from -0.25/+0.25 to 0.8/1.2. • Figure 35, "ECSPI Master Mode Timing Diagram," on page 74, Added footnote: *Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 36, "ECSPI Slave Mode Timing Diagram," on page 75, Added footnote: *Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 59, "Gated Clock Mode Timing Diagram," on page 96, Corrected IPU2_CSIx_HSYNC trace drawing. • Section 4.12.23, “USB PHY Parameters” Specified *Battery Charging Specification* applies to portable devices only. *(Revision History table continues on next page.)*