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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5eym10ae

- High-end mobile Internet devices (MID)
- High-end PDAs
- High-end portable media players (PMP) with HD video capability
- Gaming consoles
- Portable navigation devices (PND)

The i.MX 6Dual/6Quad processors offers numerous advanced features, such as:

- Applications processors—The processors enhance the capabilities of high-tier portable applications by fulfilling the ever increasing MIPS needs of operating systems and games. The Dynamic Voltage and Frequency Scaling (DVFS) provides significant power reduction, allowing the device to run at lower voltage and frequency with sufficient MIPS for tasks such as audio decode.
- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon® MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- Powerful graphics acceleration—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MTri/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, SATA-II, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated High Speed Inter-Chip (HS-IC) USB PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while the other four support 4-wire. This is due to the SoC IOMUX limitation, because all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI)
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
  - Two Controller Area Network (FlexCAN), 1 Mbps each
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)
  - MLB (MediaLB) provides interface to MOST Networks (150 Mbps) with the option of DTCP cipher accelerator

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

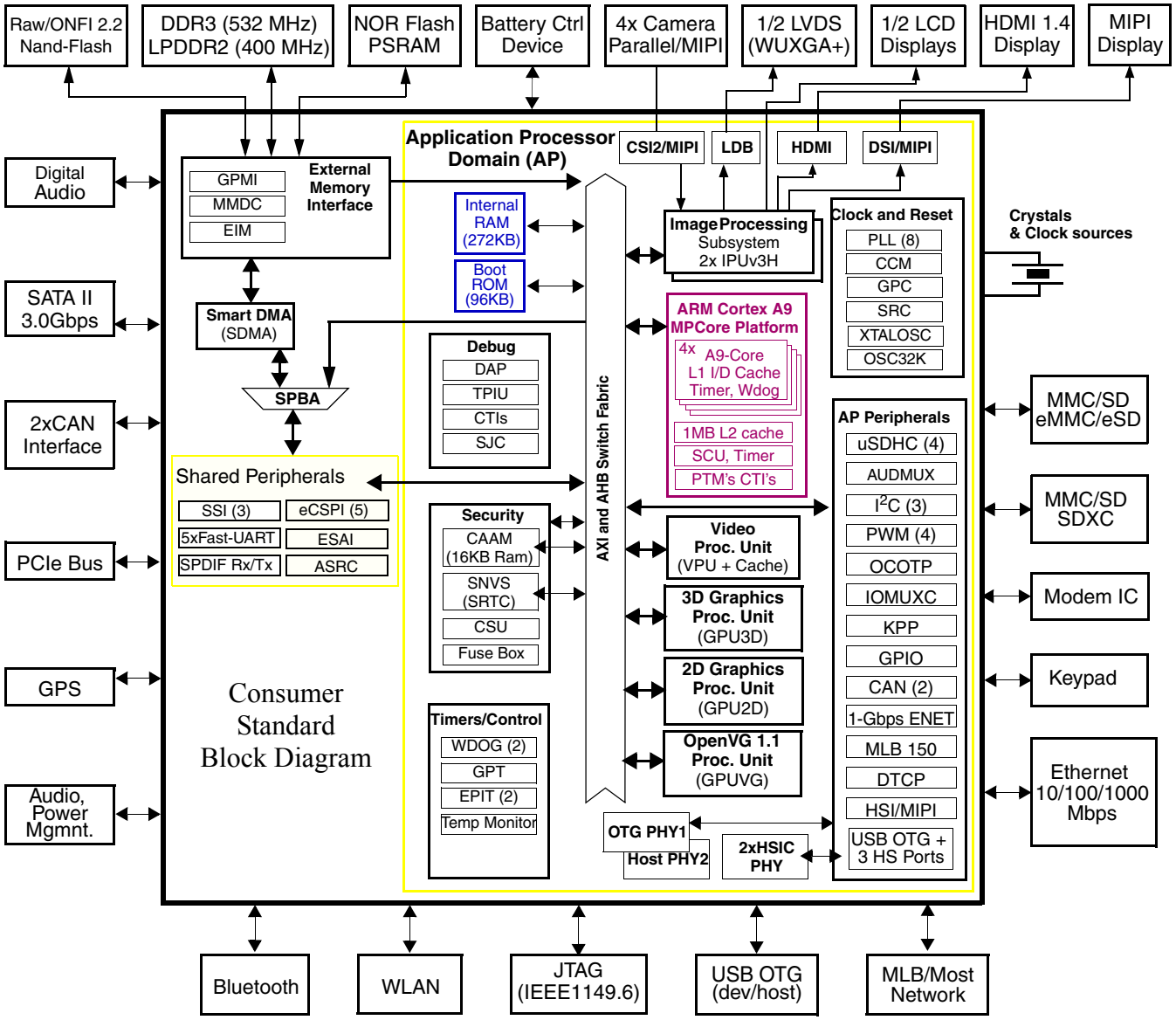


Figure 2. i.MX 6Dual/6Quad Consumer Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ROM 96 KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface	—	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual (IMX6DQRM). Special signal consideration information is contained in the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in the section, "Unused analog interfaces," of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4.1.3 Operating Ranges

Table 6 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 6. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.4[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.275 V minimum for operation up to 1200 MHz. **Only supported in LDO enabled mode.**
		1.35[6]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[7]) of 1.225 V minimum for operation up to 996 MHz.
		1.275[6]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[7]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[6]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[7]) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[8]	1.350[6]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[6,9]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed[10]	VDD_ARM_IN VDD_ARM23_IN[3]	1.225	—	1.3	V	LDO bypassed for operation up to 996 MHz.
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN[8]	1.225	—	1.3	V	264 MHz < VPU ≤ 352 MHz
		1.15	—	1.3	V	VPU ≤ 264 MHz
Standby/DSM mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, "Stop Mode Current and Power Consumption," on page 28.
	VDD_SOC_IN	0.9	—	1.3	V	
VDD_HIGH internal regulator	VDD_HIGH_IN[11]	2.7	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[11]	2.8	—	3.3	V	Should be supplied from the same supply as VDD_HIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
Supply for RGMII I/O power group[12]	NVCC_RGMII	1.15	—	2.625	V	• 1.15 V – 1.30 V in HSIC 1.2 V mode • 1.43 V – 1.58 V in RGMII 1.5 V mode • 1.70 V – 1.90 V in RGMII 1.8 V mode • 2.25 V – 2.625 V in RGMII 2.5 V mode

Table 9. Stop Mode Current and Power Consumption (continued)

Mode	Test Conditions	Supply	Typical[1]	Unit
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	22	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.4 V)	7.5	mA
		VDD_SOC_IN (1.4 V)	13.5	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	13	mA
		VDD_HIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • Crystal oscillator and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SOC_IN (0.9 V)	2	mA
		VDD_HIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDD_HIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- The SRC_POR_B signal controls the processor POR and must be immediately asserted at power-up and remain asserted until the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP supplies are stable. VDD_ARM_IN and VDD_SOC_IN may be applied in either order with no restrictions.

  Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

  NOTE

  USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

There are no special restrictions for i.MX 6Dual/6Quad SoC.

4.2.3 Power Supplies Usage

- All I/O pins must not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see the “Power Group” column of Table 96, “21 x 21 mm Functional Contact Assignments”.
- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REXT, SATA_PHY_RX_N, SATA_PHY_RX_P, and SATA_PHY_TX_N) can remain unconnected. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.

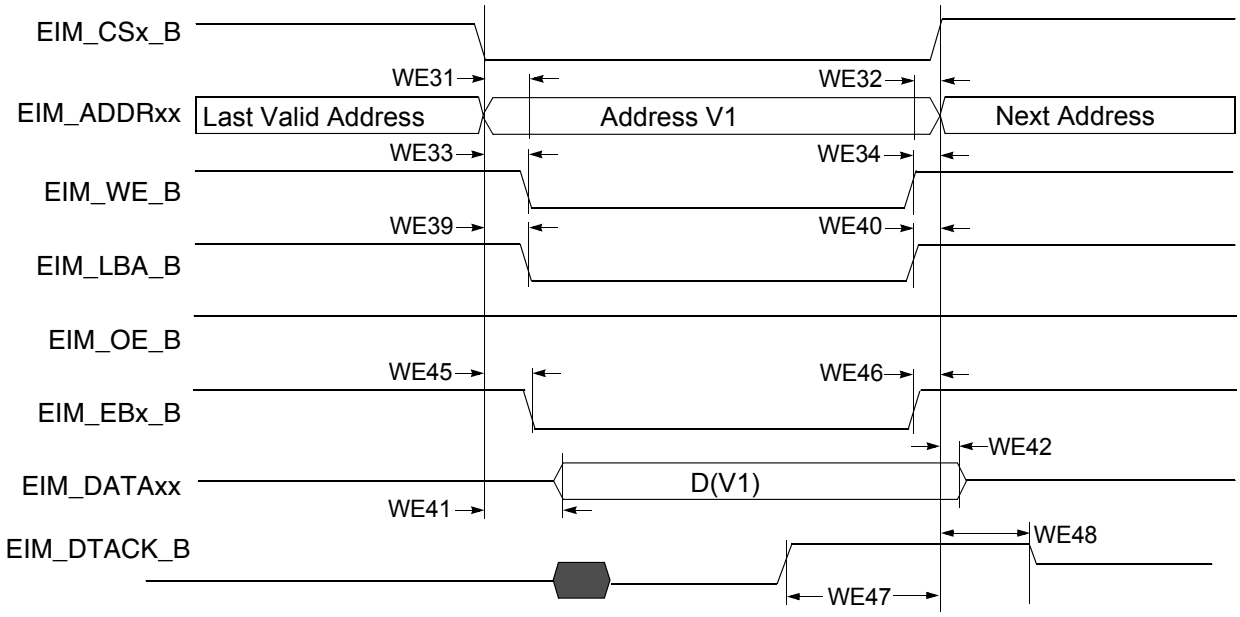


Figure 23. DTACK Mode Write Access (DAP=0)

Table 42. EIM Asynchronous Timing Parameters Relative to Chip Select[1, 2]

Ref No.	Parameter	Determination by Synchronous measured parameters	Min	Max	Unit
WE31	EIM_CSx_B valid to Address Valid	WE4-WE6-CSA×t	-3.5-CSA×t	3.5-CSA×t	ns
WE32	Address Invalid to EIM_CSx_B Invalid	WE7-WE5-CSN×t	-3.5-CSN×t	3.5-CSN×t	ns
WE32A (muxed A/D)	EIM_CSx_B valid to Address Invalid	t+WE4-WE7+ (ADVN+ADVA+1-CSA)×t	t - 3.5+(ADVN+ADVA+1-CSA)×t	t + 3.5+(ADVN+ADVA+1-CSA)×t	ns
WE33	EIM_CSx_B Valid to EIM_WE_B Valid	WE8-WE6+(WEA-WCSA)×t	-3.5+(WEA-WCSA)×t	3.5+(WEA-WCSA)×t	ns
WE34	EIM_WE_B Invalid to EIM_CSx_B Invalid	WE7-WE9+(WEN-WCSN)×t	-3.5+(WEN-WCSN)×t	3.5+(WEN-WCSN)×t	ns
WE35	EIM_CSx_B Valid to EIM_OE_B Valid	WE10- WE6+(OEA-RCSA)×t	-3.5+(OEA-RCSA)×t	3.5+(OEA-RCSA)×t	ns
WE35A (muxed A/D)	EIM_CSx_B Valid to EIM_OE_B Valid	WE10-WE6+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	-3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	3.5+(OEA+RADVN+RADVA+ADH+1-RCSA)×t	ns
WE36	EIM_OE_B Invalid to EIM_CSx_B Invalid	WE7-WE11+(OEN-RCSN)×t	-3.5+(OEN-RCSN)×t	3.5+(OEN-RCSN)×t	ns
WE37	EIM_CSx_B Valid to EIM_EBx_B Valid (Read access)	WE12-WE6+(RBEA-RCSA)× t	-3.5+(RBEA- RCSA)×t	3.5+(RBEA - RCSA)×t	ns
WE38	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Read access)	WE7-WE13+(RBEN-RCSN)×t	-3.5+ (RBEN-RCSN)×t	3.5+(RBEN-RCSN)×t	ns
WE39	EIM_CSx_B Valid to EIM_LBA_B Valid	WE14-WE6+(ADVA-CSA)×t	-3.5+ (ADVA-CSA)×t	3.5+(ADVA-CSA)×t	ns

[2] In this table:
- t means clock period from axi_clk frequency.
- CSA means register setting for WCSA when in write operations or RCSA when in read operations.
- CSN means register setting for WCSN when in write operations or RCSN when in read operations.
- ADVN means register setting for WADVN when in write operations or RADVN when in read operations.
- ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

4.10 Multi-Mode DDR Controller (MMDC)

The Multi-mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.10.1 MMDC Compatibility with JEDEC-Compliant SDRAMs

The i.MX 6Dual/6Quad MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

4.10.2 MMDC Supported DDR3/DDR3L/LPDDR2 Configurations

The table below shows the supported DDR3/DDR3L/LPDDR2 configurations:

Table 43. i.MX 6Dual/6Quad Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2	DDR3	DDR3L
Clock frequency	400 MHz	532 MHz	532 MHz
Bus width	32-bit per channel	16/32/64-bit	16/32/64-bit
Channel	Dual	Single	Single
Chip selects	2 per channel	2	2

4.11 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.11.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 29 shows the write and read timing of Source Synchronous mode.

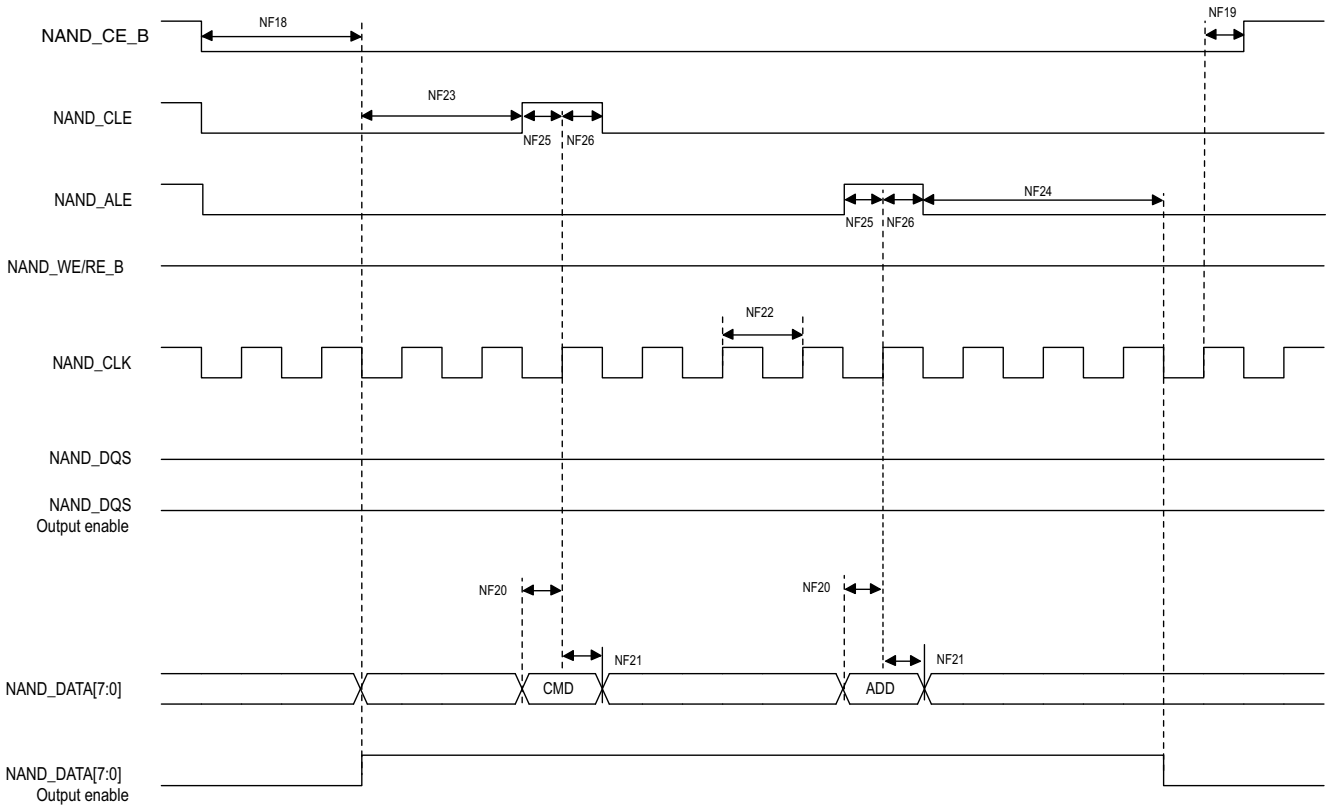
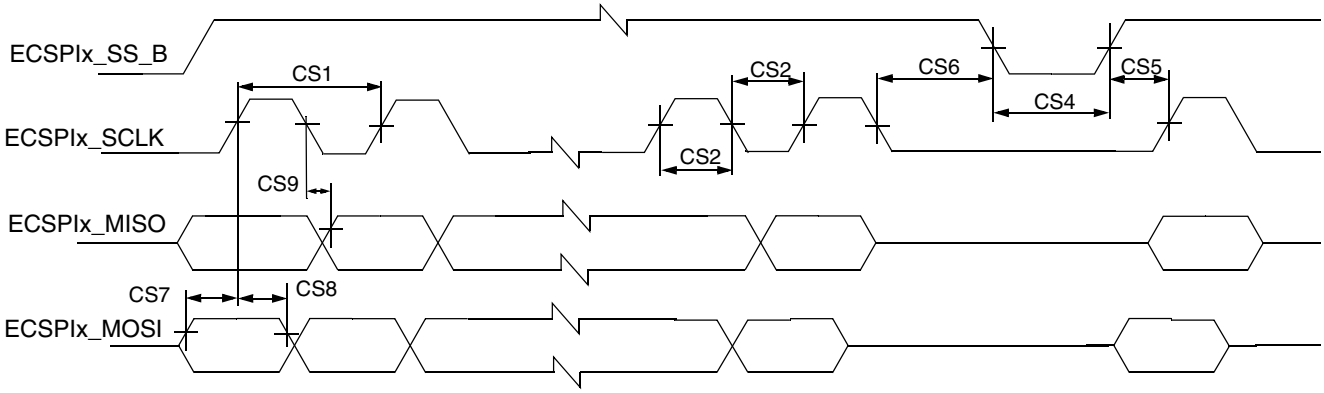


Figure 29. Source Synchronous Mode Command and Address Timing Diagram

4.12.2.2 ECSPI Slave Mode Timing

Figure 36 depicts the timing of ECSPI in slave mode and Table 48 lists the ECSPI slave mode timing characteristics.



Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Figure 36. ECSPI Slave Mode Timing Diagram

Table 48. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 55 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 26 20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx_SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF) • Slow group[1] • Fast group[2]	t_{PDmiso}	4	 25 17	ns

[1] ECSPI slow includes:
ECSPI1/DISP0_DAT22, ECSPI1/KEY_COL1, ECSPI1/CSI0_DAT6, ECSPI2/EIM_OE, ECSPI2/DISP0_DAT17, ECSPI2/CSI0_DAT10, ECSPI3/DISP0_DAT2

[2] ECSPI fast includes:
ECSPI1/EIM_D17, ECSPI4/EIM_D22, ECSPI5/SD2_DAT0, ECSPI5/SD1_DAT0

2 The MSB bits are duplicated on LSB bits implementing color extension.
3 The two MSB bits are duplicated on LSB bits implementing color extension.
4 YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).
5 RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.
6 YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.
7 YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).
8 YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.12.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.12.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is IPU2_CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering IPU2_CSIx_VSYNC and IPU2_CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the IPU2_CSIx_DATA_EN bus. On BT.1120 two components per cycle are received over the IPU2_CSIx_DATA_EN bus.

4.12.10.2.2 Gated Clock Mode

The IPU2_CSIx_VSYNC, IPU2_CSIx_HSYNC, and IPU2_CSIx_PIX_CLK signals are used in this mode. See Figure 59.

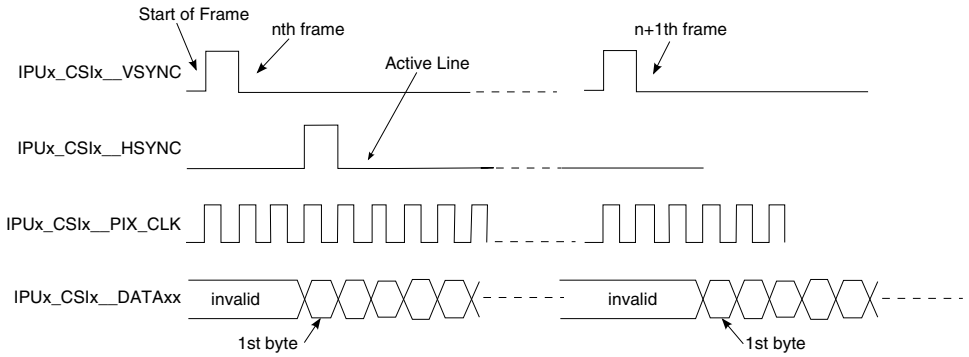


Figure 59. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on IPU2_CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then IPU2_CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as IPU2_CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. IPU2_CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI

Table 65. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}, & \text{for integer } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.
DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency
Display interface clock period average value.

$$\overline{T}dicp = T_{diclk} \times \frac{DISP\_CLK\_PERIOD}{DI\_CLK\_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximum accuracy of UP/DOWN edge of controls is:

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.62ns$$

The maximum accuracy of UP/DOWN edge of IPP_DISP_DATA is:

$$Accuracy = T_{diclk} \pm 0.62ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

4.12.21.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.12.21.2.1 UART Transmitter

Figure 94 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 87 lists the UART RS-232 serial mode transmit timing characteristics.

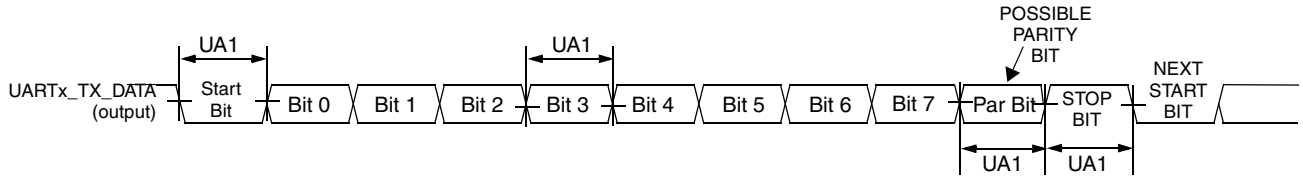


Figure 94. UART RS-232 Serial Mode Transmit Timing Diagram

Table 87. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$ [1] – T_{ref_clk} [2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.12.21.2.2 UART Receiver

Figure 95 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 88 lists serial mode receive timing characteristics.

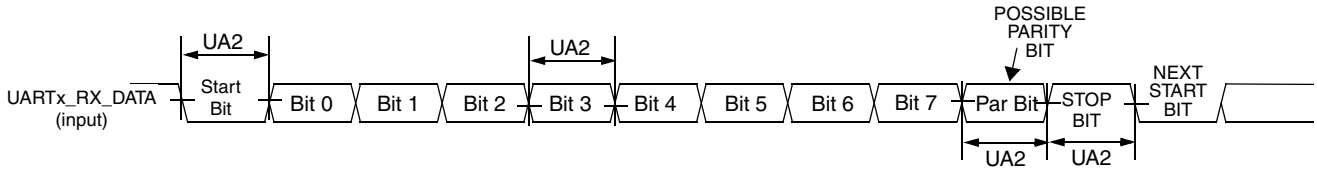


Figure 95. UART RS-232 Serial Mode Receive Timing Diagram

Table 88. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$ [2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 93 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter of the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

Table 93. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name
Boot Mode Selection		
BOOT_MODE1	Input	Boot Mode Selection
BOOT_MODE0	Input	Boot Mode Selection
Boot Options[1]		
EIM_DA0	Input	BOOT_CFG1[0]
EIM_DA1	Input	BOOT_CFG1[1]
EIM_DA2	Input	BOOT_CFG1[2]
EIM_DA3	Input	BOOT_CFG1[3]
EIM_DA4	Input	BOOT_CFG1[4]
EIM_DA5	Input	BOOT_CFG1[5]
EIM_DA6	Input	BOOT_CFG1[6]
EIM_DA7	Input	BOOT_CFG1[7]
EIM_DA8	Input	BOOT_CFG2[0]
EIM_DA9	Input	BOOT_CFG2[1]
EIM_DA10	Input	BOOT_CFG2[2]
EIM_DA11	Input	BOOT_CFG2[3]
EIM_DA12	Input	BOOT_CFG2[4]
EIM_DA13	Input	BOOT_CFG2[5]
EIM_DA14	Input	BOOT_CFG2[6]
EIM_DA15	Input	BOOT_CFG2[7]
EIM_A16	Input	BOOT_CFG3[0]
EIM_A17	Input	BOOT_CFG3[1]

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

6.2.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 95 shows the device connection list for ground, power, sense, and reference contact signals.

Table 95. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	—
DRAM_VREF	AC2	—
DSI_REXT	G4	—
FA_ANA	A5	—
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	—
GPANAIO	C8	Analog output for NXP use only. This output must remain unconnected
HDMI_DDCCEC	K2	Analog ground reference for the Hot Plug detect signal
HDMI_REF	J1	—
HDMI_VP	L7	—
HDMI_VPH	M7	—
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.

Table 96. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function (Signal Name)	Input/Output	Value[2]
CSI_D1P	D2	NVCC_MIPI	—	—	CSI_DATA1_P	—	—
CSI_D2M	E1	NVCC_MIPI	—	—	CSI_DATA2_N	—	—
CSI_D2P	E2	NVCC_MIPI	—	—	CSI_DATA2_P	—	—
CSI_D3M	F2	NVCC_MIPI	—	—	CSI_DATA3_N	—	—
CSI_D3P	F1	NVCC_MIPI	—	—	CSI_DATA3_P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	GPIO5_IO28	Input	PU (100K)
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	GPIO5_IO29	Input	PU (100K)
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	GPIO5_IO30	Input	PU (100K)
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	GPIO5_IO31	Input	PU (100K)
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	GPIO6_IO00	Input	PU (100K)
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	GPIO6_IO01	Input	PU (100K)
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	GPIO6_IO02	Input	PU (100K)
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	GPIO6_IO03	Input	PU (100K)
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	GPIO6_IO04	Input	PU (100K)
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	GPIO6_IO05	Input	PU (100K)
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	GPIO5_IO22	Input	PU (100K)
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	GPIO5_IO23	Input	PU (100K)
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	GPIO5_IO24	Input	PU (100K)
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	GPIO5_IO25	Input	PU (100K)
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	GPIO5_IO26	Input	PU (100K)
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	GPIO5_IO27	Input	PU (100K)
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	GPIO5_IO20	Input	PU (100K)
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	GPIO5_IO19	Input	PU (100K)
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	GPIO5_IO18	Input	PU (100K)
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	GPIO5_IO21	Input	PU (100K)
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	GPIO4_IO16	Input	PU (100K)
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	GPIO4_IO17	Input	PU (100K)
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	GPIO4_IO18	Input	PU (100K)
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	GPIO4_IO19	Input	PU (100K)
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	GPIO4_IO20	Input	PU (100K)
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	GPIO4_IO21	Input	PU (100K)
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	GPIO4_IO22	Input	PU (100K)
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	GPIO4_IO31	Input	PU (100K)
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	GPIO5_IO05	Input	PU (100K)
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	GPIO5_IO06	Input	PU (100K)
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	GPIO5_IO07	Input	PU (100K)

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
AC	DRAM_D4	DRAM_VREF	DRAM_DQM0	DRAM_D2	DRAM_D13	DRAM_DQM1	DRAM_D15	DRAM_D22	DRAM_D28	DRAM_SDQS3	DRAM_D31	DRAM_A11	DRAM_A6	DRAM_A0	DRAM_SDBA0	DRAM_SDODT0	DRAM_A13	DRAM_D34	DRAM_D39	DRAM_DQM5	DRAM_D47	DRAM_D48	DRAM_D53	DRAM_D51	DRAM_D55
AD	DRAM_D5	DRAM_D0	DRAM_SDQS0_B	GND	DRAM_D8	DRAM_SDQS1	GND	DRAM_SDQS2	DRAM_D29	GND	DRAM_D30	DRAM_A12	GND	DRAM_SDCLK_1	DRAM_SDCLK_0	GND	DRAM_CS1	DRAM_SDQS4	GND	DRAM_SDQS5	DRAM_D43	GND	DRAM_SDQS6	DRAM_DQM6	DRAM_D54
AE	GND	DRAM_D1	DRAM_SDQS0	DRAM_D7	DRAM_D9	DRAM_SDQS1_B	DRAM_D11	DRAM_SDQS2_B	DRAM_D24	DRAM_DQM3	DRAM_D26	DRAM_A9	DRAM_A5	DRAM_SDCLK_1_B	DRAM_SDCLK_0_B	DRAM_CAS	ZQPAD	DRAM_SDQS4_B	DRAM_D35	DRAM_SDQS5_B	DRAM_D46	DRAM_D49	DRAM_SDQS6_B	DRAM_D50	GND