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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	4 Core, 32-Bit
Speed	1.2GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	SATA 3Gbps (1)
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-20°C ~ 105°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA, FCBGA
Supplier Device Package	624-FCPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6q5eym12ce

  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
  - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
  - Three USB 2.0 (480 Mbps) hosts:
    - One HS host with integrated High Speed PHY
    - Two HS hosts with integrated High Speed Inter-Chip (HS-IC) USB PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
  - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
  - SSI block capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - ESAI is capable of supporting audio sample frequencies up to 260 kHz in I2S mode with 7.1 multi channel outputs
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode
    - One of the five UARTs (UART1) supports 8-wire while the other four support 4-wire. This is due to the SoC IOMUX limitation, because all UART IPs are identical.
  - Five eCSPI (Enhanced CSPI)
  - Three I2C, supporting 400 kbps
  - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000[1] Mbps
  - Four Pulse Width Modulators (PWM)
  - System JTAG Controller (SJC)
  - GPIO with interrupt capabilities
  - 8x8 Key Pad Port (KPP)
  - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
  - Two Controller Area Network (FlexCAN), 1 Mbps each
  - Two Watchdog timers (WDOG)
  - Audio MUX (AUDMUX)
  - MLB (MediaLB) provides interface to MOST Networks (150 Mbps) with the option of DTCP cipher accelerator

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

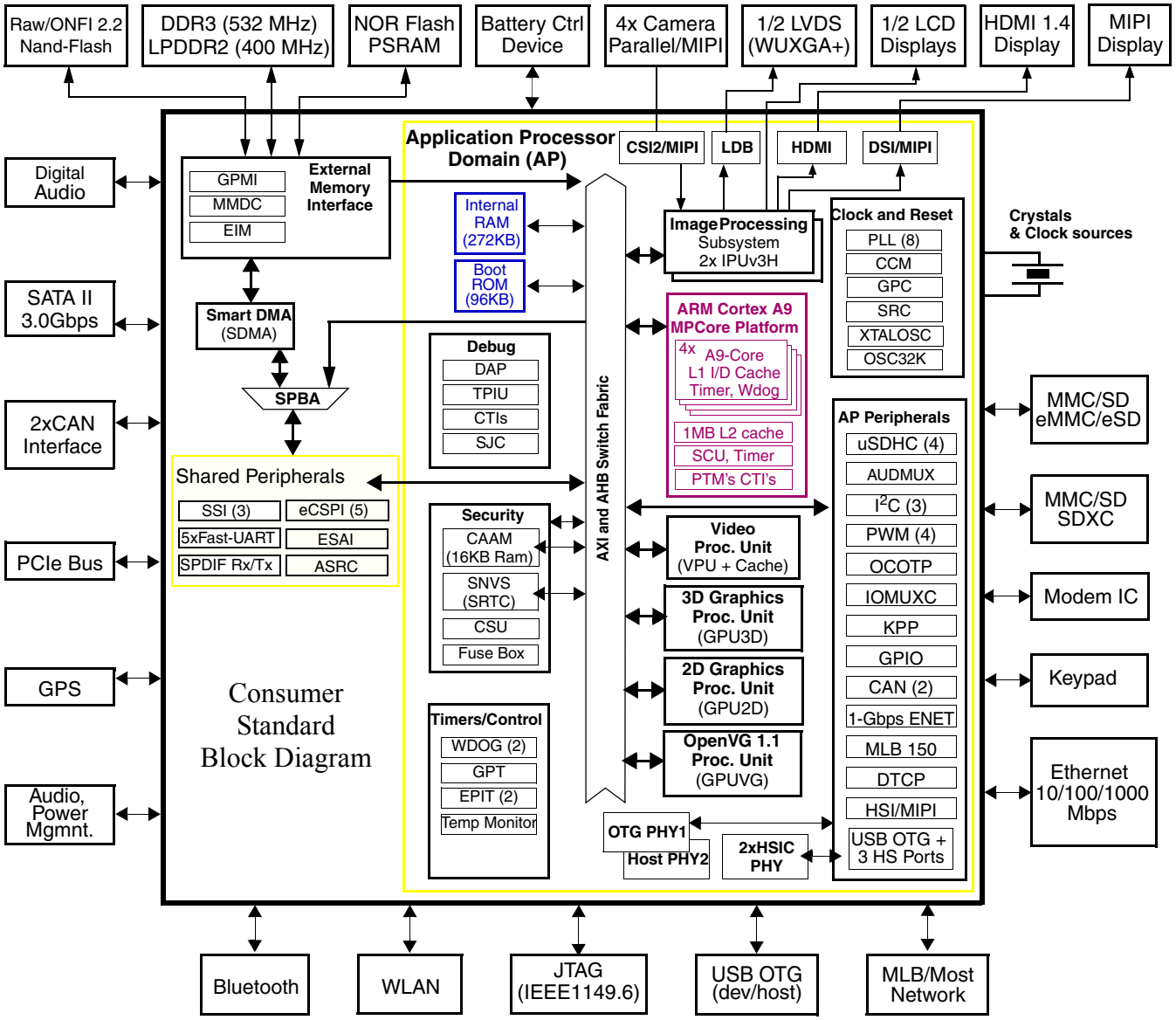

Figure 2. i.MX 6Dual/6Quad Consumer Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPU3Dv4	Graphics Processing Unit-3D, ver. 4	Multimedia Peripherals	The GPU2Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

Table 6. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
GPIO supplies[12]	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS_2P5[13] NVCC_MIPI	2.25	2.5	2.75	V	—
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	—
	HDMI_VPH	2.25	2.5	2.75	V	—
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	—
	PCIE_VPH	2.325	2.5	2.75	V	—
	PCIE_VPTX	1.023	1.1	1.3	V	—
SATA supply voltages	SATA_VP	0.99	1.1	1.3	V	—
	SATA_VPH	2.25	2.5	2.75	V	—
Junction temperature extended commercial	T_J	-20	—	105	°C	See *i.MX 6Dual/6Quad Product Lifetime Usage Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.
Junction temperature commercial	T_J	0	—	95	°C	See *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 See the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG) for bypass capacitors requirements for each of the *_CAP supply outputs.

3 For Quad core system, connect to VDD_ARM_IN. For Dual core system, may be shorted to GND together with VDD_ARM23_CAP to reduce leakage.

4 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

5 VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

6 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

7 VDD_ARM_CAP must not exceed VDD_CACHE_CAP by more than +50 mV. VDD_CACHE_CAP must not exceed VDD_ARM_CAP by more than 200 mV.

8 VDD_SOC_CAP and VDD_PU_CAP must be equal.

- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RX_N, PCIE_RX_P, PCIE_TX_N, and PCIE_TX_P) can remain unconnected. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual (IMX6DQRM) for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

Optionally LDO_SOC/VDD_SOC_CAP can be used to power the HDMI, PCIe, and SATA PHY's through external connections.

For additional information, see the i.MX 6Dual/6Quad reference manual (IMX6DQRM).

4.3.2 Regulators for Analog Modules

4.3.2.1 LDO_1P1 / NVCC_PLL_OUT

The LDO_1P1 regulator implements a programmable linear-regulator function from VDD_HIGH_IN (see Table 6 for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. The LDO_1P1 supplies the 24 MHz oscillator, PLLs, and USB PHY. A programmable brown-out detector is included in the regulator that can be used by the

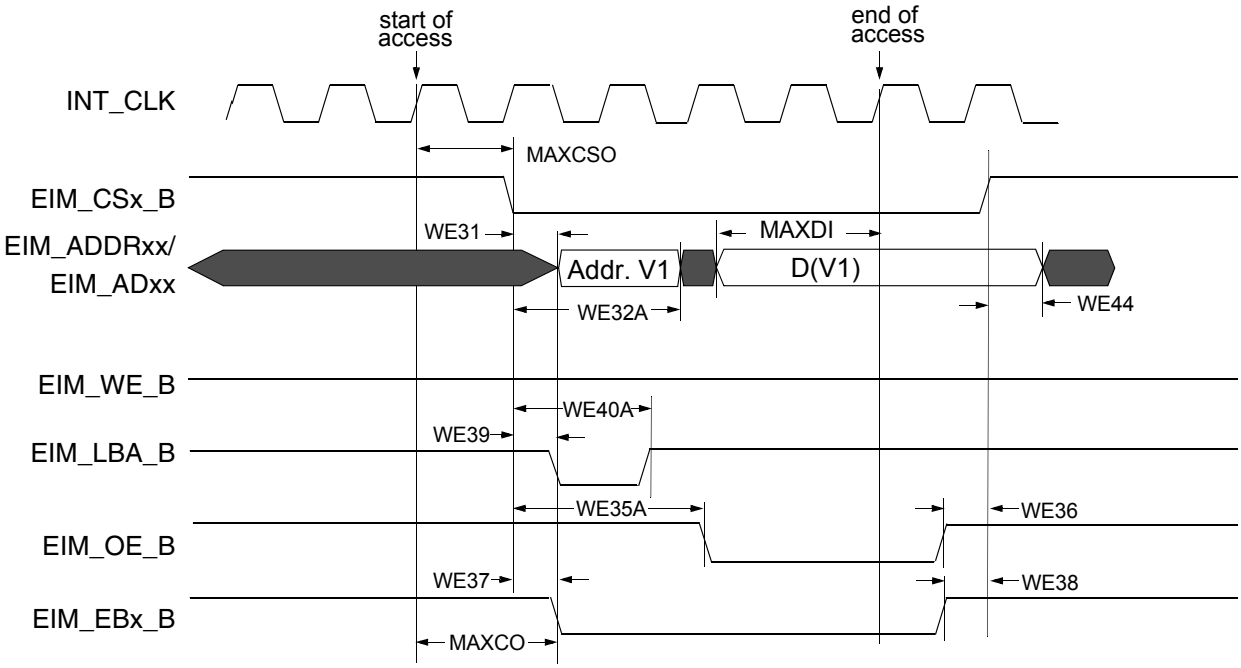

Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

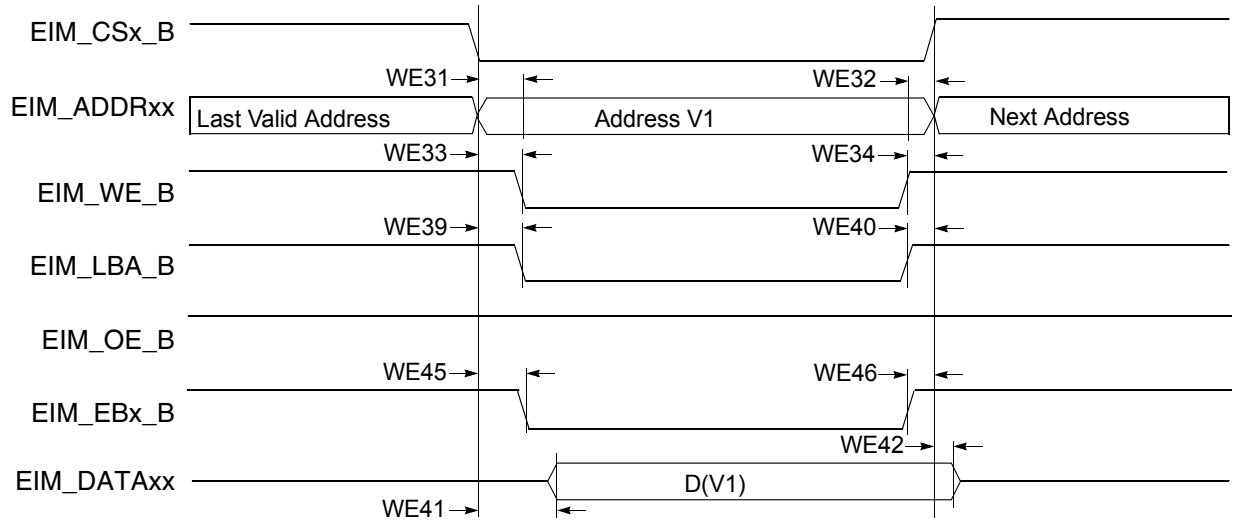

Figure 20. Asynchronous Memory Write Access

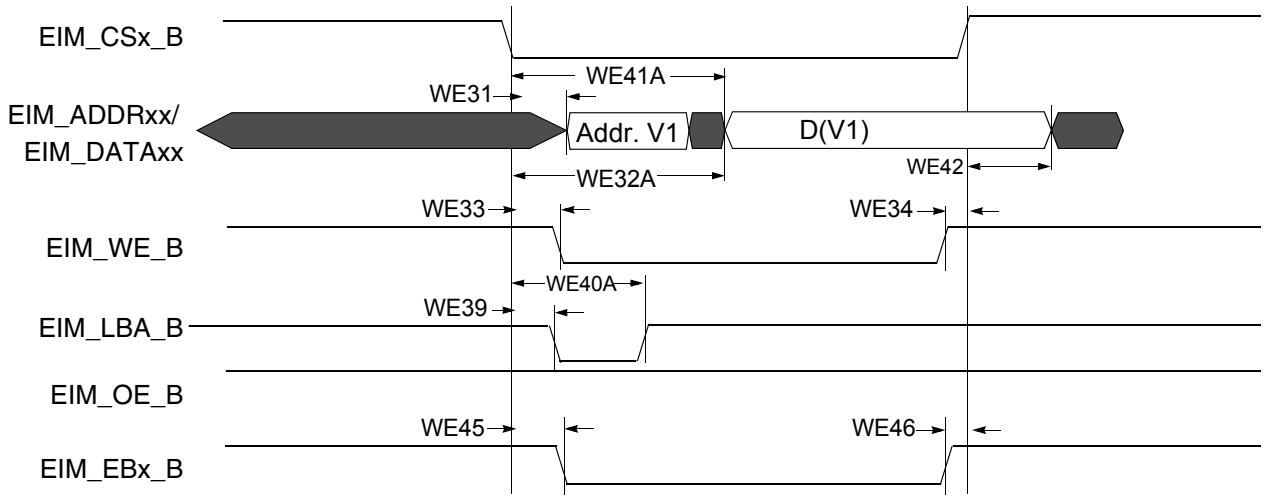

Figure 21. Asynchronous A/D Muxed Write Access

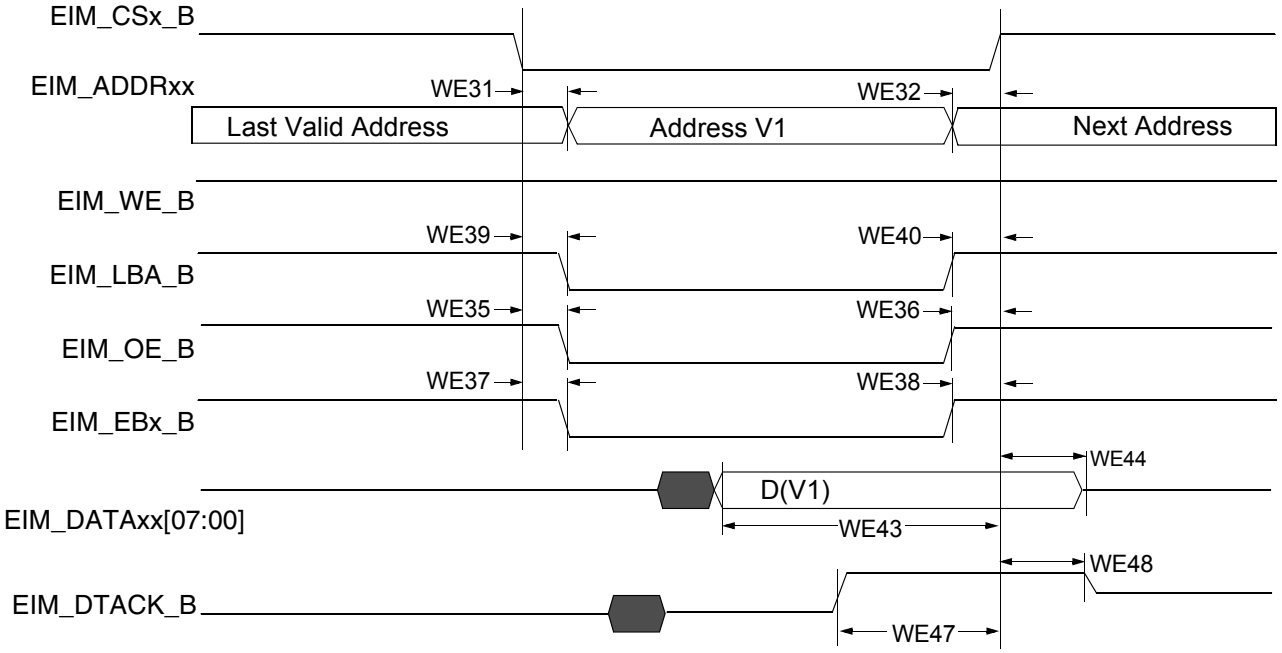

Figure 22. DTACK Mode Read Access (DAP=0)

4.12.4.3 SDR50/SDR104 AC Timing

Figure 41 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

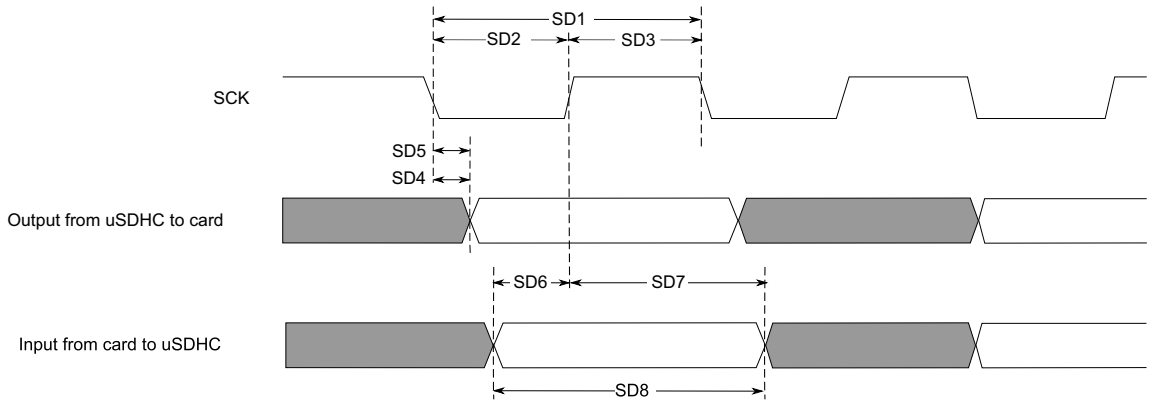

Figure 41. SDR50/SDR104 Timing

Table 52. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to SDx_CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to SDx_CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

4.12.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the ENET_RX_EN in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET_RXD[1:0] and ENET_RX_ER.

Figure 46 shows RMII mode timings. Table 57 describes the timing parameters (M16–M21) shown in the figure.

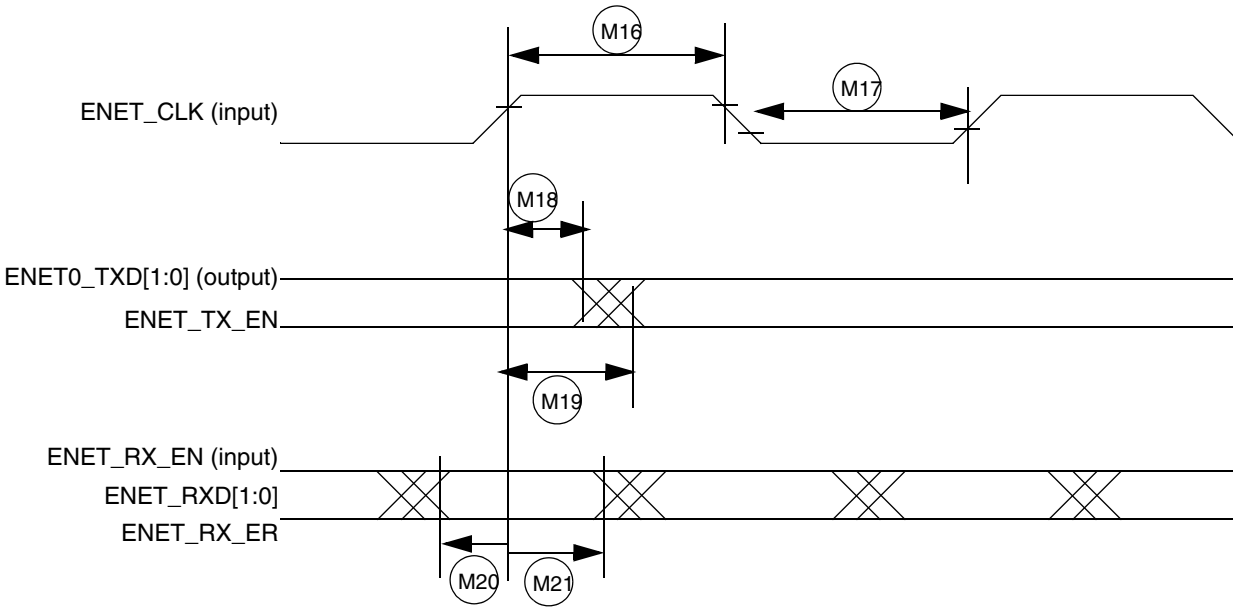

Figure 46. RMII Mode Signal Timing Diagram

Table 57. RMII Signal Timing

ID	Characteristic	Min	Max	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	13.5	ns
M20	ENET_RXD[1:0], ENET_RX_EN(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

Table 60. Switching Characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_F	Differential output signal fall time	20–80% RL = 50 Ω See Figure 57.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to 2x V_{SWING}	—	—	15	%
—	Differential signal undershoot	Referred to 2x V_{SWING}	—	—	25	%
Data and Control Interface Specifications						
$t_{Power-up}$[2]	HDMI 3D Tx PHY power-up time	From power-down to HSI_TX_READY assertion	—	—	3.35	ms

1 Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

2 For information about latencies and associated timings, see Section 4.12.7.1, "Latencies and Timing Information."

4.12.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 58 depicts the timing of I²C module, and Table 61 lists the I²C module timing characteristics.

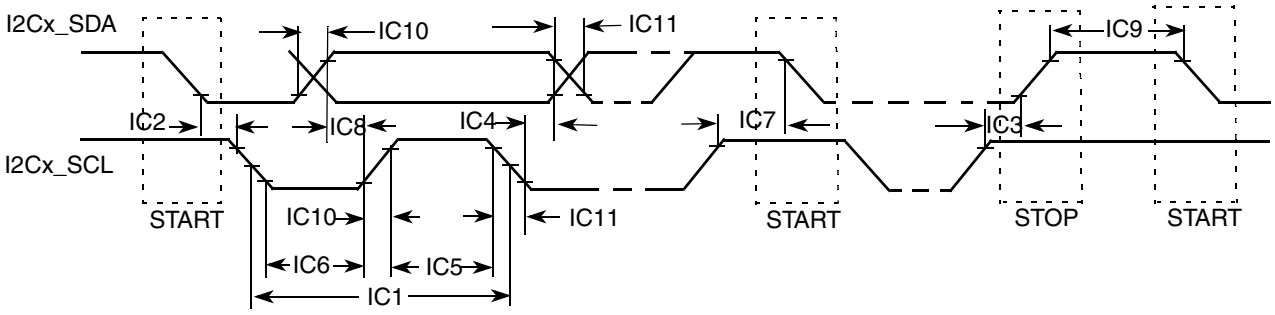

Figure 58. I²C Bus Timing

Table 61. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns

Table 69. Electrical and Timing Information (continued)

Symbol	Parameters	Test Conditions	Min	Typ	Max	Unit
t_{CDC}	DDR CLK duty cycle	$t_{CDC} = t_{CPH} / P_{DDRCLK}$	—	50	—	%
t_{CPH}	DDR CLK high time	—	—	1	—	UI
t_{CPL}	DDR CLK low time	—	—	1	—	UI
—	DDR CLK / DATA Jitter	—	—	75	—	ps pk-pk
$t_{SKEW[PN]}$	Intra-Pair (Pulse) skew	—	—	0.075	—	UI
$t_{SKEW[TX]}$	Data to Clock Skew	—	0.350	—	0.650	UI
t_r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
t_f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150	—	0.3UI	ps
$\Delta V_{CMTX(HF)}$	Common level variation above 450 MHz	80 Ω<= RL< = 125 Ω	—	—	15	mV_{rms}
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz	80 Ω<= RL< = 125 Ω	—	—	25	mV_p
LP Line Drivers AC Specifications						
t_{rlp}, t_{flp}	Single ended output rise/fall time	15% to 85%, C_L<70 pF	—	—	25	ns
t_{reo}	—	30% to 85%, C_L<70 pF	—	—	35	ns
$\delta V/\delta t_{SR}$	Signal slew rate	15% to 85%, C_L<70 pF	—	—	120	mV/ns
C_L	Load capacitance	—	0	—	70	pF
HS Line Receiver AC Specifications						
$t_{SETUP[RX]}$	Data to Clock Receiver Setup time	—	0.15	—	—	UI
$t_{HOLD[RX]}$	Clock to Data Receiver Hold time	—	0.15	—	—	UI
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	—	—	—	200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz	—	-50	—	50	mVpp
C_{CM}	Common mode termination	—	—	—	60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection	—	—	—	300	Vps
T_{MIN}	Minimum pulse response	—	50	—	—	ns
V_{INT}	Pk-to-Pk interference voltage	—	—	—	400	mV
f_{INT}	Interference frequency	—	450	—	—	MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.	—	—	—	1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.	—	—	—	2	pF

Table 72. MediaLB 6-Pin Interface Electrical DC Specifications (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Common-mode output voltage: $(V_{O+} - V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $\lvert V_{OCM, high} - V_{OCM, low} \rvert$	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note[2]	—	150	mVpp
Short circuit current	$\lvert I_{OS} \rvert$	See Note[3]	—	43	mA
Differential output impedance	Z_O	—	1.6	—	kΩ
Receiver Characteristics					
Differential clock input: • logic low steady-state • logic high steady-state • hysteresis	 V_{ILC} V_{IHC} V_{HSC}	See Note[4]	 50 -25	 -50 25	 mV mV mV
Differential signal/data input: • logic low steady-state • logic high steady-state	 V_{ILS} V_{IHS}	—	 — 50	 -50 —	 mV mV
Signal-ended input voltage (steady-state): • MLB_SIG_P, MLB_DATA_P • MLB_SIG_N, MLB_DATA_N	 V_{IN+} V_{IN-}	—	 0.5 0.5	 2.0 2.0	 V V

1 The signal-ended output voltage of a driver is defined as V_{O+} on MLB_CLK_P, MLB_SIG_P, and MLB_DATA_P. The signal-ended output voltage of a driver is defined as V_{O-} on MLB_CLK_N, MLB_SIG_N, and MLB_DATA_N.

2 Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-}.

3 Short circuit current is applicable when V_{O+} and V_{O-} are shorted together and/or shorted to ground.

4 The logic state of the receiver is undefined when -50 mV < V_{ID} < 50 mV.

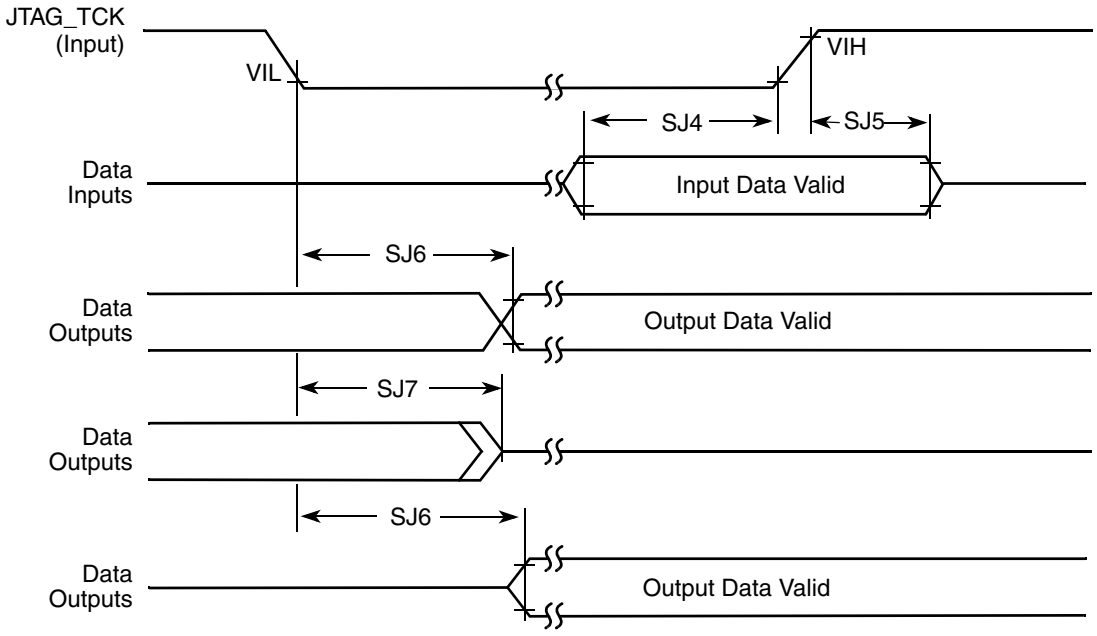

Figure 85. Boundary Scan (JTAG) Timing Diagram

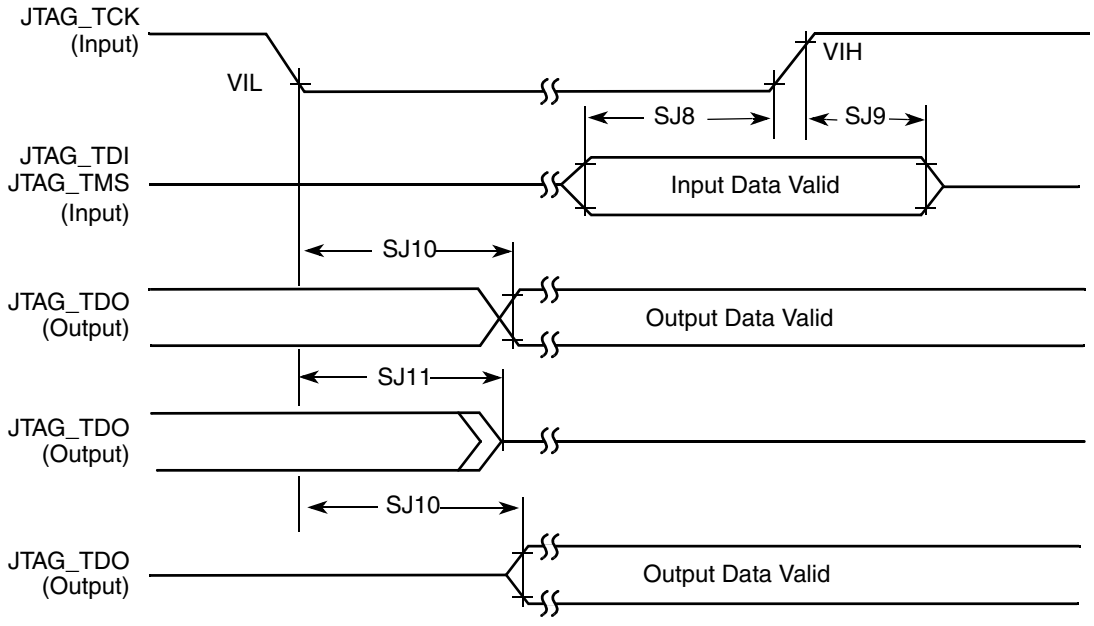

Figure 86. Test Access Port Timing Diagram

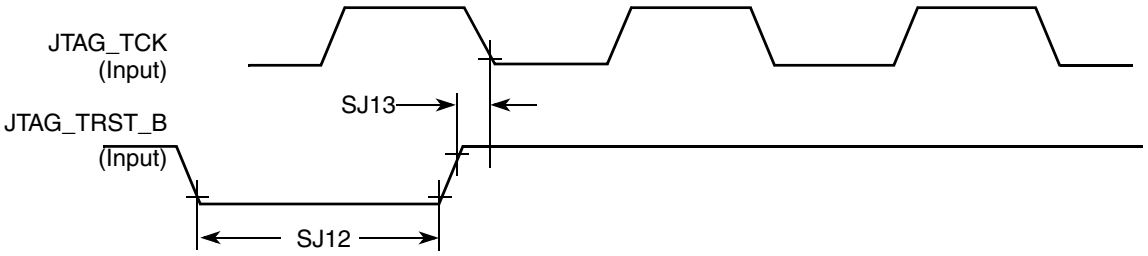

Figure 87. JTAG_TRST_B Timing Diagram

Table 79. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation $1/(3xT_{DC})$[1]	0.001	22	MHz
SJ1	JTAG_TCK cycle time in crystal mode	45	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	JTAG_TCK low to output data valid	—	40	ns
SJ7	JTAG_TCK low to output high impedance	—	40	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	25	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	44	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	44	ns
SJ12	JTAG_TRST_B assert time	100	—	ns
SJ13	JTAG_TRST_B set-up time to JTAG_TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.12.19 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 80 and Figure 88 and Figure 89 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

Table 84. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- AUDx_TXC and AUDx_RXC refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

4.12.20.4 SSI Receiver Timing with External Clock

Figure 93 depicts the SSI receiver external clock timing and Table 85 lists the timing parameters for the receiver timing with the external clock.

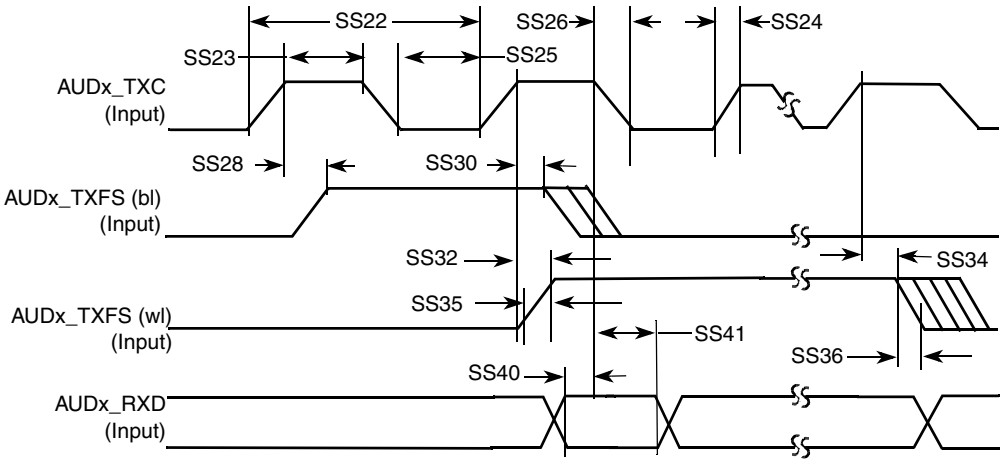

Figure 93. SSI Receiver External Clock Timing Diagram

4.12.21 UART I/O Configuration and Timing Parameters

4.12.21.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 86 shows the UART I/O configuration based on the enabled mode.

Table 86. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UARTx_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UARTx_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UARTx_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UARTx_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UARTx_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UARTx_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

Table 93. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name
EIM_A18	Input	BOOT_CFG3[2]
EIM_A19	Input	BOOT_CFG3[3]
EIM_A20	Input	BOOT_CFG3[4]
EIM_A21	Input	BOOT_CFG3[5]
EIM_A22	Input	BOOT_CFG3[6]
EIM_A23	Input	BOOT_CFG3[7]
EIM_A24	Input	BOOT_CFG4[0]
EIM_WAIT	Input	BOOT_CFG4[1]
EIM_LBA	Input	BOOT_CFG4[2]
EIM_EB0	Input	BOOT_CFG4[3]
EIM_EB1	Input	BOOT_CFG4[4]
EIM_RW	Input	BOOT_CFG4[5]
EIM_EB2	Input	BOOT_CFG4[6]
EIM_EB3	Input	BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 94 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 94. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	—
SPI	ECSPI-2	CSI0_DAT10, CSI0_DAT9, CSI0_DAT8, CSI0_DAT11, EIM_LBA, EIM_D24, EIM_D25	—
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	—
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	—
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	—
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSI0_DAT[19:4], CSI0_DATA_EN, CSI0_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported

6.2.5 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 98 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 98. 21 x 21 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN	MLB_DP	MLB_CN	SATA_TXP	GND	SATA_RXM	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	MLB_SP	MLB_DN	MLB_CP	SATA_TXM	SD3_CMD	SATA_RXP	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	SATA_REXT	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23
E	CSI_D2M	CSI_D2P	CSI_D0P	CSI_D0M	GND	GND	GND	NVCC_PLL_OUT	USB_OTG_VBUS	USB_H1_DP	TAMPER	TEST_MODE	SD3_DAT6	SD3_DAT0	NANDF_WP_B	SD4_CLK	NANDF_D6	SD4_DAT4	SD1_DAT2	SD2_DAT1	RGMII_TD2	EIM_EB2	EIM_D22	EIM_D26	EIM_D27
F	CSI_D3P	CSI_D3M	CSI_CLK0P	CSI_CLK0M	GND	GND	GND	GND	VDDUSB_CAP	USB_H1_DN	PMIC_STBY_REQ	BOOT_MODE1	SD3_DAT7	SD3_DAT1	NANDF_CS0	NANDF_D2	SD4_DAT2	SD1_DAT3	SD2_CMD	RGMII_TD1	EIM_D17	EIM_D24	EIM_EB3	EIM_A22	EIM_A24
G	DSI_D0P	DSI_D0M	GND	DSI_REXT	JTAG_TDI	JTAG_TDO	PCIE_VPH	PCIE_VPTX	VDD_SNVS_CAP	GND	VDD_SNVS_IN	SATA_VPH	SATA_VP	NVCC_SD3	NVCC_NANDF	NVCC_SD1	NVCC_SD2	NVCC_RGMII	GND	EIM_D20	EIM_D19	EIM_D25	EIM_D28	EIM_A17	EIM_A19

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	07/2015	• Added footnote to Table 1, “Example Orderable Part Numbers,” on page 3: If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz. • Section 1.2, “Features” changed Five UARTs, from *up to 4.0 Mbps*, to *up to 5.0 Mbps.* • Table 6, “Operating Ranges,” on page 23: Row: VDD_HIGH internal regulator, changed minimum parameter value from 2.8 to 2.7V. • Table 6, “Operating Ranges,” on page 23: Removed footnote: *VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM-VDDSOC/PU<50mV.* This was a duplicate footnote, renumbered footnotes accordingly. • Table 6, “Operating Ranges,” on page 23: Changed value: *Standby/DSM Mode, VDD_SOC_IN, minimum voltage, from 0.9V to 1.05V.* • Consumer: Added Table 18, “MLB PLL Electrical Parameters,” on page 37 which had erroneously been removed from previous revisions. • Table 8, “Maximum Supply Currents,” on page 27, Differentiated VDD_ARM_IN, VDD_ARM23_IN, and VDD_SOC_IN by frequency and by Power Virus/CoreMark maximum current. • Table 21, “XTALI and RTC_XTALI DC Parameters,” on page 39, Added rows: *Input capacitance*; *Startup current*; and *DC input current* and their values. • Table 41, “EIM Bus Timing Parameters,” on page 55, Changed WE4–WE17 minimum and maximum parameter values from, *0.5 t (k+1)/2-1.25*, to *0.5 x t x (k+1)-1.25.* • Table 42, “EIM Asynchronous Timing Parameters Relative to Chip Select¹,” on page 62 Added to end of formulas in the minimum, typical, and maximum parameter values for WE31–WE42 and WE45–WE46, *×t*. For example from *3-CSN*, to *3-CSN×t*. Also added maximum value to MAXDTI of 10. • Table 58, “DDR3/DDR3L Write Cycle,” on page 90, Changed minimum parameter value of DDR17 from 240 to 125; and of DDR18 from 240 to 150. • Figure 29, “LPDDR2 Command and Address Timing Diagram,” on page 91, LP2 signal cycle reduced. • Table 62, “LPDDR2 Write Cycle,” on page 93, Changed LP21 minimum and maximum parameter value from -0.25/+0.25 to 0.8/1.2. • Figure 35, "ECSPI Master Mode Timing Diagram," on page 74, Added footnote: *Note: ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 36, "ECSPI Slave Mode Timing Diagram," on page 75, Added footnote: *Note: ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.* • Figure 59, "Gated Clock Mode Timing Diagram," on page 96, Corrected IPU2_CSIx_HSYNC trace drawing. • Section 4.12.23, “USB PHY Parameters” Specified *Battery Charging Specification* applies to portable devices only. *(Revision History table continues on next page.)*

Table 99. i.MX 6Dual/6Quad Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 2	04/2013	Substantive changes throughout this document are as follows: • Incorporated standardized signal names. This change is extensive throughout. Added reference to EB792, i.MX Signal Name Mapping. • Figures updated to align to standardized signal names. • Aligned references to FCBGA to read FC**P**BGA throughout document. • Updated references to eMMC standard to include 4.41. • Added MediaLB feature and DTCP module. • Table 2, “i.MX 6Dual/6Quad Modules List,” Changed reference to Global Power Controller to read General Power Controller. • Table 4, “Absolute Maximum Ratings,” Added VDD_ARM23_IN to Core supply voltages. • Table 6 “Operating Ranges”: Run Mode - LDO Enabled, VDD_ARM_IN/VDD_ARM23_IN, 792 MHz, input voltage minimum changed to 1.275V and VDD_ARM CAP minimum changed to 1.150V. NVCC_NAND, changed to NVCC_NANDF. • Table 6 “Operating Ranges”: Added reference for information on product lifetime: *i.MX 6Dual/6Quad Product Usage Lifetime Estimates Application Note*, AN4724. • Table 9. “Maximum Supply Currents”: Added current for i.MX6Dual • Table 10 “Stop Mode Current and Power Consumption”: Added SNVS Only mode. • Table 22 “GPIO I/O DC Parameters”: Removed parameters Iskod and Isspp. • Table 48, “ECSPI Master Mode Timing Parameters,” Updated parameter CS6 ECSPIx_SSx Lag Time (CS hold time) Min from Half SCLK period to Half SCLK period-2. • Table 77 “SD/eMMC4.3 Interface Timing Specification,” eMMC parameter SD8 value Min updated from 5.6 ns to 1.5 ns. • Table 89 RGMII Signal Switching Specifications RGMII parameter TskewR units corrected. • Table 134 “21 x 21 mm Functional Contact Assignments,” Updated GPIO_1 Ball Name value to PU (100K). • Table 134 “21 x 21 mm Functional Contact Assignments,” Clarification of ENET_REF_CLK naming. • Removed section, EIM Signal Cross Reference. Signal names are now aligned with reference manual. • Section 1.2, “Features added bulleted item regarding the SOC-level memory system. • Section 4.2.1, “Power-Up Sequence” updated wording. • Section 4.3.2, “Regulators for Analog Modules”: Added NVCC_PLL_OUT to section heading. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters”: Added section. • Section 4.10, “General-Purpose Media Interface (GPMI) Timing” figures replaced, tables revised.