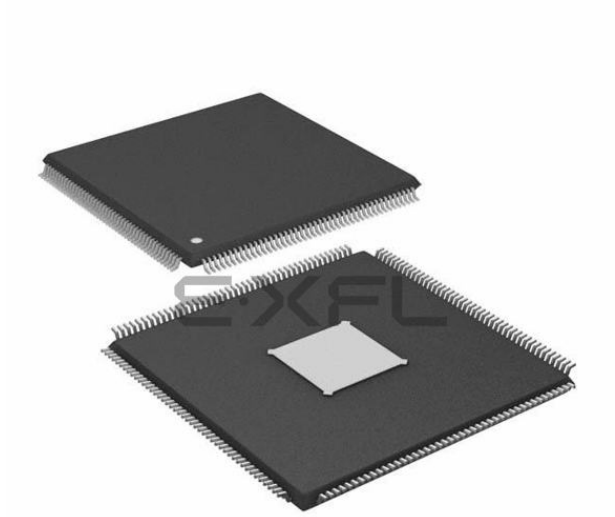

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/sp5748gtk0amku6r

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Three System Timer Module (STM)
  - Four Software WatchDog Timers (SWT)
  - 96 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1) and 1149.7 (cJTAG)
- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS and TDM) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
  - ISO26262 ASIL compliance
- Multiple operating modes
  - Includes enhanced low power operation

1 Block diagram

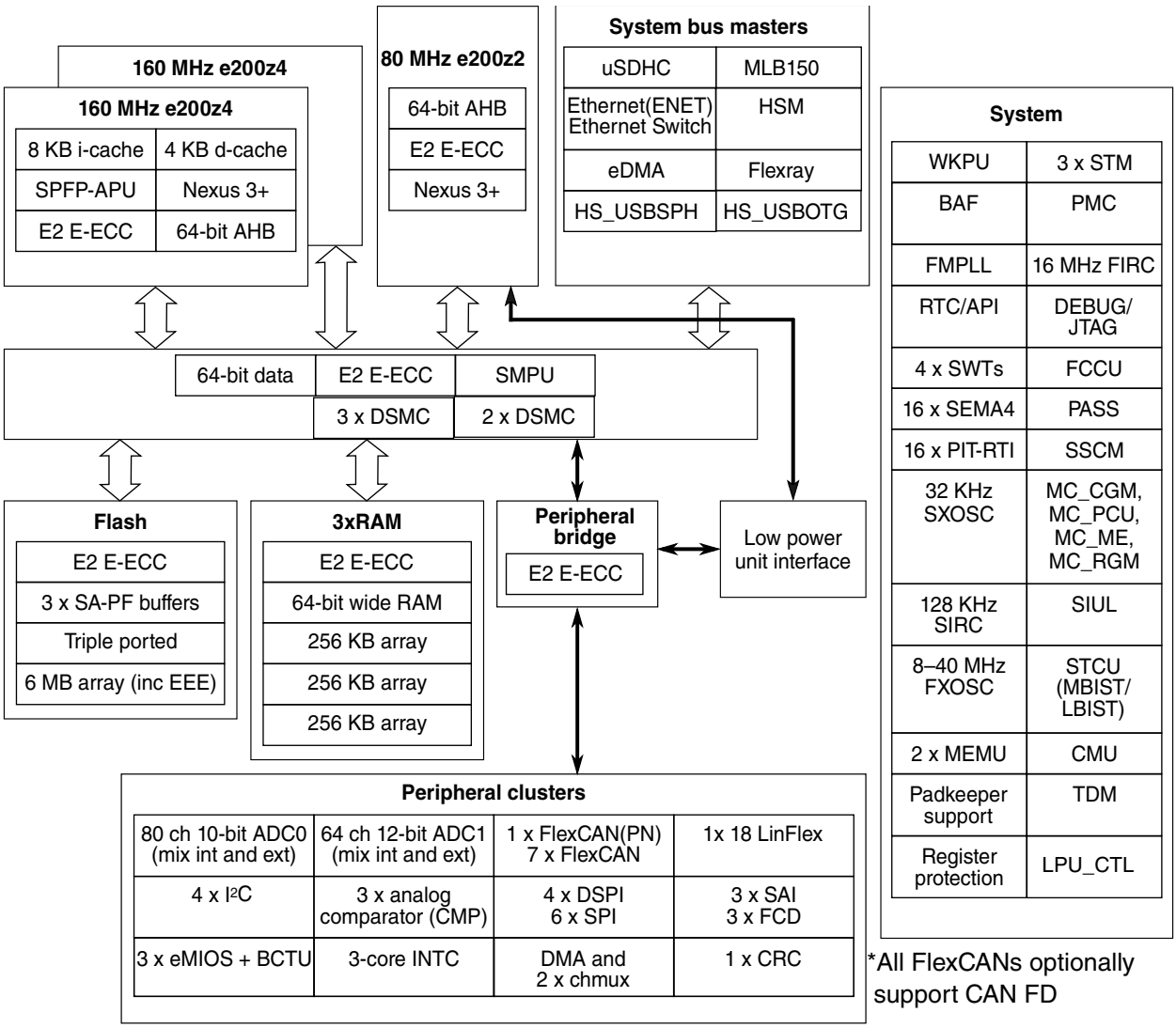


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
T_A	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.

NOTE

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)

Symbol	Parameter	Conditions [1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	5.5	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[5]	Analog Comparator DAC reference voltage	—	3.15	5.5	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with C_{flash_reg}.
4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. This supply is shorted VDD_HV_A on lower packages.

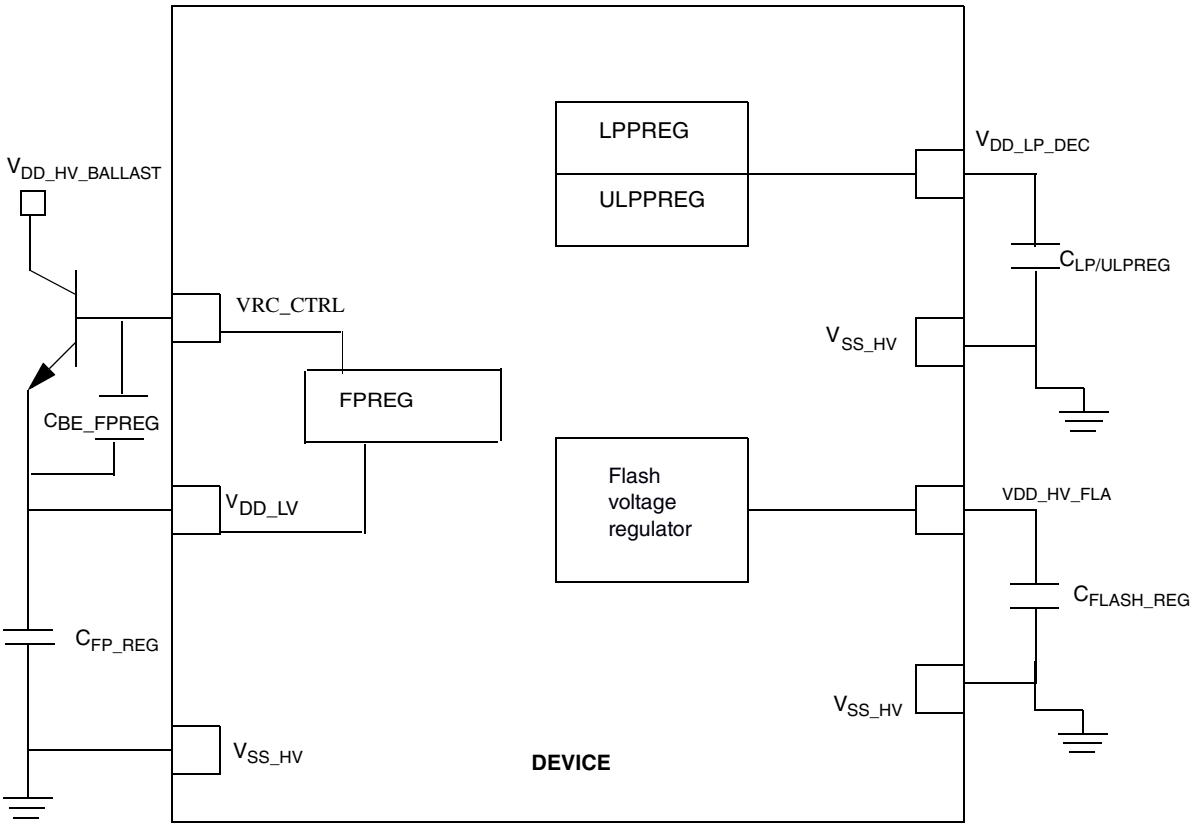


Figure 2. Voltage regulator capacitance connection

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{fp_reg}[1]	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2[2]	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C_{be_fpreg}[3]	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		
C_{flash_reg}[4]	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm

Table continues on the next page...

7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If $V_{DD\_HV\_BALLAST}$ is supplied from the same source as VDD_HV_A this condition is implicitly met):
   - During power-up, $V_{DD\_HV\_BALLAST}$ must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
   - During power-down, $V_{DD\_HV\_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 8) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may cause the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

4.4 Voltage monitor electrical characteristics

Table 9. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Powerup	0.930	0.979	1.028	V
			Trimmed				0.959	0.979	0.999	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				1.009	1.029	1.049	V

Table continues on the next page...

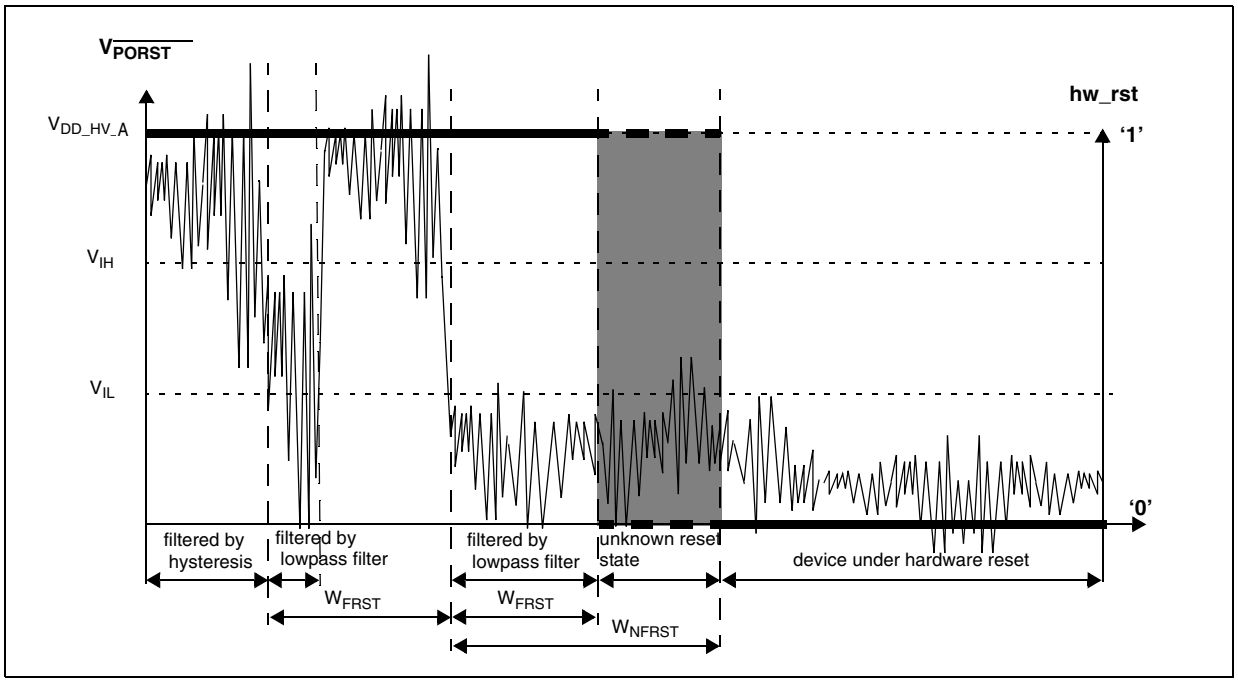


Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_A}$ +0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1]	Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\lvert I_{WPU} \rvert$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

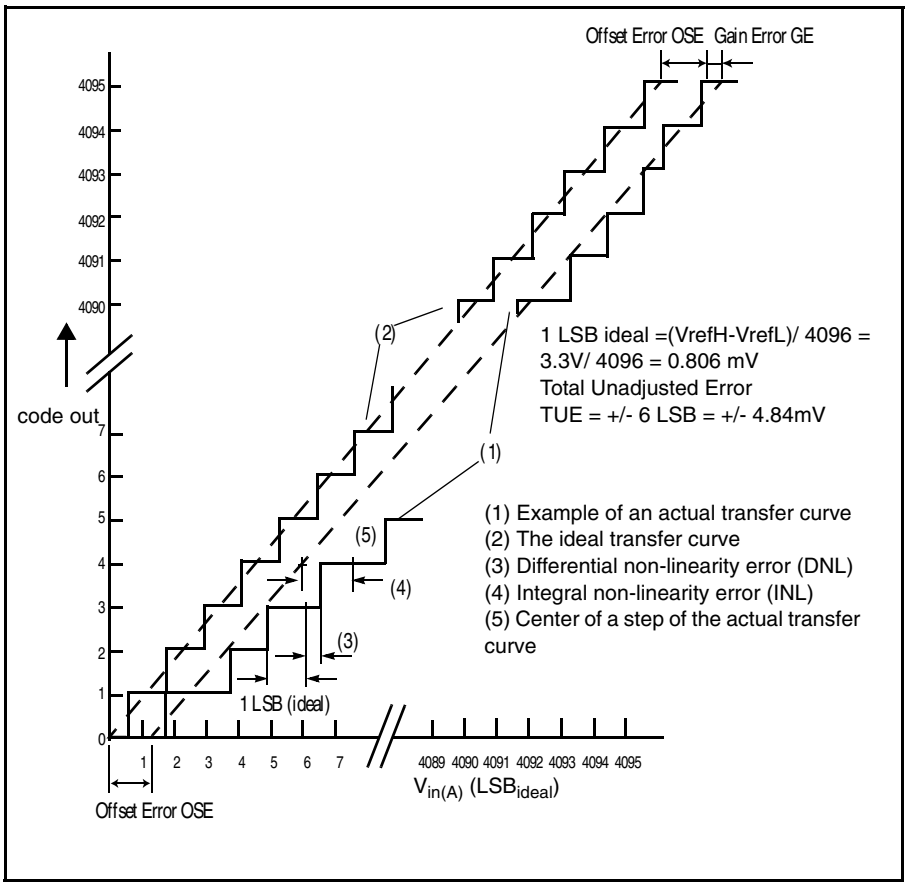


Figure 5. ADC characteristics and error definitions

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1\_CMP\_REF}$	V
V_{AIO}	Analog input offset voltage [1]	-42	—	42	mV
V_H	Analog comparator hysteresis [2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV
	• CR0[HYSTCTR] = 10	—	60	105	mV
	• CR0[HYSTCTR] = 11				
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	21	µs
	Analog comparator initialization delay, High speed mode[4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

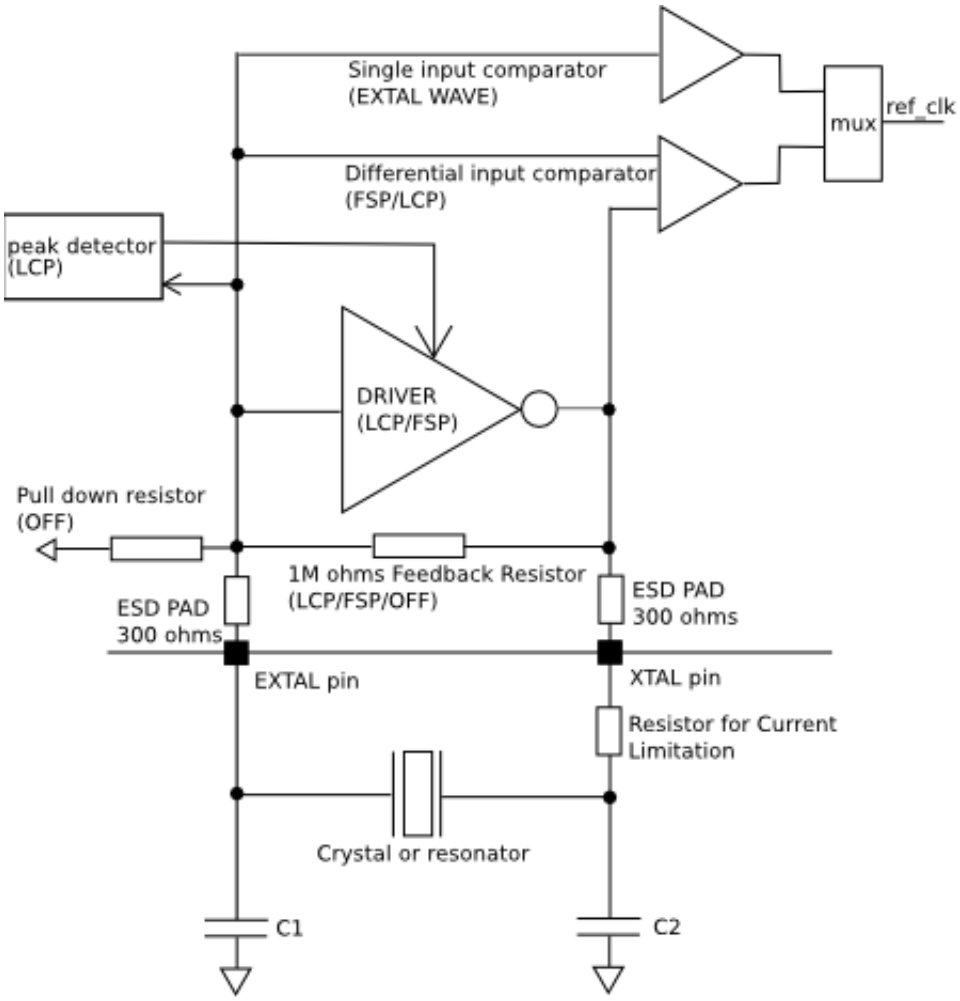


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		

Table continues on the next page...

Table 30. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max	Units
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	$_{SS}$ inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8[1]	—	

Table continues on the next page...

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

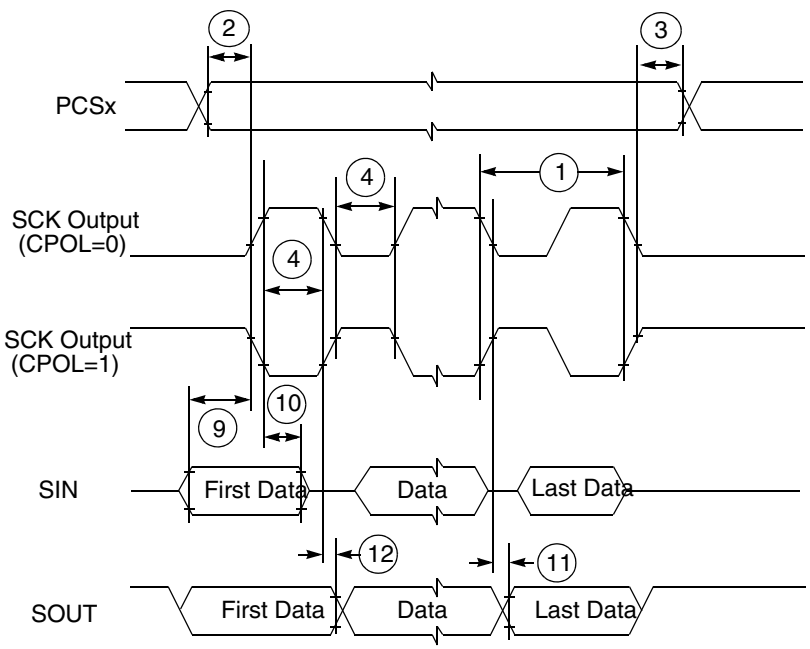
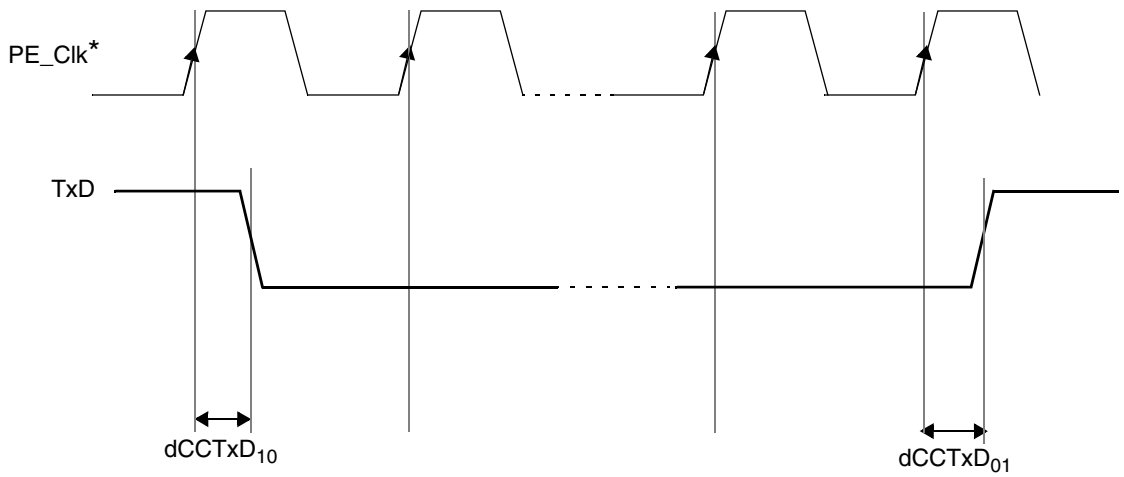


Figure 8. DSPI classic SPI timing — master, CPHA = 0

Table 39. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

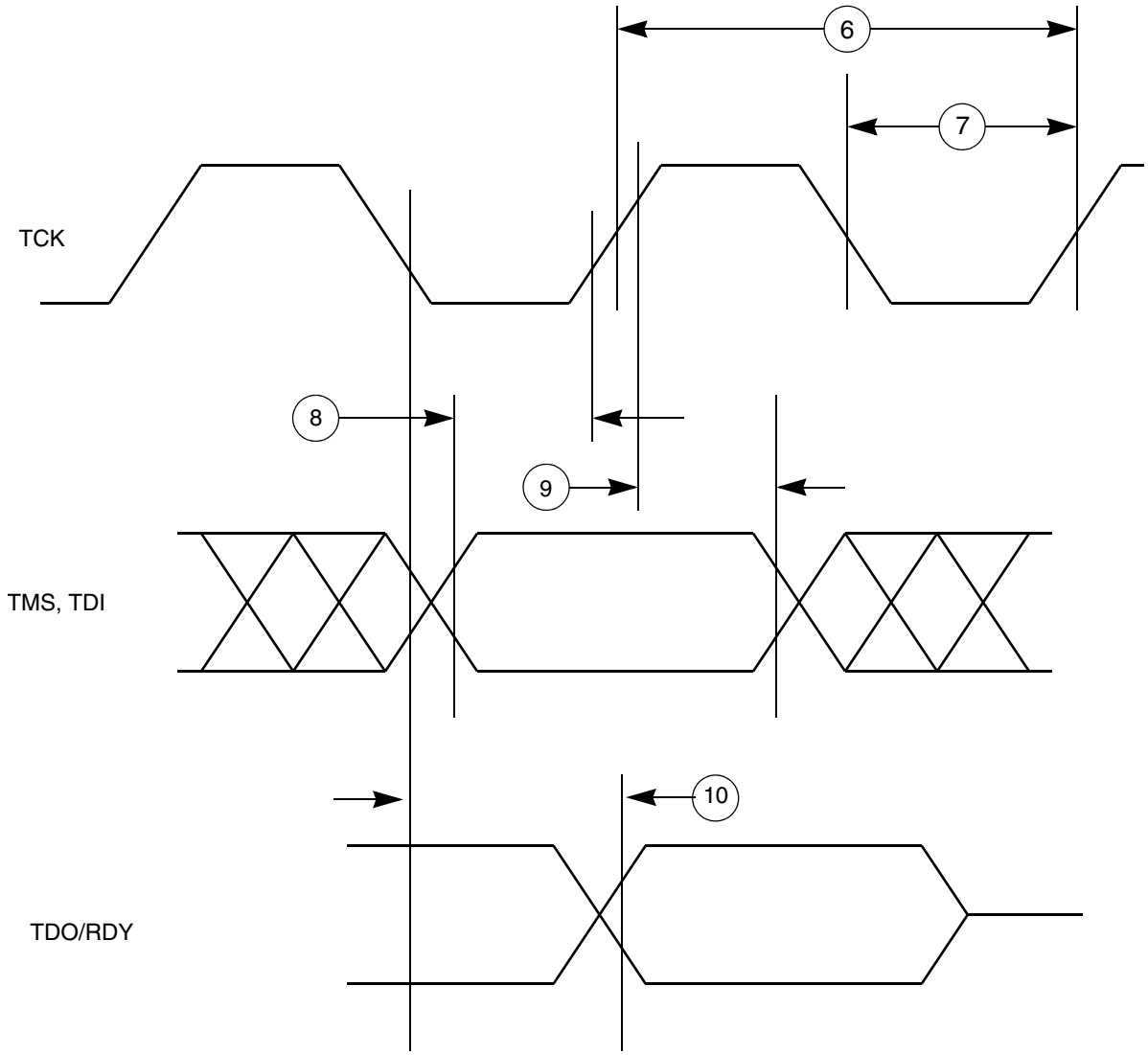


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	39.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	22.9	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	28.5	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	18.3	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	9.5	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	5.8	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	6.4	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
176-pin LQFP-EP	98ASA00673D
256 MAPBGA	98ASA00346D
324 MAPBGA	98ASA10582D

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

Table 54 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 54. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ [1]	Max	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T_{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T_{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T_{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Revised Electromagnetic Interference (EMI) characteristics section • Revised DC electrical specifications @ 3.3V Range table for naming convections. • Revised DC electrical specifications @ 5 V Range table for naming conventions • Deleted MLB 6-pin Electrical Specifications • Removed PORST characteristics from Functional reset pad electrical characteristics table • Added section PORST electrical characteristics • Revised Input impedance and ADC accuracy section to remove SNR, THD, SINAD, ENOB, • Revised 32 kHz oscillator electrical specifications table to remove 'Vpp' row. • Updated 16 MHz RC Oscillator electrical specifications table for statuptime, cycle to cycle jitter, and lonf term jitter • Updated 128 KHz Internal RC oscillator electrical specifications table. • Updated PLL electrical specifications table • Added Jitter Calculation table • Added Percentage of Sample exceeding specified value of jitter table

		• Revised Memory interfaces section
		• Revised Communication interfaces section
		  • Updated note
		  • Added Continuous SCK timing table
		  • Added DSPI high speed mode I/Os table
		• Updated input transition value in section MLB 3-pin interface electrical specifications
		• Deleted MLB 6-pin interface DC characteristics section
		• Deleted MLB 6-pin interface AC characteristics section
		• Updated JTAG pin AC electrical characteristics table
		• Revised table under Thermal attributes section
		• Updated Obtaining package dimensions section for Freescale Document numbers

3	12 May 2015	• Editorial updates throughout the sections
		• Renamed '176 LQFP' package to '176 LQFP-EP'
		• Added following sections:
		  • Block diagram
		  • Family comparison
		  • Ordering Information
		• In table: Absolute maximum ratings as follows:
		  • Removed row for symbol: 'V_{SS_HV}'
		  • Added symbol: 'V_{DD_LV}'
		  • Updated 'Max' column for symbol 'V_{INA}'
		  • Added footnote to 'Conditions' column
		  • Removed footnote from 'Max' column
		• In section: Recommended operating conditions
		  • Added opening text: ''The following table describes the operating conditions ... "
		  • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... "
		  • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)
		  • Added footnote to 'Conditions' cloumn
		  • Updated footnote for 'Min' column
		  • Removed footnote from symbols '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$'
		  • Removed row for symbol: 'V_{SS_HV}'
		  • Updated 'Parameter' column for symbol '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}'
		  • Updated 'Min' column for symbol '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$'
		  • Updated 'Parameter' 'Min' 'Max' column for symbol '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$'
		  • Added footnote to symbol 'V_{DD_LV} '
		  • Removed footnote from symbol '$V_{IN1\_CMP\_REF}$'

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In table: Functional Pad AC Specifications @ 3.3 V Range
		  • Updated values for symbol 'pad_sr_hv (output)'
		• In table: DC electrical specifications @ 3.3V Range
		  • Updtaed values for VDD_HV_x, Vih, Vhys
		  • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		• In table: Functional Pad AC Specifications @ 5 V Range
		  • Updated values for symbol 'pad_sr_hv (output)'
		• In table DC electrical specifications @ 5 V Range
		  • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys

		• In section: PORST electrical specifications
		  • In table: PORST electrical specifications
		  • Updated 'Min' value for $W_{NFPORST}$
		  • Corrected 'Unit' for V_{IH} and V_{IL}
		
		• In section: Peripheral operating requirements and behaviours
		  • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit)
		
		• In section: Analogue Comparator (CMP) electrical specifications
		  • In table: Comparator and 6-bit DAC electrical specifications
		  • Updated 'Max' value of I_{DDLS}
		  • Updated 'Min' and 'Max' for V_{AIO} and DNL
		  • Updated 'Descripton' 'Min' 'Max' od V_H
		  • Updated row for tDHS
		  • Added row for tDLS
		  • Removed row for VCMPOh and VCMPOl
		
		• In section: Clocks and PLL interfaces modules
		  • Revised table: Main oscillator electrical characteristics
		  • In table: 16 MHz RC Oscillator electrical specifications
		  • Updated 'Max' of Tstartup
		  • In table: 128 KHz Internal RC oscillator electrical specifications
		  • Removed Uncaliberated 'Condition' for Fosc
		  • Updated 'Min' and 'Max' of Caliberated Fosc
		  • Updated 'Temperature dependence' and 'Supply dependence'
		  • In table: PLL electrical specifications
		  • Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption
		  • Removed 'Typ' value of Duty Cycle at pllclkout
		  • Removed 'Min' from calibration mode of Lock Time
		  • In table: Jitter calculation
		  • Added 1 Sigma Random Jitter value for Long term jitter

		• In section Flash read wait state and address pipeline control settings • Revised table: Flash Read Wait State and Address Pipeline Control • Removed section: On-chip peripherals • Added section: 'Reset sequence'
Rev4	Feb 10 2017	• Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics • Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics • Updated SIUL2_MSCRn[SRC 1:0]=11@25pF max value; SIUL2_MSCRn[SRC 1:0]=11@50pF min value; SIUL2_MSCRn[SRC 1:0]=10@25pF min and max values in AC specifications @ 3.3 V Range

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated VIH min and VIL max values in Main oscillator electrical characteristics • Replaced ipp_sre[1:0] by SIUL2_MSCRn[SRC 1:0] in AC specifications @ 3.3 V Range, DC electrical specifications @ 3.3V Range • Functional reset sequence short, unsecure boot corrected Reset sequence duration • Added NVM memory map and RAM memory map Family comparison • Added BAF execution duration section BAF execution duration • Supply names (VDD_LV, VSS_LV replace dvss, avss, dvdd, avdd) corrected in Jitter calculation table PLL electrical specifications • Updated Ordering information: Fab and Mask version indicator • Updated tpsus typical and max values Flash memory AC timing specifications • Added Notes on IBIS models use in AC specifications @3.3 V Range AC specifications @ 3.3 V Range • Updated Vol value in DC electrical specifications @ 3.3V Range DC electrical specifications @ 3.3V Range • Added Notes on IBIS models in Functional Pad AC Specifications @ 5 V Range AC specifications @ 5 V Range • Updated Vol values in DC electrical specifications @5V Range DC electrical specifications @ 5 V Range • Updated IDD Current values Supply current characteristics • Updated STANDBY current consumption with FIRC ON Supply current characteristics • Thermal numbers update for 256MAPBGA Thermal attributes • POR_HV Trim values removed Voltage monitor electrical characteristics • ADC analog pad leakage for 105 C added ADC electrical specifications • IDD STANDBY0, 1, 2 and 3 added Supply current characteristics
Rev5	July 31 2017	• Updated Standby2 value to 125 C in Standby current consumption characteristics • Corrected typo in Note from "case" to "cause" Voltage regulator electrical characteristics • Updated propagation delay from 14 to 21 in ACMP electrical specifications