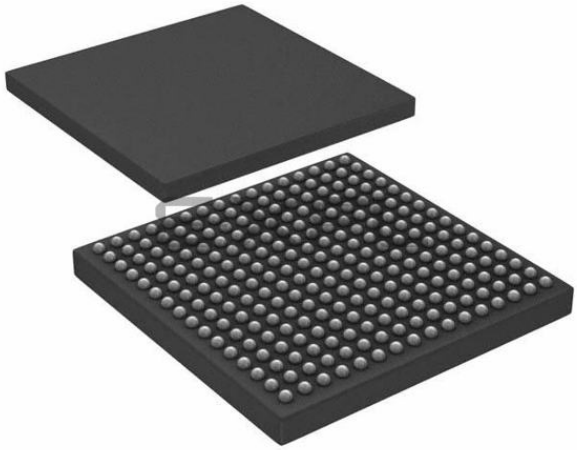

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | e200z2, e200z4 |
| Core Size | 32-Bit Dual-Core |
| Speed | 80MHz/120MHz |
| Connectivity | CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG |
| Peripherals | DMA, LVD, POR, WDT |
| Number of I/O | 178 |
| Program Memory Size | 4MB (4M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 512K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 80x10b, 64x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-MAPPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747ck1cmj2r |

# Table of Contents

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

## Table 2. MPC5748G Family Comparison - NVM Memory Map 1

| Start Address | End Address | Flash block | RWW | MPC5746 | MPC5747 | MPC5748 |
|---|---|---|---|---|---|---|
| 0x01000000 | 0x0103FFFF | 256 KB code Flash block 0 | 6 | available | available | available |
| 0x01040000 | 0x0107FFFF | 256 KB code Flash block 1 | 6 | available | available | available |
| 0x01080000 | 0x010BFFFF | 256 KB code Flash block 2 | 6 | available | available | available |
| 0x010C0000 | 0x010FFFFF | 256 KB code Flash block3 | 6 | available | available | available |
| 0x01100000 | 0x0113FFFF | 256 KB code Flash block 4 | 6 | available | available | available |
| 0x01140000 | 0x0117FFFF | 256 KB code Flash block 5 | 6 | available | available | available |
| 0x01180000 | 0x011BFFFF | 256 KB code Flash block 6 | 6 | available | available | available |
| 0x011C0000 | 0x011FFFFF | 256 KB code Flash block 7 | 6 | available | available | available |
| 0x01200000 | 0x0123FFFF | 256 KB code Flash block 8 | 7 | available | available | available |
| 0x01240000 | 0x0127FFFF | 256 KB code Flash block 9 | 7 | available | available | available |
| 0x01280000 | 0x012BFFFF | 256 KB code Flash block 10 | 7 | not available | available | available |
| 0x012C0000 | 0x012FFFFF | 256 KB code flash block 11 | 7 | not available | available | available |
| 0x01300000 | 0x0133FFFF | 256 KB code flash block 12 | 7 | not available | available | available |
| 0x01340000 | 0x0137FFFF | 256 KB code flash block 13 | 7 | not available | available | available |
| 0x01380000 | 0x013BFFFF | 256 KB code flash block 14 | 7 | not available | not available | available |
| 0x013C0000 | 0x013FFFFF | 256 KB code flash block 15 | 7 | not available | not available | available |
| 0x01400000 | 0x0143FFFF | 256 KB code flash block 16 | 8 | not available | not available | available |
| 0x01440000 | 0x0147FFFF | 256 KB code flash block 17 | 8 | not available | not available | available |
| 0x01480000 | 0x014BFFFF | 256 KB code flash block 18 | 8 | not available | not available | available |
| 0x14C0000 | 0x014FFFFF | 256 KB code flash block 19 | 9 | not available | not available | available |
| 0x01500000 | 0x0153FFFF | 256 KB code flash block 20 | 9 | not available | not available | available |
| 0x01540000 | 0x0157FFFF | 256 KB code flash block 21 | 9 | not available | not available | available |

**Table 3. MPC5748G Family Comparison - NVM Memory Map 2**

| Start Address | End Address | Flash block | RWW | MPC5747C<br>MPC5748C | MPC5746G<br>MPC5747G<br>MPC5748G |
|---|---|---|---|---|---|
| 0x00F90000 | 0x00F93FFF | 16 KB data Flash | 2 | available | available |
| 0x00F94000 | 0x00F97FFF | 16 KB data Flash | 2 | available | available |
| 0x00F98000 | 0x00F9BFFF | 16 KB data Flash | 2 | available | available |
| 0x00F9C000 | 0x00F9FFFF | 16 KB data Flash | 2 | available | available |
| 0x00FA0000 | 0x00FA3FFF | 16 KB data Flash | 3 | available | available |
| 0x00FA4000 | 0x00FA7FFF | 16 KB data Flash | 3 | available | available |
| 0x00FA8000 | 0x00FABFFF | 16 KB data Flash | 3 | available | available |
| 0x00FAC000 | 0x00FAFFFF | 16 KB data Flash | 3 | available | available |
| 0x00FB0000 | 0x00FB7FFF | 32 KB data Flash | 2 | not available | available |
| 0x00FB8000 | 0x00FBFFFF | 32 KB data flash | 3 | not available | available |

**Table 4. MPC5748G Family Comparison - RAM Memory Map**

| Start Address | End Address | Allocated size [KB] | MPC5747C | MPC5748C<br>MPC5746G<br>MPC5747G<br>MPC5748G |
|---|---|---|---|---|
| 0x40000000 | 0x40001FFF | 8 | available | available |
| 0x40002000 | 0x4000FFFF | 56 | available | available |
| 0x40010000 | 0x4001FFFF | 64 | available | available |
| 0x40020000 | 0x4003FFFF | 128 | available | available |
| 0x40040000 | 0x4007FFFF | 256 | available | available |
| 0x40080000 | 0x400BFFFF | 256 | not available | available |

# 3 Ordering parts

## 3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

## 4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

**NOTE**

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

**Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)**

| Symbol | Parameter | Conditions[1] | Min[2] | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_A}$<br>$V_{DD\_HV\_B}$<br>$V_{DD\_HV\_C}$ | HV IO supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_FLA}$[3] | HV flash supply voltage | — | 3.15 | 3.6 | V |
| $V_{DD\_HV\_ADC1\_REF}$ | HV ADC1 high reference voltage | — | 3.0 | 5.5 | V |
| $V_{DD\_HV\_ADC0}$<br>$V_{DD\_HV\_ADC1}$ | HV ADC supply voltage | — | max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05 | 3.6 | V |
| $V_{SS\_HV\_ADC0}$<br>$V_{SS\_HV\_ADC1}$ | HV ADC supply ground | — | -0.1 | 0.1 | V |
| $V_{DD\_LV}$[4] | Core supply voltage | — | 1.2 | 1.32 | V |
| $V_{IN1\_CMP\_REF}$[5, 6] | Analog Comparator DAC reference voltage | — | 3.15 | 3.6 | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition | — | -3.0 | 3.0 | mA |

*Table continues on the next page...*

## Table 9. Voltage monitor electrical characteristics (continued)

| Symbol | Parameter | State | Conditions | Configuration | | | Threshold | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Power Up [1] | Mask Opt | Reset Type | Min | Typ | Max | V |
| $V_{HVD\_LV\_cold}$ | LV supply high voltage monitoring, detecting at the device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.325 | 1.345 | 1.375 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.345 | 1.365 | 1.395 | V |
| $V_{LVD\_LV\_PD2\_hot}$ | LV supply low voltage monitoring, detecting in the PD2 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.125 | 1.143 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.145 | 1.163 | 1.180 | V |
| $V_{LVD\_LV\_PD1\_hot}$ | LV supply low voltage monitoring, detecting in the PD1 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.114 | 1.137 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.134 | 1.157 | 1.180 | V |
| $V_{LVD\_LV\_PD0\_hot}$ | LV supply low voltage monitoring, detecting in the PD0 core (hot) area | Fall | Untrimmed | Yes | No | Powerup | 1.080 | 1.120 | 1.160 | V |
| | | | Trimmed | | | | 1.114 | 1.137 | 1.160 | V |
| | | Rise | Untrimmed | | | | 1.100 | 1.140 | 1.180 | V |
| | | | Trimmed | | | | 1.134 | 1.157 | 1.180 | V |
| $V_{POR\_HV}$ | HV supply power on reset detector | Fall | Untrimmed | Yes | No | Powerup | 2.700 | 2.850 | 3.000 | V |
| | | Rise | Untrimmed | | | | 2.750 | 2.900 | 3.050 | V |
| $V_{LVD\_IO\_A\_LO}$, [2] | HV IO_A supply low voltage monitoring - low range | Fall | Untrimmed | Yes | No | Powerup | 2.750 | 2.923 | 3.095 | V |
| | | | Trimmed | | | | 2.978 | 3.039 | 3.100 | V |
| | | Rise | Untrimmed | | | | 2.780 | 2.953 | 3.125 | V |
| | | | Trimmed | | | | 3.008 | 3.069 | 3.130 | V |
| $V_{LVD\_IO\_A\_HI}$ [2] | HV IO_A supply low voltage monitoring - high range | Fall | Trimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | | | | | 4.060 | 4.151 | 4.240 | V |
| | | Rise | Trimmed | | | | Disabled at Start | | | |
| | | | | | | | 4.115 | 4.201 | 4.3 | V |
| $V_{LVD\_LV\_PD2\_cold}$ | LV supply low voltage monitoring, detecting at the device pin | Fall | Untrimmed | No | Yes | Functional | Disabled at Start | | | |
| | | | Trimmed | | | | 1.14 | 1.158 | 1.175 | V |
| | | Rise | Untrimmed | | | | Disabled at Start | | | |
| | | | Trimmed | | | | 1.16 | 1.178 | 1.195 | V |

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

## 4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

**NOTE**

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

**Table 10. Current consumption characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_FULL}$ 2, 3 | RUN Full Mode Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies<br>$T_a$ = 85°C<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 160MHz | — | 219 | 292 | mA |
| | | $T_a$ = 105°C | — | 230 | 328 | mA |
| | | $T_a$ = 125 °C | — | 249 | 400 | mA |
| $I_{DD\_GWY}$ 5, 6 | RUN Gateway Mode Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies<br>$T_a$ = 85°C<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 160MHz | — | 183 | 260 | mA |
| | | $T_a$ = 105°C | — | 196 | 294 | mA |
| | | $T_a$ = 125°C[4] | — | 215 | 348 | mA |
| $I_{DD\_BODY\_1}$ 7, 8 | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies<br>$T_a$ = 85 °C<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 120MHz | — | 149 | 223 | mA |
| | | $T_a$ = 105 °C | — | 158 | 270 | mA |
| | | $T_a$ = 125°C [4] | — | 175 | 310 | mA |
| IDD_BODY_2[9, 10] | RUN Body Mode Profile Operating current | LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies<br>$T_a$ = 85 °C<br>$V_{DD\_LV}$ = 1.25 V<br>VDD_HV_A = 5.5V<br>SYS_CLK = 80MHz | — | 105 | 174 | mA |

*Table continues on the next page...*

**Table 12. STANDBY Current consumption characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| STANDBY0 | STANDBY with 8K RAM | $T_a$ = 25 °C | — | 71 | — | µA |
| | | $T_a$ = 85 °C | — | 175 | 800 | |
| | | $T_a$ = 105 °C | — | 338 | 1725 | |
| | | $T_a$ = 125 °C | — | 750 | 2775 | |
| STANDBY1 | STANDBY with 64K RAM | $T_a$ = 25 °C | — | 72 | — | µA |
| | | $T_a$ = 85 °C | — | 176 | 815 | |
| | | $T_a$ = 105 °C | — | 350 | 1775 | |
| | | $T_a$ = 125 °C | — | 825 | 3000 | |
| STANDBY2 | STANDBY with 128K RAM | $T_a$ = 25 °C | — | 75 | — | µA |
| | | $T_a$ = 85 °C | — | 182 | 830 | |
| | | $T_a$ = 105 °C | — | 366 | 1825 | |
| | | $T_a$ = 125 °C | — | 900 | 3250 | |
| STANDBY3 | STANDBY with 256K RAM | $T_a$ = 25 °C | — | 80 | — | µA |
| | | $T_a$ = 85 °C | — | 197 | 860 | |
| | | $T_a$ = 105 °C | — | 400 | 1875 | |
| | | $T_a$ = 125 °C | — | 975 | 3500 | |
| STANDBY3 | FIRC ON | $T_a$ = 25 °C | — | 500 | — | µA |

1. The content of the Conditions column identifies the components that draw the specific current.

## 4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**NOTE**

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 13. ESD ratings**

| Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C | H1C | 2000 | V |

*Table continues on the next page...*

3. Slew rate control modes
4. Input slope = 2ns

**NOTE**

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

**NOTE**

The specification given above is measured between 20% / 80%.

## 5.2 DC electrical specifications @ 3.3V Range

**Table 15. DC electrical specifications @ 3.3V Range**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| VDD | LV (core) Supply Voltage | 1.08 | 1.32 | V |
| VDD_HV_x[1] | I/O Supply Voltage | 3.15 | 3.63 | V |
| Vih (pad_i_hv) | pad_i_hv Input Buffer High Voltage | 0.72*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil (pad_i_hv) | pad_i_hv Input Buffer Low Voltage | VSS_LV - 0.3 | 0.45*VDD_HV_x | V |
| Vhys (pad_i_hv) | pad_i_hv Input Buffer Hysteresis | 0.11*VDD_HV_x | | V |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.67*VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | VSS_LV - 0.3 | 0.35*VDD_HV_x | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.57 * VDD_HV_x | VDD_HV_x + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | VSS_LV - 0.3 | 0.4 * VDD_HV_x | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.09 * VDD_HV_x | | V |
| Pull_IIH (pad_i_hv) | Weak Pullup Current Low | 15 | | µA |
| Pull_IIH (pad_i_hv) | Weak Pullup Current High | | 55 | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[3] Low | 28 | | µA |
| Pull_IIL (pad_i_hv) | Weak Pulldown Current[2] High | | 85 | µA |
| Pull_Ioh | Weak Pullup Current[4] | 15 | 50 | µA |
| Pull_Iol | Weak Pulldown Current[5] | 15 | 50 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[6] | 0.8 *VDD_HV_x | — | V |
| Vol | Output Low Voltage[7] | — | 0.2 *VDD_HV_x | V |

*Table continues on the next page...*

**Table 15. DC electrical specifications @ 3.3V Range (continued)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| | Output Low Voltage[8] | | 0.1 *VDD_HV_x | |
| Ioh_f | Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10) | 10.5 | 60 | mA |

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

## 5.3 AC specifications @ 5 V Range

**Table 16. Functional Pad AC Specifications @ 5 V Range**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns) | | Drive Load (pF) | SIUL2_MSCRn[SRC 1:0] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | | 4.5/4.5 | | 1.3/1.2 | 25 | 11 |
| | | 6/6 | | 2.5/2 | 50 | |
| | | 13/13 | | 9/9 | 200 | |
| | | 5.25/5.25 | | 3/2 | 25 | 10 |
| | | 9/8 | | 5/4 | 50 | |
| | | 22/22 | | 18/16 | 200 | |
| | | 27/27 | | 13/13 | 50 | 01[2] |
| | | 40/40 | | 24/24 | 200 | |
| | | 40/40 | | 24/24 | 50 | 00[2] |
| | | 65/65 | | 40/40 | 200 | |
| pad_i_hv/ pad_sr_hv (input) | | 1.5/1.5 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

## 5.6 PORST electrical specifications

**Table 19. PORST electrical specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $W_{FPORST}$ | $\overline{PORST}$ input filtered pulse | — | — | 200 | ns |
| $W_{NFPORST}$ | $\overline{PORST}$ input not filtered pulse | 1000 | — | — | ns |
| $V_{IH}$ | Input high level | — | 0.65 x $V_{DD\_HV\_A}$ | — | V |
| $V_{IL}$ | Input low level | — | 0.35 x $V_{DD\_HV\_A}$ | — | V |

# 6 Peripheral operating requirements and behaviours

## 6.1 Analog

### 6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

## Table 20. ADC conversion characteristics (for 12-bit) (continued)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{AD}$[6] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity (precise channel) | — | –2 | — | 2 | LSB |
| INL | Integral non-linearity (standard channel) | — | –3 | — | 3 | LSB |
| DNL | Differential non-linearity | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –6 | — | 6 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |
| ADC Analog Pad (pad going to one ADC) | Max leakage (precision channel) | 150 °C | — | — | 250 | nA |
| | Max leakage (standard channel) | 150 °C | — | — | 2500 | nA |
| | Max leakage (standard channel) | 105 °C $_{TA}$ | — | 5 | 250 | nA |
| | Max positive/negative injection | | –5 | — | 5 | mA |
| $TUE_{precision\ channels}$ | Total unadjusted error for precision channels | Without current injection | –6 | +/-4 | 6 | LSB |
| | | With current injection | | +/-5 | | LSB |
| $TUE_{standard/extended\ channels}$ | Total unadjusted error for standard/ extended channels | Without current injection | –8 | +/-6 | 8 | LSB |
| | | With current injection[7] | | +/-8 | | LSB |
| $t_{recovery}$ | STOP mode to Run mode recovery time | | | | < 1 | µs |

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 2.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

## Table 21. ADC conversion characteristics (for 10-bit)

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.) | — | 15.2 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz@ 100 ohm source impedance | 275 | — | — | ns |

*Table continues on the next page...*

## 6.1.2 Analog Comparator (CMP) electrical specifications

### Table 22. Comparator and 6-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DDHS}$ | Supply current, High-speed mode (EN=1, PMODE=1) | — | — | 250 | µA |
| $I_{DDLS}$ | Supply current, low-speed mode (EN=1, PMODE=0) | — | 5 | 11 | µA |
| $V_{AIN}$ | Analog input voltage | $V_{SS}$ | — | $V_{IN1\_CMP\_REF}$ | V |
| $V_{AIO}$ | Analog input offset voltage [1] | -42 | — | 42 | mV |
| $V_H$ | Analog comparator hysteresis [2] | — | 1 | 25 | mV |
| | • CR0[HYSTCTR] = 00 | — | 20 | 50 | mV |
| | • CR0[HYSTCTR] = 01 | — | 40 | 70 | mV |
| | • CR0[HYSTCTR] = 10 | — | 60 | 105 | mV |
| | • CR0[HYSTCTR] = 11 | | | | |
| $t_{DHS}$ | Propagation Delay, High Speed Mode (Full Swing) [1, 3] | — | — | 250 | ns |
| $t_{DLS}$ | Propagation Delay, Low power Mode (Full Swing) [1, 3] | — | 5 | 21 | µs |
| | Analog comparator initialization delay, High speed mode[4] | — | 4 | | µs |
| | Analog comparator initialization delay, Low speed mode [4] | — | 100 | | µs |
| $I_{DAC6b}$ | 6-bit DAC current adder (when enabled) | | | | |
| | 3.3V Reference Voltage | — | 6 | 9 | µA |
| | 5V Reference Voltage | — | 10 | 16 | µA |
| INL | 6-bit DAC integral non-linearity | –0.5 | — | 0.5 | LSB[5] |
| DNL | 6-bit DAC differential non-linearity | –0.8 | — | 0.8 | LSB |

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

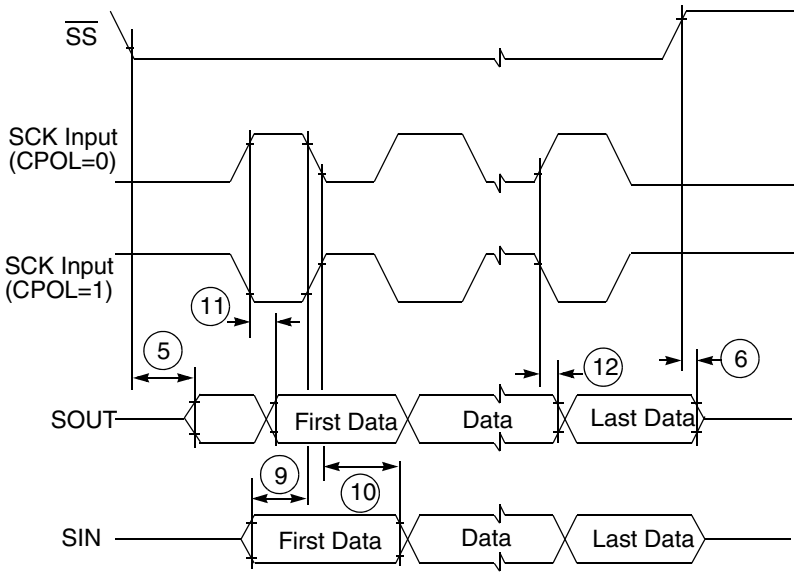



**Figure 11. DSPI classic SPI timing — slave, CPHA = 1**

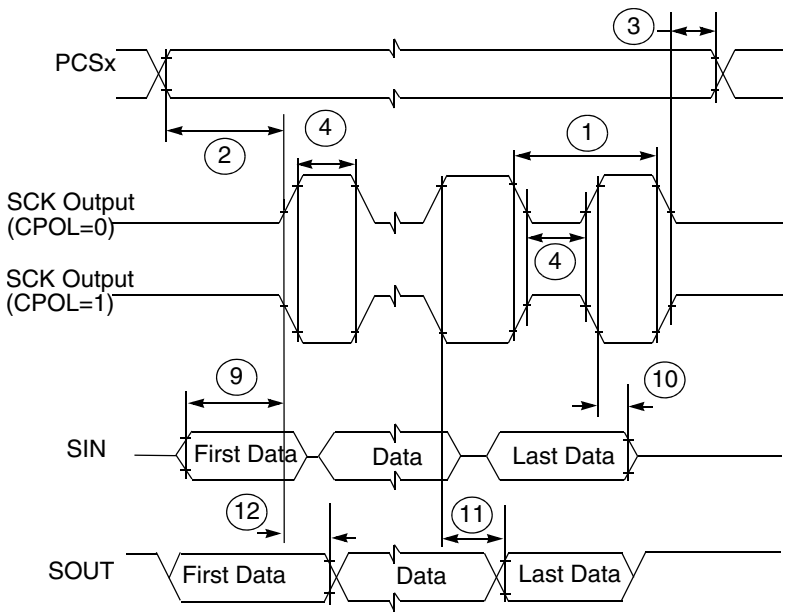



**Figure 12. DSPI modified transfer format timing — master, CPHA = 0**

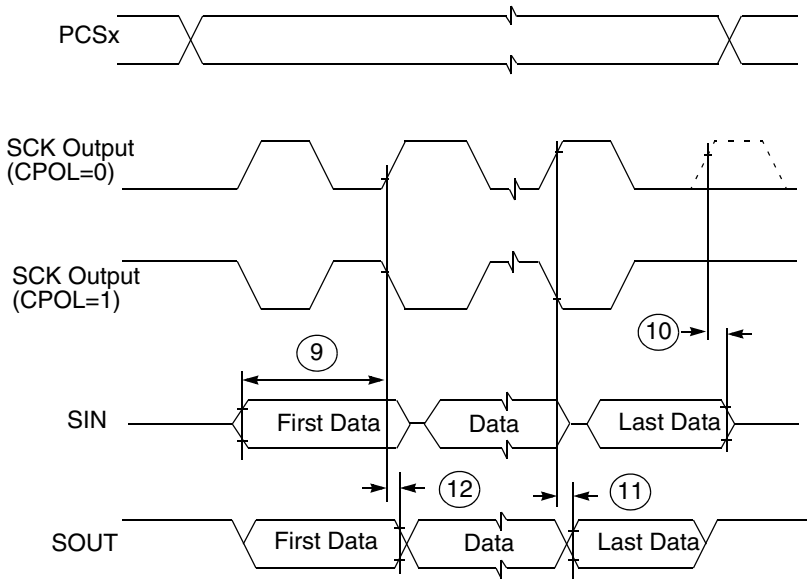



**Figure 13. DSPI modified transfer format timing — master, CPHA = 1**

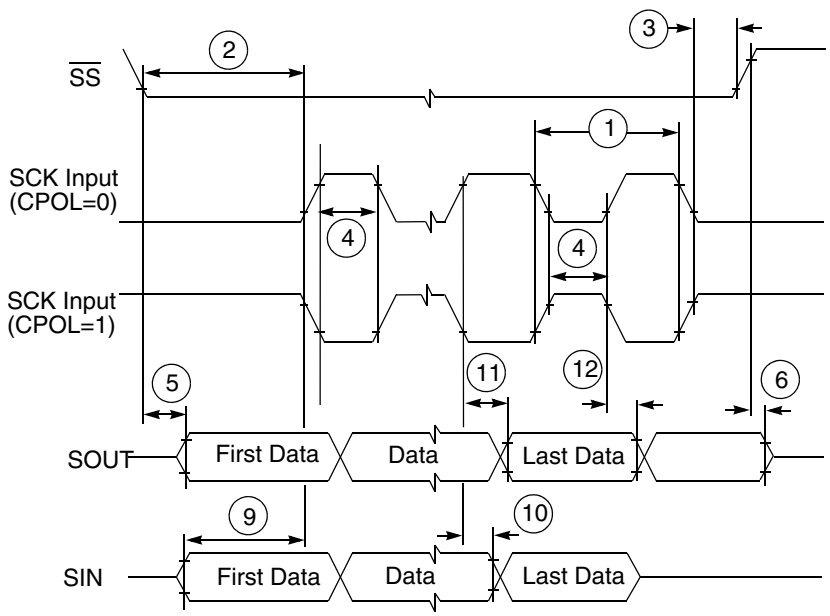



**Figure 14. DSPI modified transfer format timing – slave, CPHA = 0**

### 6.4.2.2 TxEN

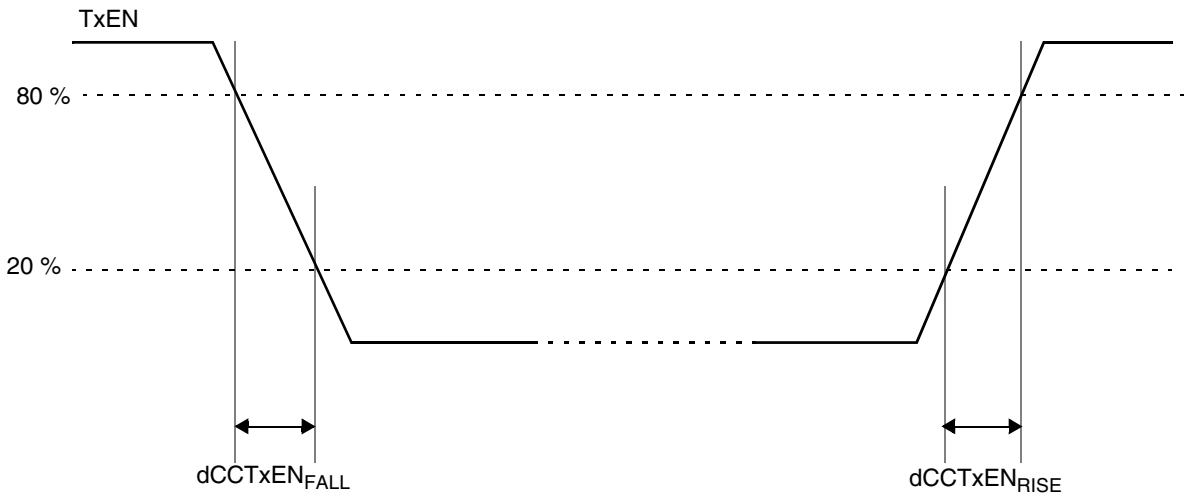



**Figure 17. TxEN signal**

**Table 38. TxEN output characteristics[1]**

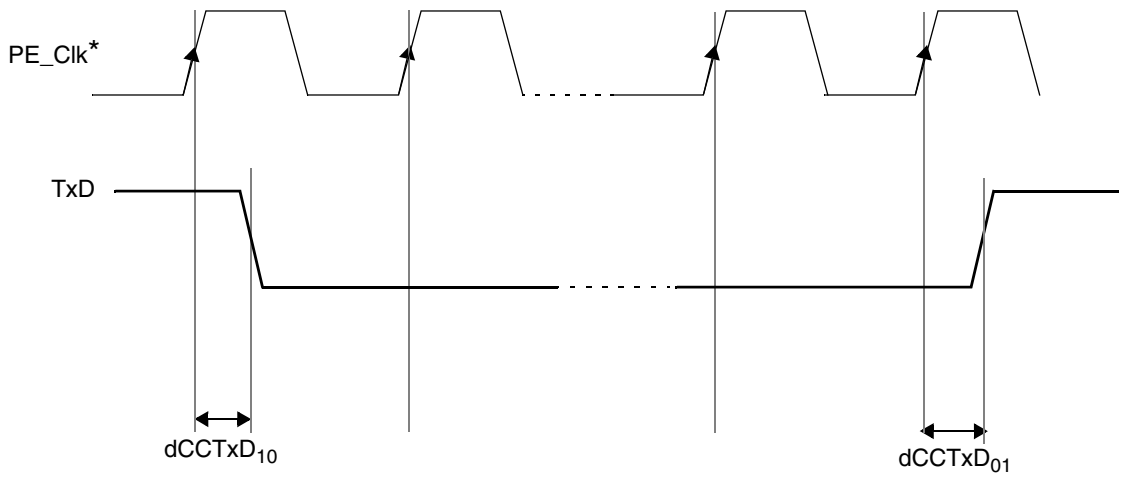
| Name | Description | Min | Max | Unit |
|---|---|---|---|---|
| $dCCTxEN_{RISE25}$ | Rise time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{FALL25}$ | Fall time of TxEN signal at CC | — | 9 | ns |
| $dCCTxEN_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxEN_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

**Table 39. TxD output characteristics (continued)**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| $dCCTxD_{01}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge | — | 25 | ns |
| $dCCTxD_{10}$ | Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge | — | 25 | ns |

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.




*FlexRay Protocol Engine Clock

**Figure 20. TxD Signal propagation delays**

## 6.4.2.4 RxD

**Table 40. RxD input characteristic**

| Name | Description[1] | Min | Max | Unit |
|---|---|---|---|---|
| C_CCRxD | Input capacitance on RxD pin | — | 7 | pF |
| uCCLogic_1 | Threshold for detecting logic high | 35 | 70 | % |
| uCCLogic_0 | Threshold for detecting logic low | 30 | 65 | % |
| $dCCRxD_{01}$ | Sum of delay from actual input to the D input of the first FF, rising edge | — | 10 | ns |
| $dCCRxD_{10}$ | Sum of delay from actual input to the D input of the first FF, falling edge | — | 10 | ns |

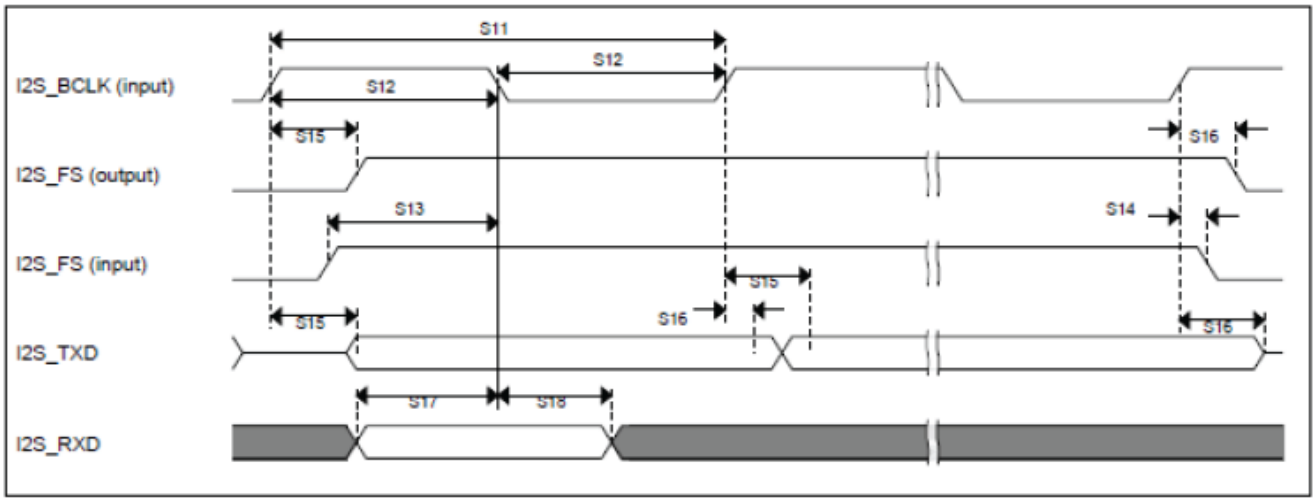



**Figure 27. Slave mode SAI Timing**

# 6.5 Debug specifications

## 6.5.1 JTAG interface timing

### Table 50. JTAG pin AC electrical characteristics [1]

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{JCYC}$ | TCK Cycle Time [2] | 62.5 | — | ns |
| 2 | $t_{JDC}$ | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK Rise and Fall Times (40% - 70%) | — | 3 | ns |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | TMS, TDI Data Setup Time | 5 | — | ns |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | TMS, TDI Data Hold Time | 5 | — | ns |
| 6 | $t_{TDOV}$ | TCK Low to TDO Data Valid | — | 20[3] | ns |
| 7 | $t_{TDOI}$ | TCK Low to TDO Data Invalid | 0 | — | ns |
| 8 | $t_{TDOHZ}$ | TCK Low to TDO High Impedance | — | 15 | ns |
| 11 | $t_{BSDV}$ | TCK Falling Edge to Output Valid | — | 600[4] | ns |
| 12 | $t_{BSDVZ}$ | TCK Falling Edge to Output Valid out of High Impedance | — | 600 | ns |
| 13 | $t_{BSDHZ}$ | TCK Falling Edge to Output High Impedance | — | 600 | ns |
| 14 | $t_{BSDST}$ | Boundary Scan Input Valid to TCK Rising Edge | 15 | — | ns |
| 15 | $t_{BSDHT}$ | TCK Rising Edge to Boundary Scan Input Invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

**Thermal attributes**

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|---|---|---|---|---|---|
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top | 0.2 | °C/W | 7 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

| Board type | Symbol | Description | 324 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 25.5 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 19.0 | °C/W | 1,23 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 18.1 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 14.8 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 10.4 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 8.4 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top natural convection) | 0.45 | °C/W | 6 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package top natural convection) | 2.65 | °C/W | 7 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

| Board type | Symbol | Description | 256 MAPBGA | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 39.5 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 22.9 | °C/W | 1,23 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 28.5 | °C/W | 1,3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./min. air speed) | 18.3 | °C/W | 1,3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 9.5 | °C/W | 4 |
| — | $R_{\theta JC}$ | Thermal resistance, junction to case | 5.8 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction to package top outside center (natural convection) | 0.2 | °C/W | 6 |
| — | $\Psi_{JB}$ | Thermal characterization parameter, junction to package bottom outside center (natural convection) | 6.4 | °C/W | 7 |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

# 8 Dimensions

## 8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

| Package | NXP Document Number |
|---|---|
| 176-pin LQFP-EP | 98ASA00673D |
| 256 MAPBGA | 98ASA00346D |
| 324 MAPBGA | 98ASA10582D |

## Table 56. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • Updated VIH min and VIL max values in Main oscillator electrical characteristics<br>• Replaced ipp_sre[1:0] by SIUL2_MSCRn[SRC 1:0] in AC specifications @ 3.3 V Range, DC electrical specifications @ 3.3V Range<br>• Functional reset sequence short, unsecure boot corrected Reset sequence duration<br>• Added NVM memory map and RAM memory map Family comparison<br>• Added BAF execution duration section BAF execution duration<br>• Supply names (VDD_LV, VSS_LV replace dvss, avss, dvdd, avdd) corrected in Jitter calculation table PLL electrical specifications<br>• Updated Ordering information: Fab and Mask version indicator<br>• Updated tpsus typical and max values Flash memory AC timing specifications<br>• Added Notes on IBIS models use in AC specifications @3.3 V Range AC specifications @ 3.3 V Range<br>• Updated Vol value in DC electrical specifications @ 3.3V Range DC electrical specifications @ 3.3V Range<br>• Added Notes on IBIS models in Functional Pad AC Specifications @ 5 V Range AC specifications @ 5 V Range<br>• Updated Vol values in DC electrical specifications @5V Range DC electrical specifications @ 5 V Range<br>• Updated IDD Current values Supply current characteristics<br>• Updated STANDBY current consumption with FIRC ON Supply current characteristics<br>• Thermal numbers update for 256MAPBGA Thermal attributes<br>• POR_HV Trim values removed Voltage monitor electrical characteristics<br>• ADC analog pad leakage for 105 C added ADC electrical specifications<br>• IDD STANDBY0, 1, 2 and 3 added Supply current characteristics |
| Rev5 | July 31 2017 | • Updated Standby2 value to 125 C in Standby current consumption characteristics<br>• Corrected typo in Note from "case" to "cause" Voltage regulator electrical characteristics<br>• Updated propagation delay from 14 to 21 in ACMP electrical specifications |