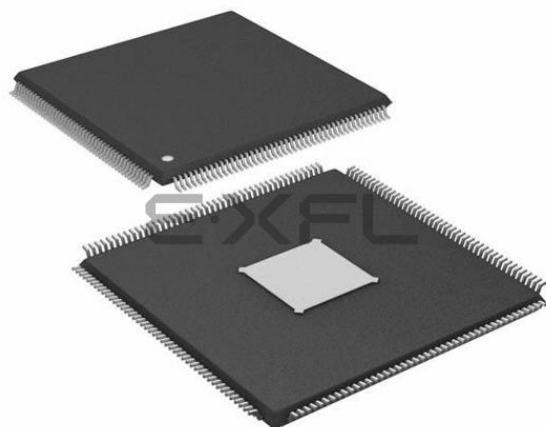




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Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747ck1mku6r

Table of Contents

1	Block diagram.....	4	6.3.5	Flash memory AC timing specifications.....	41
2	Family comparison.....	4	6.3.6	Flash read wait state and address pipeline control settings	42
3	Ordering parts.....	8	6.4	Communication interfaces.....	42
3.1	Determining valid orderable parts	8	6.4.1	DSPI timing.....	42
3.2	Ordering Information	9	6.4.2	FlexRay electrical specifications.....	48
4	General.....	9	6.4.2.1	FlexRay timing.....	48
4.1	Absolute maximum ratings.....	9	6.4.2.2	TxEN.....	49
4.2	Recommended operating conditions.....	11	6.4.2.3	TxD.....	50
4.3	Voltage regulator electrical characteristics.....	13	6.4.2.4	RxD.....	51
4.4	Voltage monitor electrical characteristics.....	16	6.4.3	uSDHC specifications.....	52
4.5	Supply current characteristics.....	18	6.4.4	Ethernet switching specifications.....	53
4.6	Electrostatic discharge (ESD) characteristics.....	21	6.4.5	MediaLB (MLB) electrical specifications.....	55
4.7	Electromagnetic Compatibility (EMC) specifications.....	22	6.4.5.1	MLB 3-pin interface DC characteristics.....	55
5	I/O parameters.....	22	6.4.5.2	MLB 3-pin interface electrical specifications.....	55
5.1	AC specifications @ 3.3 V Range.....	22	6.4.6	USB electrical specifications.....	57
5.2	DC electrical specifications @ 3.3V Range.....	23	6.4.6.1	USB electrical specifications.....	57
5.3	AC specifications @ 5 V Range.....	24	6.4.6.2	ULPI timing specifications.....	57
5.4	DC electrical specifications @ 5 V Range.....	25	6.4.7	SAI electrical specifications	58
5.5	Reset pad electrical characteristics.....	26	6.5	Debug specifications.....	60
5.6	PORST electrical specifications.....	28	6.5.1	JTAG interface timing	60
6	Peripheral operating requirements and behaviours.....	28	6.5.2	Nexus timing.....	62
6.1	Analog.....	28	6.5.3	WKPU/NMI timing.....	64
6.1.1	ADC electrical specifications.....	28	6.5.4	External interrupt timing (IRQ pin).....	65
6.1.2	Analog Comparator (CMP) electrical specifications	33	7	Thermal attributes.....	65
6.2	Clocks and PLL interfaces modules.....	34	7.1	Thermal attributes.....	65
6.2.1	Main oscillator electrical characteristics.....	34	8	Dimensions.....	67
6.2.2	32 kHz Oscillator electrical specifications	36	8.1	Obtaining package dimensions	67
6.2.3	16 MHz RC Oscillator electrical specifications.....	36	9	Pinouts.....	68
6.2.4	128 KHz Internal RC oscillator Electrical specifications	37	9.1	Package pinouts and signal descriptions.....	68
6.2.5	PLL electrical specifications	37	10	Reset sequence.....	68
6.3	Memory interfaces.....	38	10.1	Reset sequence duration.....	68
6.3.1	Flash memory program and erase specifications.....	38	10.2	BAF execution duration.....	68
6.3.2	Flash memory Array Integrity and Margin Read specifications.....	39	10.3	Reset sequence description.....	69
6.3.3	Flash memory module life specifications.....	40	11	Revision History.....	71
6.3.4	Data retention vs program/erase cycles.....	40			

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions (V_{DD_HV_x} = 3.3 V)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
V _{DD_HV_A} V _{DD_HV_B} V _{DD_HV_C}	HV IO supply voltage	—	3.15	3.6	V
V _{DD_HV_FL A} ³	HV flash supply voltage	—	3.15	3.6	V
V _{DD_HV_ADC1_REF}	HV ADC1 high reference voltage	—	3.0	5.5	V
V _{DD_HV_ADC0} V _{DD_HV_ADC1}	HV ADC supply voltage	—	max(V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}) - 0.05	3.6	V
V _{SS_HV_ADC0} V _{SS_HV_ADC1}	HV ADC supply ground	—	-0.1	0.1	V
V _{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
V _{IN1_CMP_REF} ^{5, 6}	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I _{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
 - Control of external NPN ballast transistor
 - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD_HV_IO_A}$ supply
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD_HV_IO_A}$ supply
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors¹ are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for I_{dd} , collector voltage, etc

1. BCP56, MCP68 and MJD31 are guaranteed ballasts.

Table 8. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{HV_VDD_A}$	VDD_HV_A supply capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{HV_VDD_B}$	VDD_HV_B supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{HV_VDD_C}$	VDD_HV_C supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
C_{HV_ADC0} C_{HV_ADC1}	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
C_{HV_ADR} ⁶	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	μF
$V_{DD_HV_BALLAST}$ ⁷	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C_BALLAST}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{C_BALLAST}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time after main supply stabilization	$C_{fp_reg} = 3 \mu F$	—	74	—	μs
t_{ramp}	Load current transient	I_{load} from 15% to 55% $C_{fp_reg} = 3 \mu F$		1.0		μs

- Split capacitance on each pair VDD_LV pin should sum up to a total value of C_{fp_reg}
- Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
- Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
- It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.
- For VDD_HV_A, VDD_HV_B, and VDD_HV_C, 1 μF on each side of the chip
 - 0.1 μF close to each VDD/VSS pin pair.
 - 10 μF near for each power supply source
 - For VDD_LV, 0.1 μF close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
 - For VDD_LV, 0.1 μF close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
- Only applicable to ADC1

7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If $V_{DD_HV_BALLAST}$ is supplied from the same source as $V_{DD_HV_A}$ this condition is implicitly met):
- During power-up, $V_{DD_HV_BALLAST}$ must have met the min spec of 2.25V before $V_{DD_HV_A}$ reaches the POR_HV_RISE min of 2.75V.
 - During power-down, $V_{DD_HV_BALLAST}$ must not drop below the min spec of 2.25V until $V_{DD_HV_A}$ is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for $V_{DD_HV_A}$ and the ballast collector, a bulk storage capacitor (as defined in [Table 8](#)) is required on $V_{DD_HV_A}$ close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the $V_{DD_HV_A}$ supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may cause the $V_{DD_HV_A}$ voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or $V_{DD_HV_A}$ pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on $V_{DD_HV_A}$ must be maintained within the specified operating range (see [Recommended operating conditions](#)) to prevent LVD events.

4.4 Voltage monitor electrical characteristics

Table 9. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up ¹	Mask Opt	Reset Type	Min	Typ	Max	
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Powerup	0.930	0.979	1.028	V
			Trimmed				0.959	0.979	0.999	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				1.009	1.029	1.049	V

Table continues on the next page...

Table 13. ESD ratings (continued)

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
		conforming to AEC-Q100-002			
V _{ESD(CDM)}	Electrostatic discharge (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry ²	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00 ³
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input) ⁴		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.

Table 15. DC electrical specifications @ 3.3V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
	Output Low Voltage ⁸		0.1 *VDD_HV_x	
loh_f	Full drive loh ⁹ (SIUL2_MSCRn[SRC 1:0]= 11)	18	70	mA
lol_f	Full drive lol ⁹ (SIUL2_MSCRn[SRC 1:0]= 11)	21	120	mA
loh_h	Half drive loh ⁹ (SIUL2_MSCRn[SRC 1:0]= 10)	9	35	mA
lol_h	Half drive lol ⁹ (SIUL2_MSCRn[SRC 1:0]= 10)	10.5	60	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. loh/lol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01 ²
		40/40		24/24	200	
		40/40		24/24	50	00 ²
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

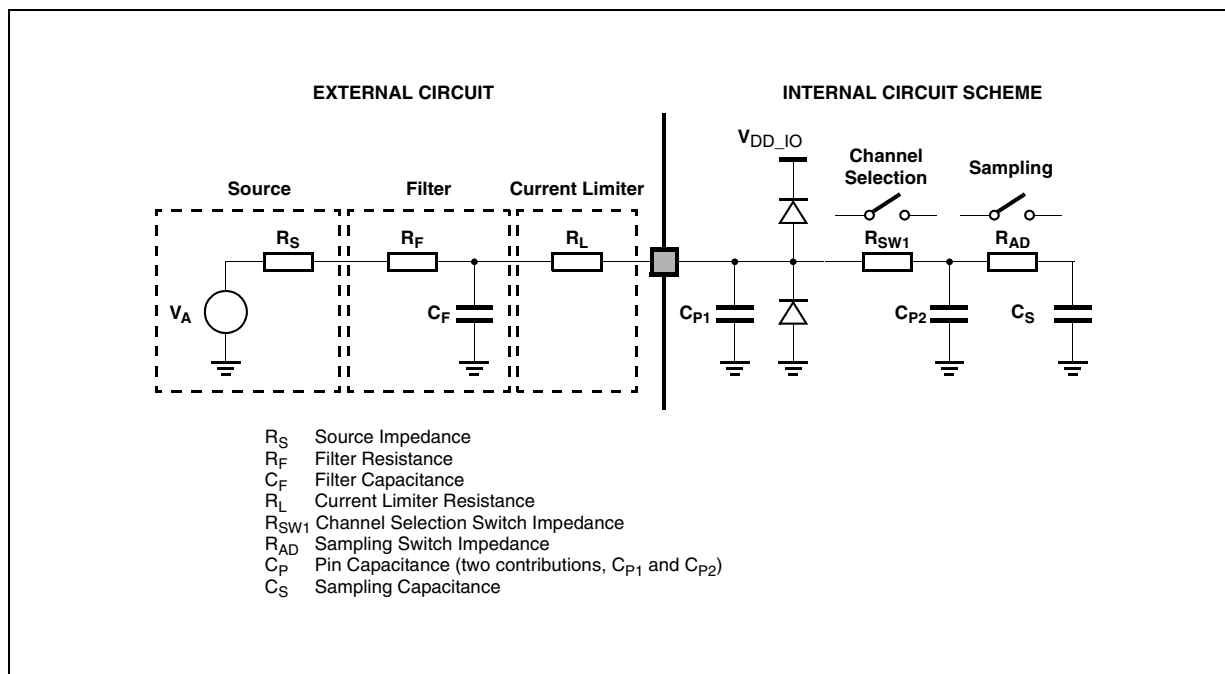


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time ⁴	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard and extended channels)	80 MHz	1.5 ⁵	—	—	μ s
	Total Conversion time $t_{sample} + t_{conv}$ (for precision channels)		1	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁶	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁶	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁶	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R_{AD}^6	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{\text{precision channels}}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection		+/-5		LSB
$TUE_{\text{standard/extended channels}}$	Total unadjusted error for standard/extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection ⁷		+/-8		LSB
t_{recovery}	STOP mode to Run mode recovery time				< 1	μs

- Active ADC input, $V_{inA} < [\min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]$. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions ($VDD_HV_x = 3.3\text{ V}$)' for required relation between IO_supply_A,B,C and ADC_Supply .
- The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
- Apart from t_{sample} and t_{conv} , few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- See Figure 2.
- Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK^2 frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{osc1} ¹	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	μA
		Clock stopped			200	nA

1. V_{dd}=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	μs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN} ¹	Jitter due to Fractional Mode (ps) J_{SDM} ²	Jitter due to Fractional Mode J_{SSCG} (ps) ³	1 Sigma Random Jitter J_{RJ} (ps) ⁴	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	$\pm(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ})$
Long Term Jitter (Integer Mode)				40	$\pm(N \times J_{RJ})$
Long Term jitter (Fractional Mode)				100	$\pm(N \times J_{RJ})$

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

Memory interfaces

2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See [Percentage of sample exceeding specified value of jitter table](#)

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30×10^{-3}
5	5.63×10^{-5}
6	2.00×10^{-7}
7	2.82×10^{-10}

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

[Table 30](#) shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic ¹	Typ ²	Factory Programming ^{3, 4}		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life ⁵	Lifetime Max ⁶		
			20°C ≤T _A ≤30°C	-40°C ≤T _J ≤150°C	-40°C ≤T _J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t _{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t _{ppgm}	Page (256 bits) program time	73	200	300	108	500		μs
t _{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t _{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t _{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms

Table continues on the next page...

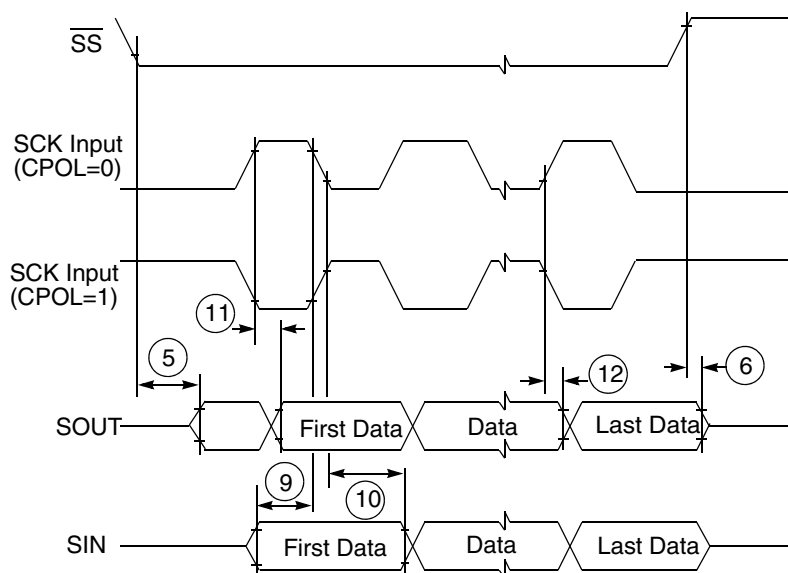


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

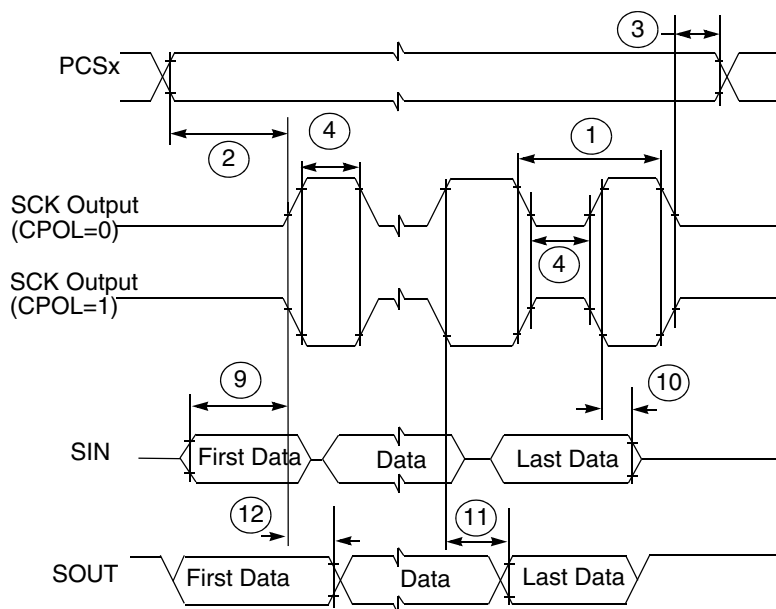


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

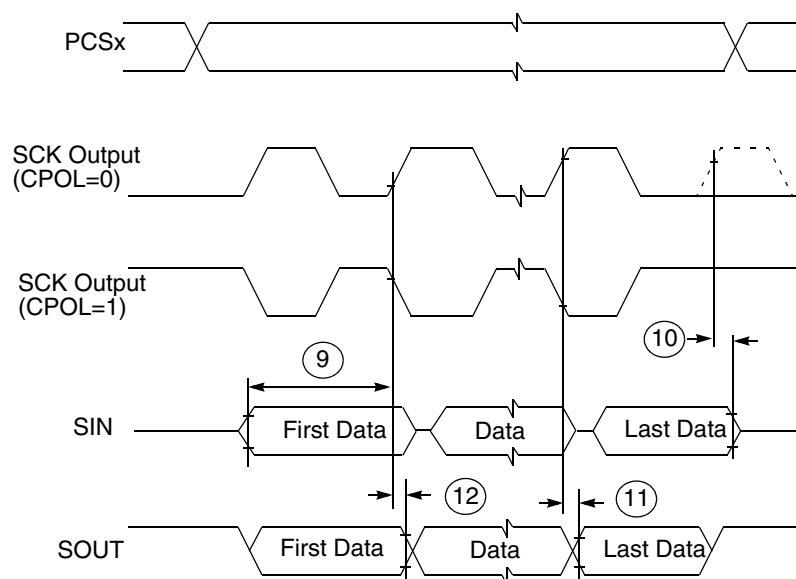


Figure 13. DSPI modified transfer format timing — master, CPHA = 1

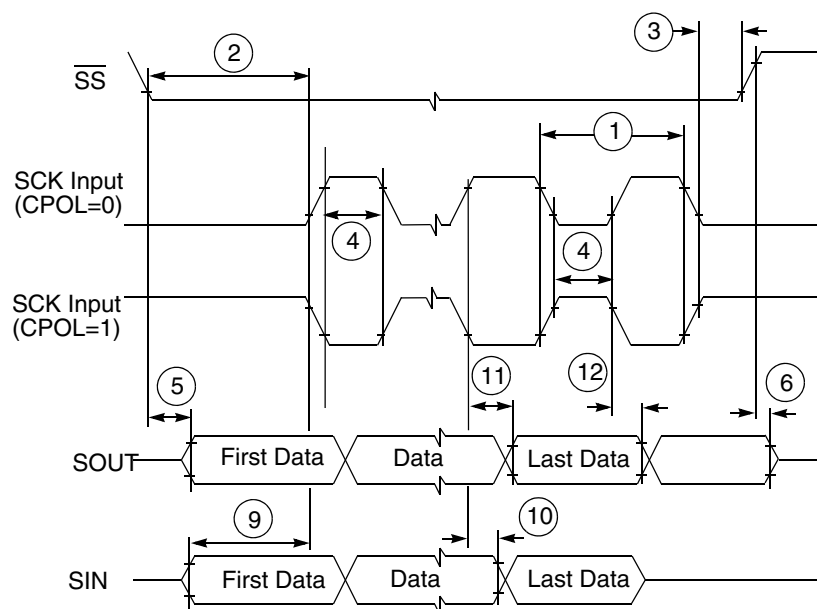


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

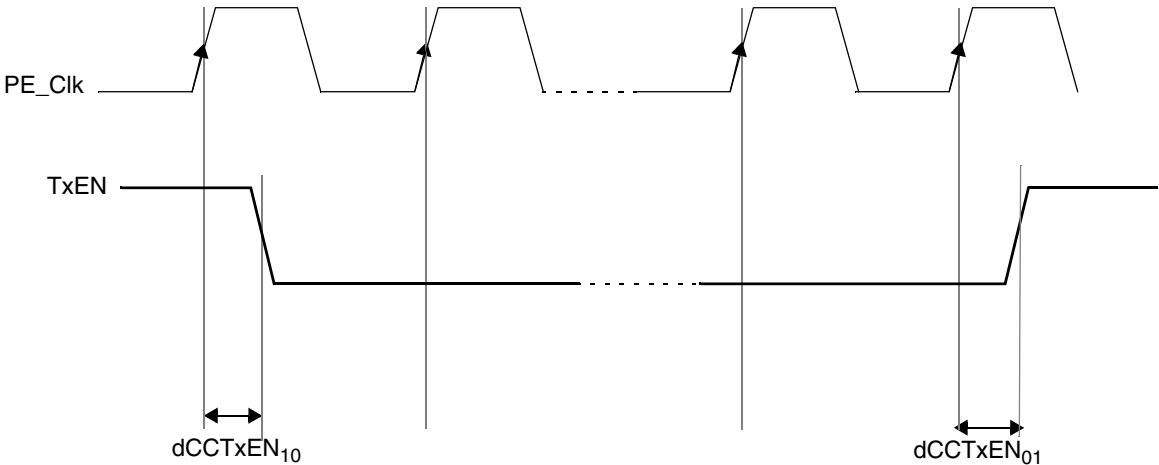


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

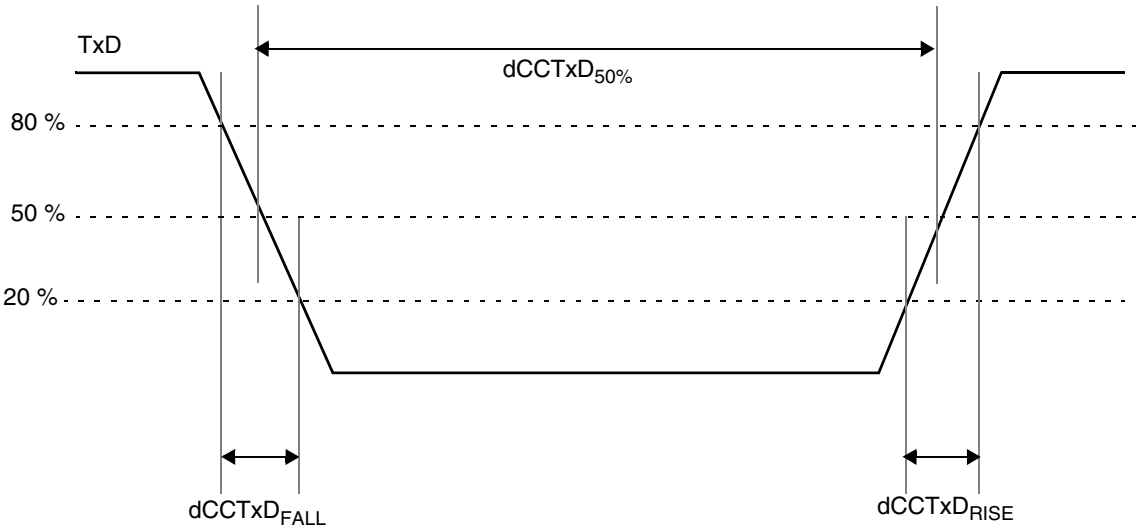


Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description ¹	Min	Max	Unit
dCCT _{xAsym}	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	-2.45	2.45	ns
dCCTxD _{RISE25} +dCCTxD _{FALL25}	Sum of Rise and Fall time of TxD signal at the output	—	9 ²	ns

Table continues on the next page...

1. All parameters specified for $VDD_HV_IOx = 3.3\text{ V} \pm 5\%$, $\pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$.

6.4.3 uSDHC specifications

Table 41. uSDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
Card input clock					
SD1	fpp	Clock frequency (Identification mode)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (SD\SDIO high speed)	0	40	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f _{OD}	Clock frequency (MMC full speed)	0	40	MHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	6.5	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

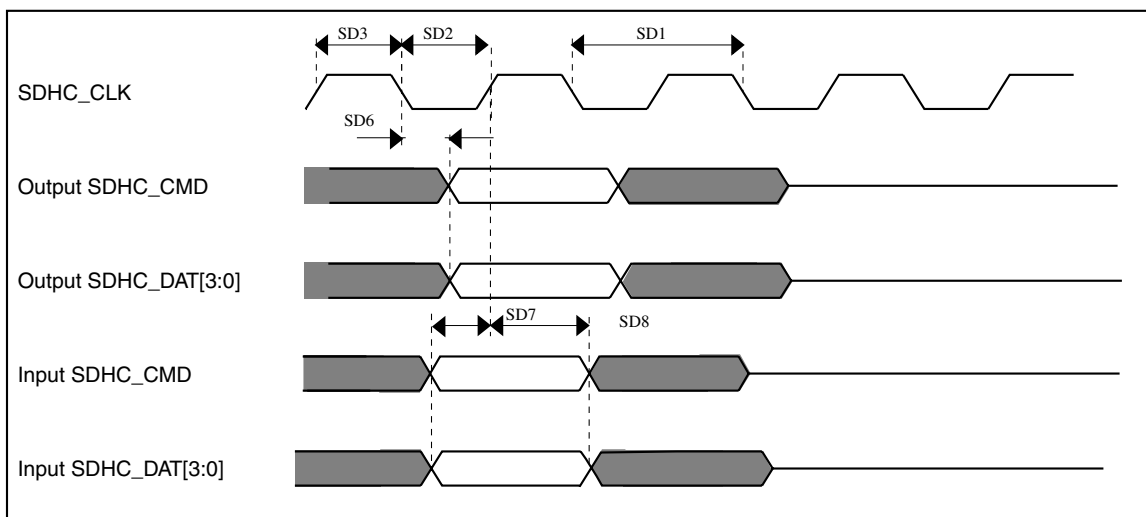


Figure 21. uSDHC timing

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMII. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

MediaLB (MLB) electrical specifications

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 45. MLB 3-Pin 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}		3	ns	V_{IL} to V_{IH}
MLBCLK fall time	t_{mckf}		3	ns	V_{IH} to V_{IL}
MLBCLK low time ¹	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	$t_{mcf dz}$	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	$t_{mcf dz}$	0	t_{mckl}	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	4	—	ns	2

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 46. MLB 3-Pin 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency ¹	f_{mck}	45.056 -	- 51.2	MHz MHz	1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz
MLBCLK rise time	f_{mckr}		1	ns	V_{IL} to V_{IH}
MLBCLK fall time	f_{mckf}		1	ns	V_{IH} to V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	2
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	$t_{mcf dz}$	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	$t_{mcf dz}$	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	3

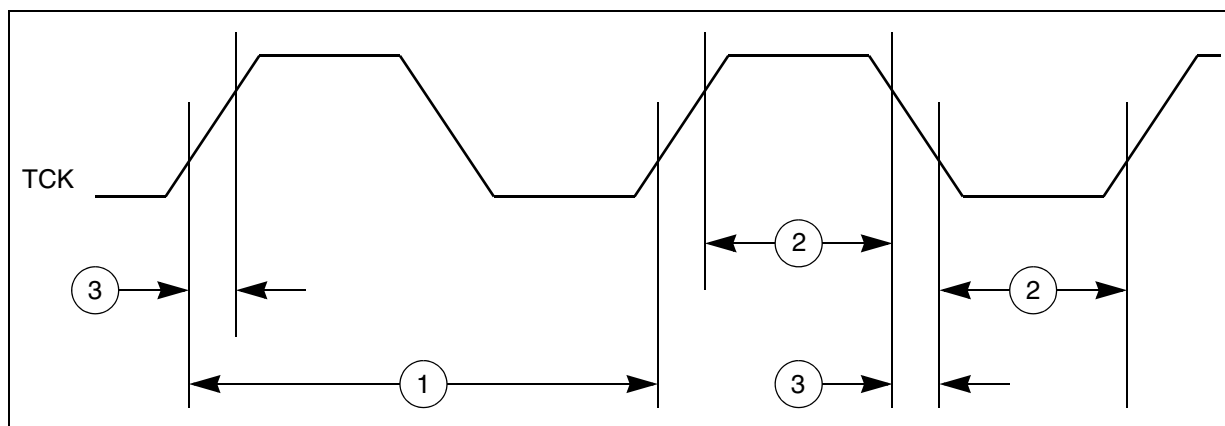


Figure 28. JTAG test clock input timing

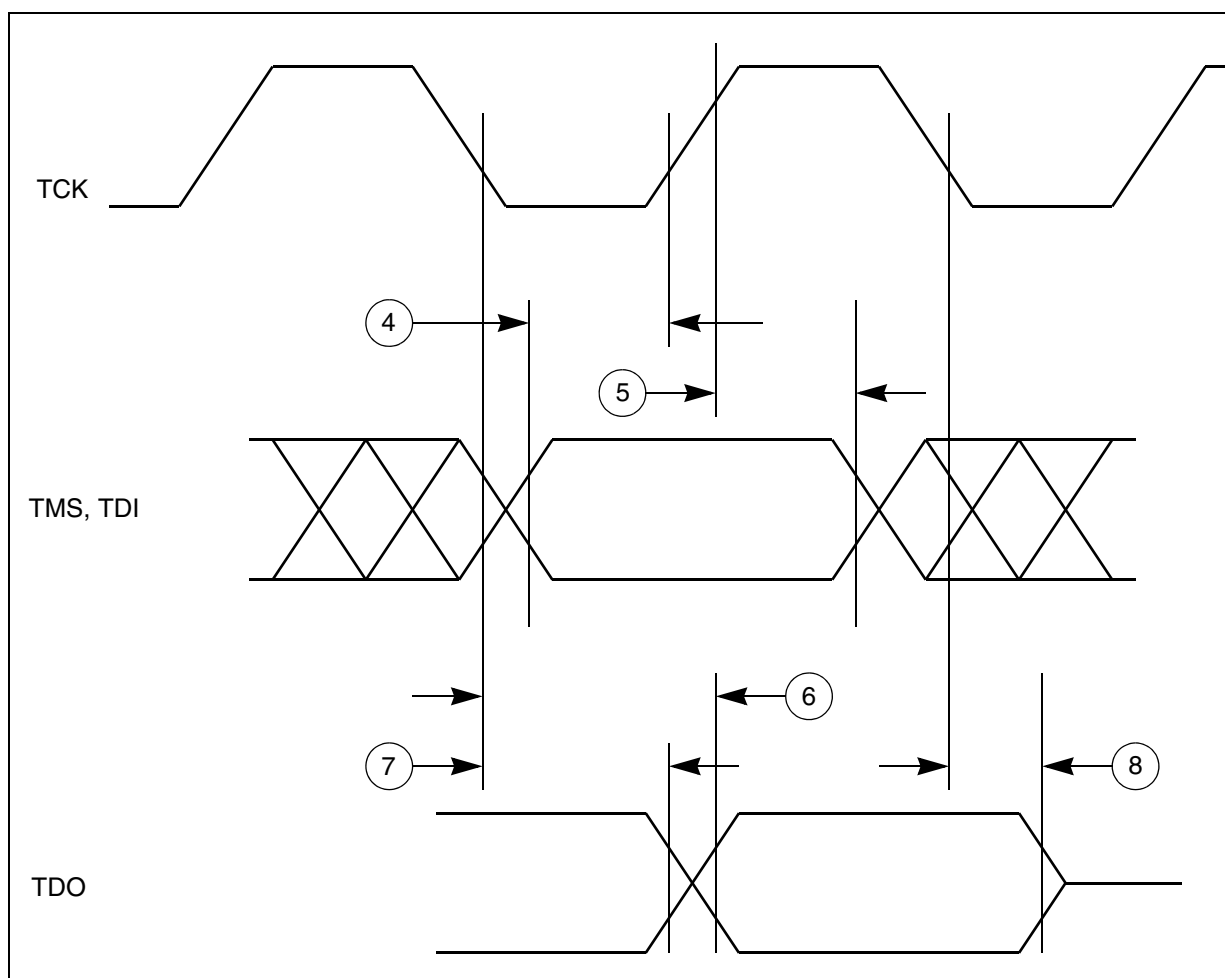


Figure 29. JTAG test access port timing

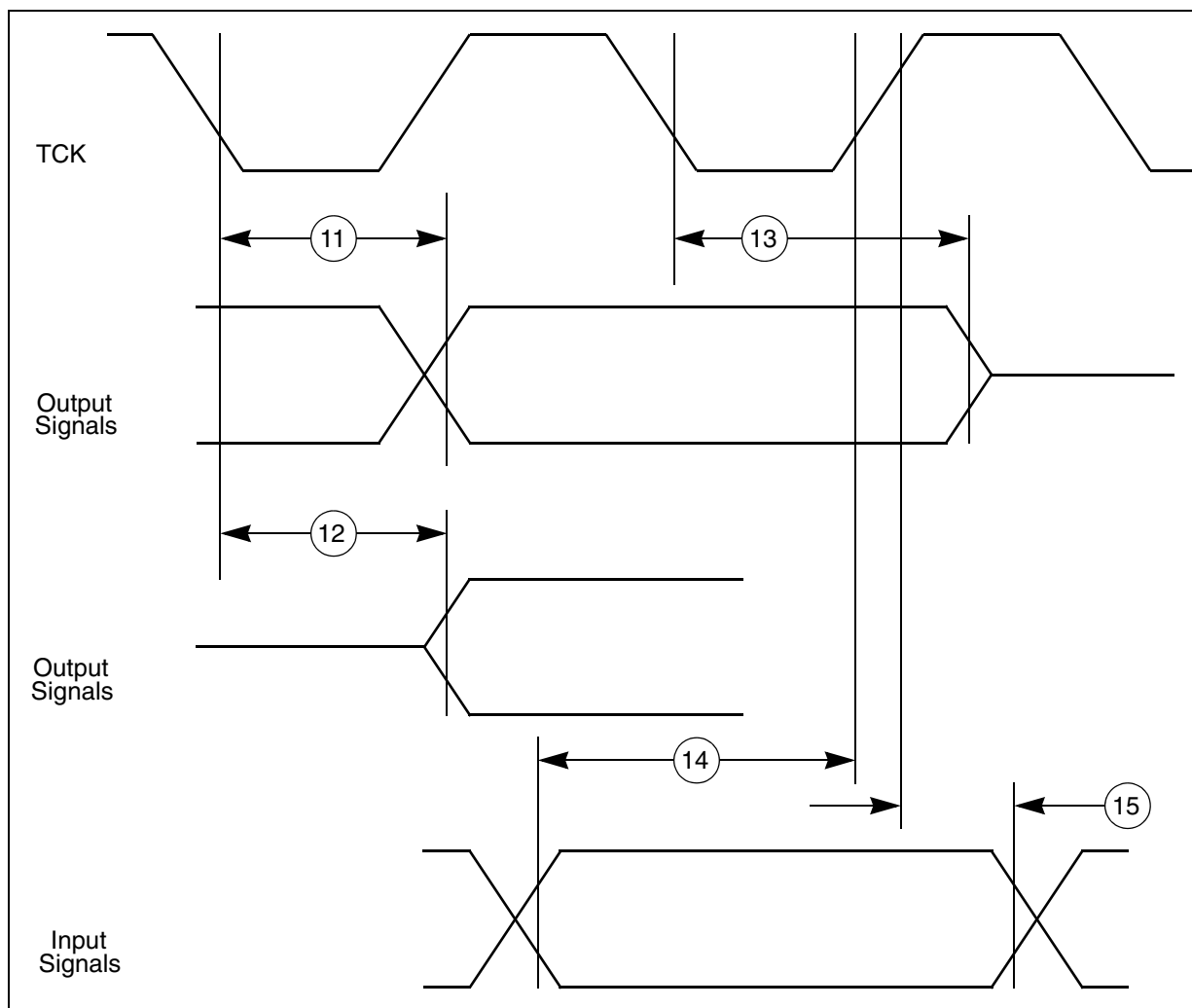


Figure 30. JTAG boundary scan timing

6.5.2 Nexus timing

Table 51. Nexus debug port timing ¹

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, MSEO, EVTO Data Valid ²	—	-0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	EVTI Pulse Width	—	4	—	t_{TCYC}
5	t_{EVTOPW}	EVTO Pulse Width	—	1	—	t_{MCYC}
6	t_{TCYC}	TCK Cycle Time ³	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS} , t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

[Table 54](#) specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in [Reset sequence description](#).

Table 54. RESET sequences

No.	Symbol	Parameter	T _{Reset}			Unit
			Min	Typ ¹	Max	
1	T _{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T _{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T _{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T _{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T _{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.