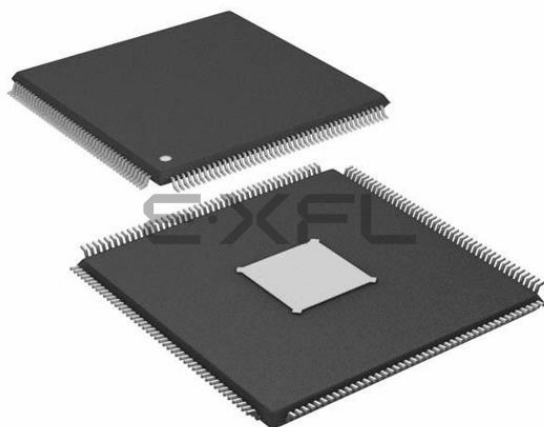




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747ck1vku6r

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison¹

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
CPUs	e200z4	e200z4	e200z4	e200z4	e200z4
	e200z2	e200z2	e200z4	e200z4	e200z4
			e200z2	e200z2	e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4
			e200z4	e200z4	e200z4
Maximum Operating Frequency ²	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)
	80MHz (z2)	80MHz (z2)	160MHz (z4)	160MHz (z4)	160MHz (z4)
			80MHz (z2)	80MHz (z2)	80MHz (z2)
Flash memory	4 MB	6 MB	3 MB	4 MB	6 MB
EEPROM support	32 KB to 128 KB emulated		32 KB to 192 KB emulated		
RAM	512 KB	768 KB			
ECC	End to End				
SMPU	24 entry		32 entry		
DMA	32 channels				
10-bit ADC	48 Standard channels 32 External channels				
12-bit ADC	16 Precision channels 16 Standard channels 32 External channels				
AnalogComparator	3				
BCTU	1				
SWT	2		4 ³		
STM	2		3		
PIT-RTI	16 channels PIT 1 channels RTI				
RTC/API	Yes				
Total Timer I/O ⁴	96 channels 16-bits				
LINFlexD	1 M/S, 15 M		1 M/S, 17 M		
FlexCAN	8 with optional CAN FD support				
DSPI/SPI	4 x DSPI				
	6 x SPI				

Table continues on the next page...

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_FULL} 2, 3	RUN Full Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	219	292	mA
		T _a = 105°C	—	230	328	mA
		T _a = 125 °C	—	249	400	mA
I _{DD_GWY} 5, 6	RUN Gateway Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	183	260	mA
		T _a = 105°C	—	196	294	mA
		T _a = 125°C ⁴	—	215	348	mA
I _{DD_BODY_1} 7, 8	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85 °C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	149	223	mA
		T _a = 105 °C	—	158	270	mA
		T _a = 125°C ⁴	—	175	310	mA
IDD_BODY_2 ^{9, 10}	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85 °C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	105	174	mA

Table continues on the next page...

General

- x FlexCAN state machines clocked (other FLEXCAN clock gated), 4 x LINFlexD transmitting (Other clock gated), 1x eMIOS clocked (used OPWFMB mode) (Others clock gated), FIRC, SIRC, FXOSC, SXOSC, PLL running, BCTU, DMAMUX, ACOMP clock gated. All others modules clock gated if not specifically mentioned. I/O supply current excluded
6. Recommended Transistors: MJD31 @ 85°C, 105°C and 125°C.
 7. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @ 120Mhz (Instruction and Data cache enabled), Platform @ 120MHz, SRAMs accessed in parallel, Flash access (prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT (ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting (others DSPIs clocked), 2 x SPI transmitting (others clocked), 4 x FlexCAN state machines working (others clocked), 9x LINFlexD transmitting (others clocked), 1x eMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC, CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
 8. Recommended Transistors: BCP56, BCP68 or MJD31 @ 85°C, BCP56, BCP68 or MJD31 @ 105°C and MJD31 @ 125°C.
 9. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @ 80Mhz (Instruction and Data cache enabled), Platform @ 80MHz, SRAMs accessed in parallel, Flash access (prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT (ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting (others DSPIs clocked), 2 x SPI transmitting (others clocked), 4 x FlexCAN state machines working (others clocked), 9x LINFlexD transmitting (others clocked), 1x eMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC, CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
 10. Recommended Transistors: BCP56, BCP68 or MJD31 @ 85°C, 105°C and 125°C
 11. Internal structures hold the input voltage less than $V_{DD_HV_ADC_REF} + 1.0$ V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
 12. This value is the total current for two ADCs. Each ADC might consume up to 2mA at max.

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM, but only one RAM being accessed	$T_a = 25^\circ\text{C}$ SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	8.9		mA
		$T_a = 25^\circ\text{C}$ SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON		10.2		
		$T_a = 85^\circ\text{C}$	—	12.5	22	
		$T_a = 105^\circ\text{C}$	—	14.5	24	
		$T_a = 125^\circ\text{C}$ ² SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	16	26	
LPU_STOP	with 256K RAM	$T_a = 25^\circ\text{C}$	—	0.535		mA
		$T_a = 85^\circ\text{C}$	—	0.72	6	
		$T_a = 105^\circ\text{C}$	—	1	8	
		$T_a = 125^\circ\text{C}$ ²	—	1.6	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming $T_a = T_j$, as the device is in static (fully clock gated) mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

Table 13. ESD ratings (continued)

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
		conforming to AEC-Q100-002			
V _{ESD(CDM)}	Electrostatic discharge (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry ²	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00 ³
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input) ⁴		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.

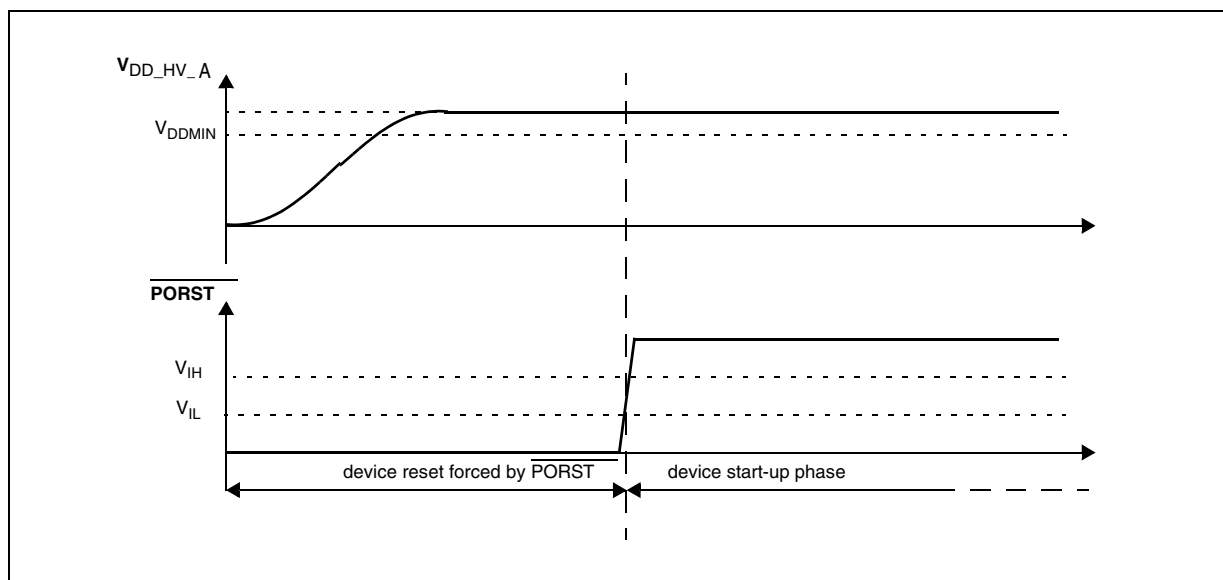
Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
loh_f	Full drive loh ⁹ (SIUL2_MSCRn[SRC 1:0]= 11)	38	132	mA
lol_f	Full drive lol ⁹ (SIUL2_MSCRn[SRC 1:0]= 11)	48	220	mA
loh_h	Half drive loh ⁹ (SIUL2_MSCRn[SRC 1:0]= 10)	19	66	mA
lol_h	Half drive lol ⁹ (SIUL2_MSCRn[SRC 1:0]= 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. loh/lol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

**Figure 3. Start-up reset requirements**

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$W_{F\text{PORST}}$	PORST input filtered pulse	—	—	200	ns
$W_{NF\text{PORST}}$	PORST input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	$0.65 \times V_{DD_HV_A}$	—	V
V_{IL}	Input low level	—	$0.35 \times V_{DD_HV_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

Table 35. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	-5	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11 ¹	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-5	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	4	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	4	—	16 ¹	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	-2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10 ¹	—	
			Master (MTFE = 1, CPHA = 1)	-2	—	-2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see [Table 35](#)

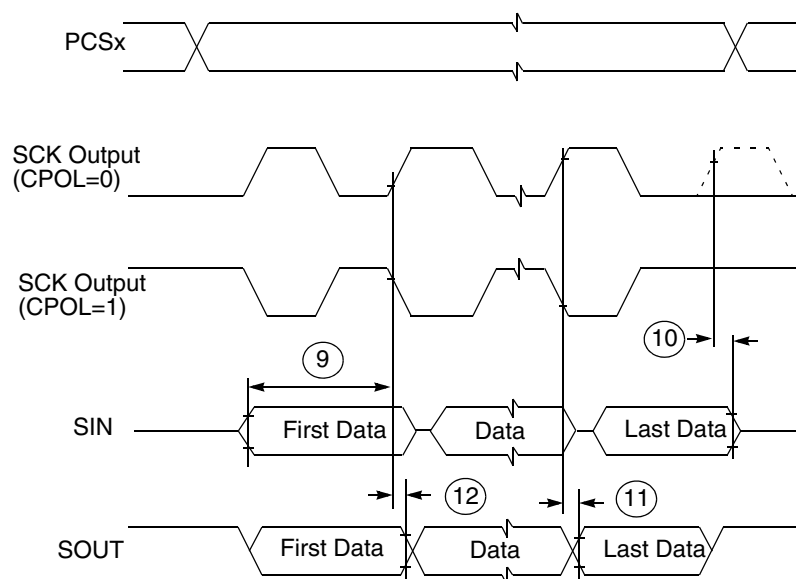


Figure 13. DSPI modified transfer format timing — master, CPHA = 1

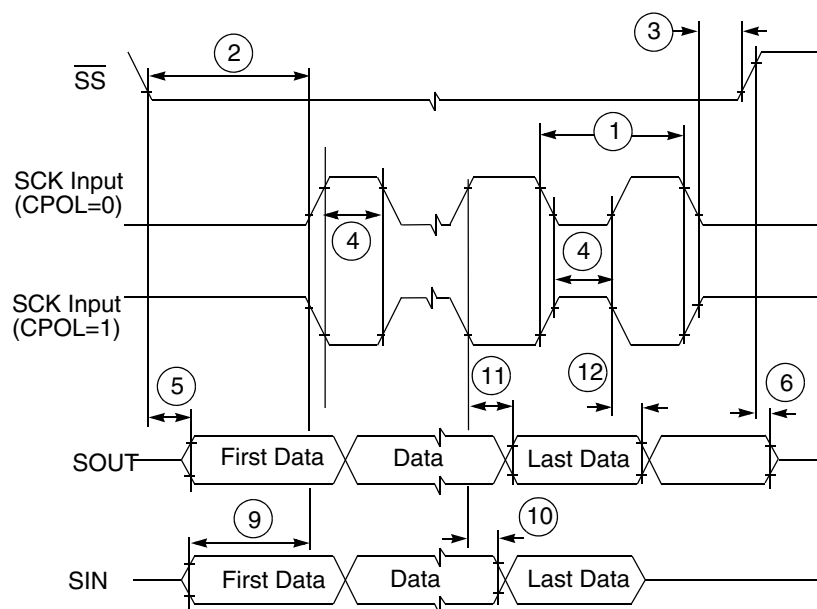


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

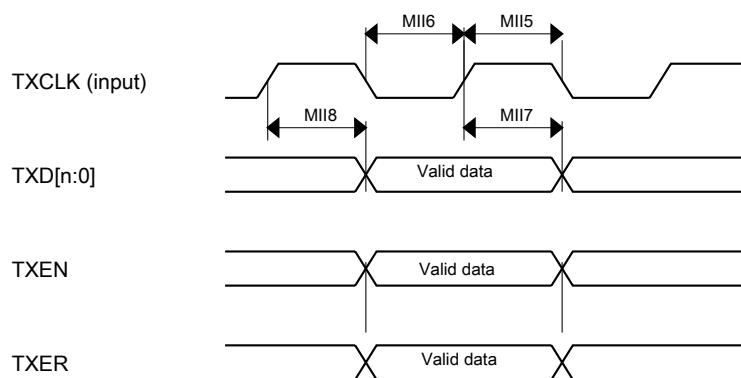


Figure 22. RMII/MII transmit signal timing diagram

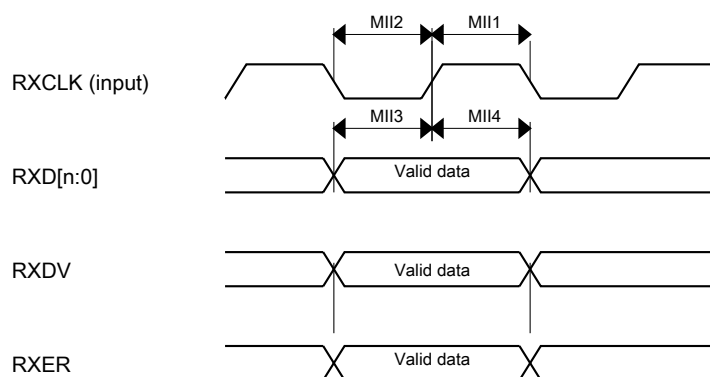


Figure 23. RMII/MII receive signal timing diagram

6.4.4.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 43. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

MediaLB (MLB) electrical specifications

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 45. MLB 3-Pin 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}		3	ns	V_{IL} to V_{IH}
MLBCLK fall time	t_{mckf}		3	ns	V_{IH} to V_{IL}
MLBCLK low time ¹	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	4	—	ns	2

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 46. MLB 3-Pin 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency ¹	f_{mck}	45.056 -	- 51.2	MHz MHz	1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz
MLBCLK rise time	f_{mckr}		1	ns	V_{IL} to V_{IH}
MLBCLK fall time	f_{mckf}		1	ns	V_{IH} to V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	2
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	3

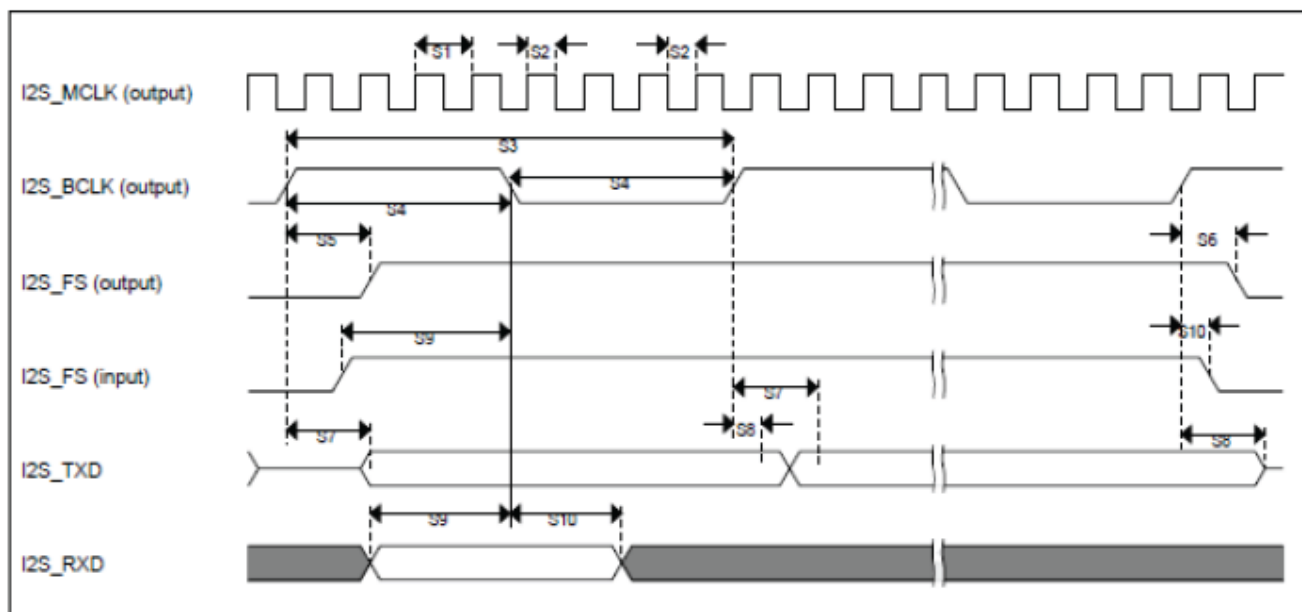


Figure 26. Master mode SAI Timing

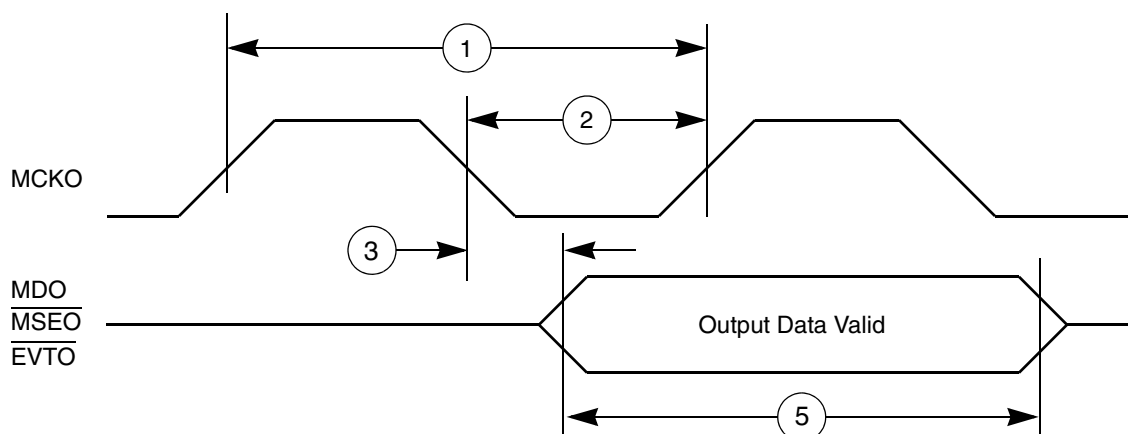
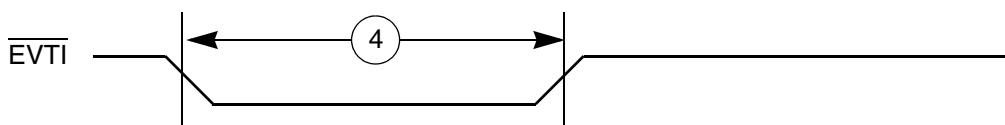
Table 49. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

Table 51. Nexus debug port timing ¹ (continued)

No.	Symbol	Parameter	Condition s	Min	Max	Unit
9	t_{NTDIH} , t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

**Figure 31. Nexus output timing****Figure 32. Nexus EVTI Input Pulse Width**

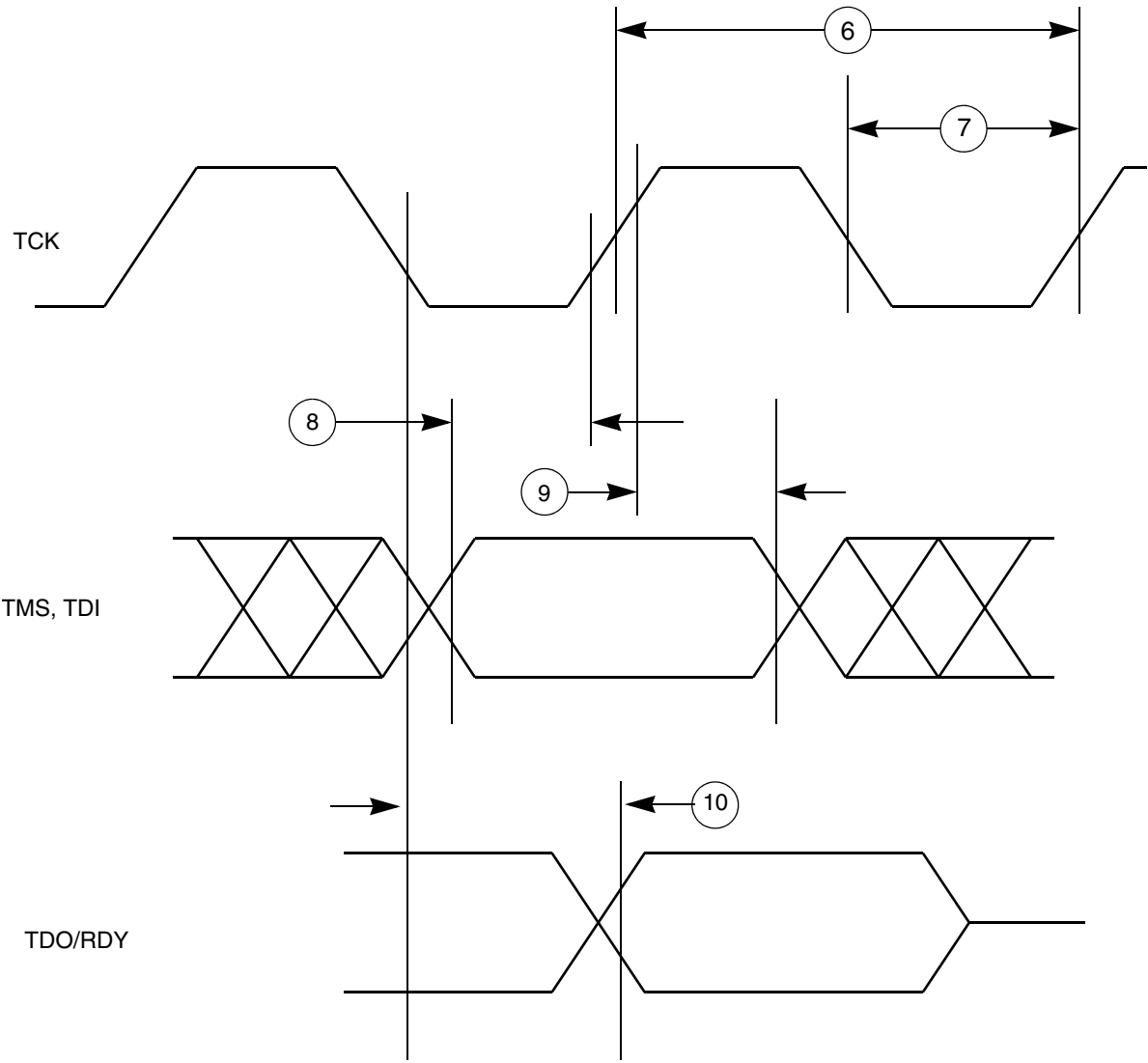


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	18.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Reset sequence

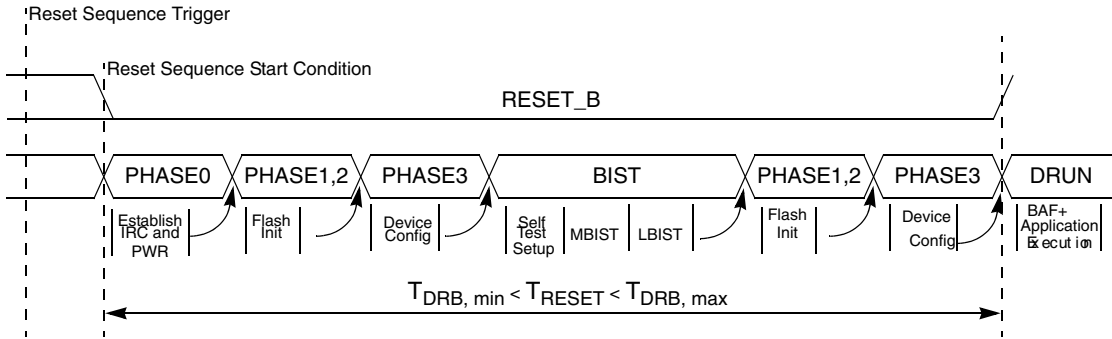


Figure 35. Destructive reset sequence, BIST enabled

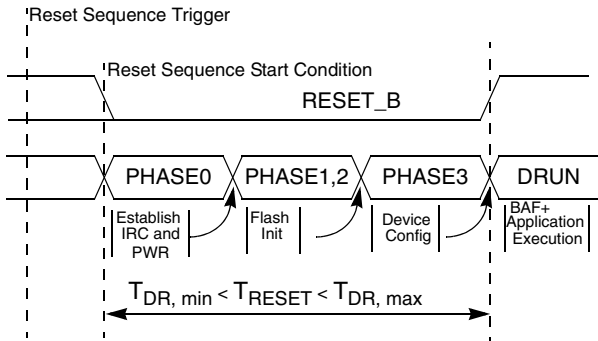


Figure 36. Destructive reset sequence, BIST disabled

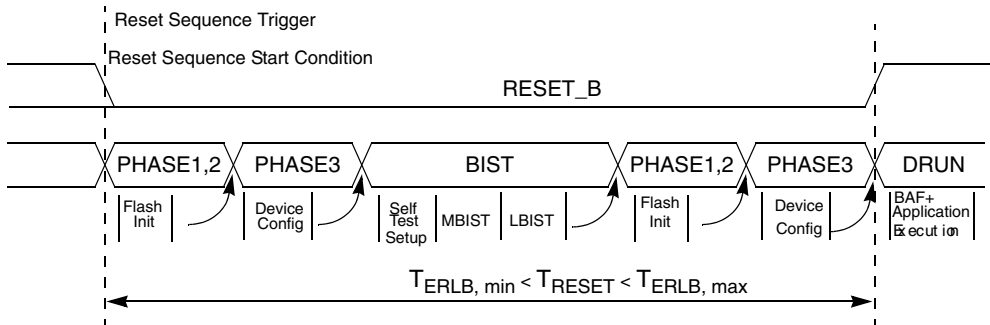


Figure 37. External reset sequence long, BIST enabled

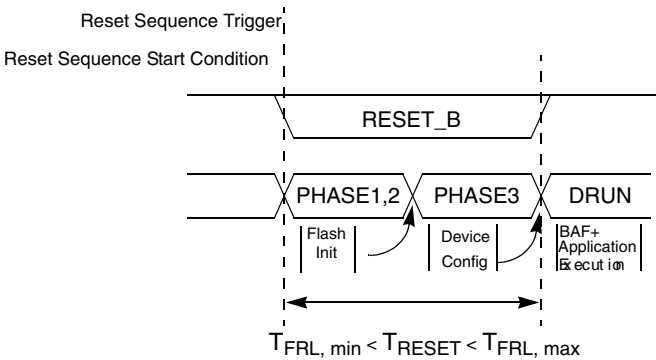


Figure 38. Functional reset sequence long

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Removed row for symbol 'V_{SS_LV}' - Removed footnote from 'Max' column of symbols 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}'
		- In section: Recommended operating conditions - In table: Recommended operating conditions (V_{DD_HV_x} = 5 V) - Added footnote to 'Conditions' column - Updated footnote for 'Min' column - Removed footnote from symbols 'V_{DD_HV_A}', 'V_{DD_HV_B}', and 'V_{DD_HV_C}' - Removed row for symbol: 'V_{SS_HV}' - Updated 'Parameter' column for symbol 'V_{DD_HV_ADC1_REF}' - Updated 'Min' column of symbol 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' - Updated 'Parameter', 'Min' 'Max' column for symbol 'V_{SS_HV_ADC0}' and 'V_{SS_HV_ADC1}' - Added footnote to symbol 'V_{DD_LV}' - Removed row for symbol 'V_{SS_LV}' - Added row for symbol 'V_{IN1_CMP_REF}' and corresponding footnotes to the symbol - In section: Voltage regulator electrical characteristics - In table: Voltage regulator electrical specifications - Added note to symbol 'Cbe_fpreg' - In section: Voltage monitor electrical characteristics - In table: Voltage monitor electrical characteristics - Updated column 'Parameter', 'Min' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{HVD_LV_cold}' and 'V_{LVD_IO_A_HI}' - Updated column 'Parameter', 'Min' and 'Typ' (of fall/rise trimmed condition) for symbol 'V_{LVD_LV_PD2_hot}', 'V_{LVD_LV_PD2_cold LV}' - Updated column 'Parameter' for symbol 'V_{LVD_LV_PD0_hot}' - Updated column 'Typ' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{LVD_FLASH}' - Updated footnote on symbol 'V_{LVD_IO_A_LO}' and 'V_{LVD_IO_A_HI}'
		- In section: Supply current characteristics - In table: Current consumption characteristics - Updated column 'Typ' for symbol 'I_{DD_FULL}' for temperature 85, 105, 125 - Updated column 'Typ' for symbol 'I_{DD_GWY}' for temperature 85, 105, 125 and column 'Max' for temperature 105 - Updated column 'Typ' for symbol 'I_{DD_BODY1}' for temperature 85, 105, 125 - Updated column 'Typ' for symbol 'I_{DD_BODY2}' for temperature 85, 105, 125 and 'Max' for temperature 125 - Added 'Typ' value for temperature 25 for symbol 'I_{DD_STOP}' - Updated column 'Typ' and 'Max' for symbol 'I_{DD_STOP}' for temperature 85, 105, 125 - In table: Low Power Unit (LPU) Current consumption characteristics - Updated column 'Typ' for symbol 'LPU_RUN' for temperature 25 and 125 - Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_RUN' - Updated column 'Typ' for symbol 'LPU_STOP' for temperature 25 and 125 - Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_STOP' - In table: STANDBY Current consumption characteristics - Updated to have one STANDBY - In section: I/O parameters

Table continues on the next page...

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