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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747ck1vmj6r

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

3.2 Ordering Information

Example Code	P	PC	57	4	8	G	S	K0	M	MJ	6	R
Qualification Status	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Power Architecture	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Automotive Platform	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Core Version	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Flash Size (core dependent)	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Product	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Optional fields	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Fab and mask indicator	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Temperature spec.	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Package Code	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
CPU Frequency	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
R = Tape & Reel (blank if Tray)												

Qualification Status P = Engineering samples S = Automotive qualified	Product Version C = Body Control Feature Set G = Gateway Feature Set	Package Code KU = 176 LQFP EP MJ = 256 MAPBGA MN = 324 MAPBGA
PC = Power Architecture Automotive Platform 57 = Power Architecture in 55nm	Optional fields Blank = Feature not available S = HSM (Security Module) F = CAN FD B = Both HSM and CAN FD T = HSM and 2nd Ethernet G = CAN FD and 2nd Ethernet H = HSM, CAN FD, and 2nd Ethernet	CPU Frequency 2 = Each z4 operates up to 120 MHz 6 = Each z4 operates up to 160 MHz
Core Version 4 = e200z4 Core Version (highest core version in the case of multiple cores)	Fab and mask version indicator K=TSMC Fab # = Version of maskset 0=0N65H 1=1N81M 0A=0N78S	Shipping Method R = Tape and reel Blank = Tray
Flash Memory Size 6 = 3 MB 7 = 4 MB 8 = 6 MB		Temperature spec. C = -40.C to +85.C Ta V = -40.C to +105.C Ta M = -40.C to +125.C Ta

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in [Table 5](#) for specific conditions

Table 6. Recommended operating conditions ($V_{DD_HV_x} = 3.3\text{ V}$) (continued)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3\text{ V}$
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
5. $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
6. This supply is shorted $V_{DD_HV_A}$ on lower packages.

NOTE

If $V_{DD_HV_A}$ is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. $V_{DD_HV_FLA}$ should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
$V_{DD_HV_A}$ $V_{DD_HV_B}$ $V_{DD_HV_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD_HV_FLA}$ ³	HV flash supply voltage	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	HV ADC supply voltage	—	$\max(V_{DD_H_V_A}, V_{DD_H_V_B}, V_{DD_H_V_C}) - 0.05$	5.5	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
$V_{IN1_CMP_REF}$ ⁵	Analog Comparator DAC reference voltage	—	3.15	5.5	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When V_{DD_HV} is in 5 V range, $V_{DD_HV_FLA}$ cannot be supplied externally. This pin is decoupled with C_{flash_reg} .
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. This supply is shorted $V_{DD_HV_A}$ on lower packages.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
I _{DD_FULL} 2, 3	RUN Full Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	219	292	mA
		T _a = 105°C	—	230	328	mA
		T _a = 125 °C	—	249	400	mA
I _{DD_GWY} 5, 6	RUN Gateway Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85°C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	183	260	mA
		T _a = 105°C	—	196	294	mA
		T _a = 125°C ⁴	—	215	348	mA
I _{DD_BODY_1} 7, 8	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85 °C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	149	223	mA
		T _a = 105 °C	—	158	270	mA
		T _a = 125°C ⁴	—	175	310	mA
IDD_BODY_2 ^{9, 10}	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T _a = 85 °C V _{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	105	174	mA

Table continues on the next page...

Table 13. ESD ratings (continued)

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
		conforming to AEC-Q100-002			
V _{ESD(CDM)}	Electrostatic discharge (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry ²	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00 ³
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input) ⁴		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.

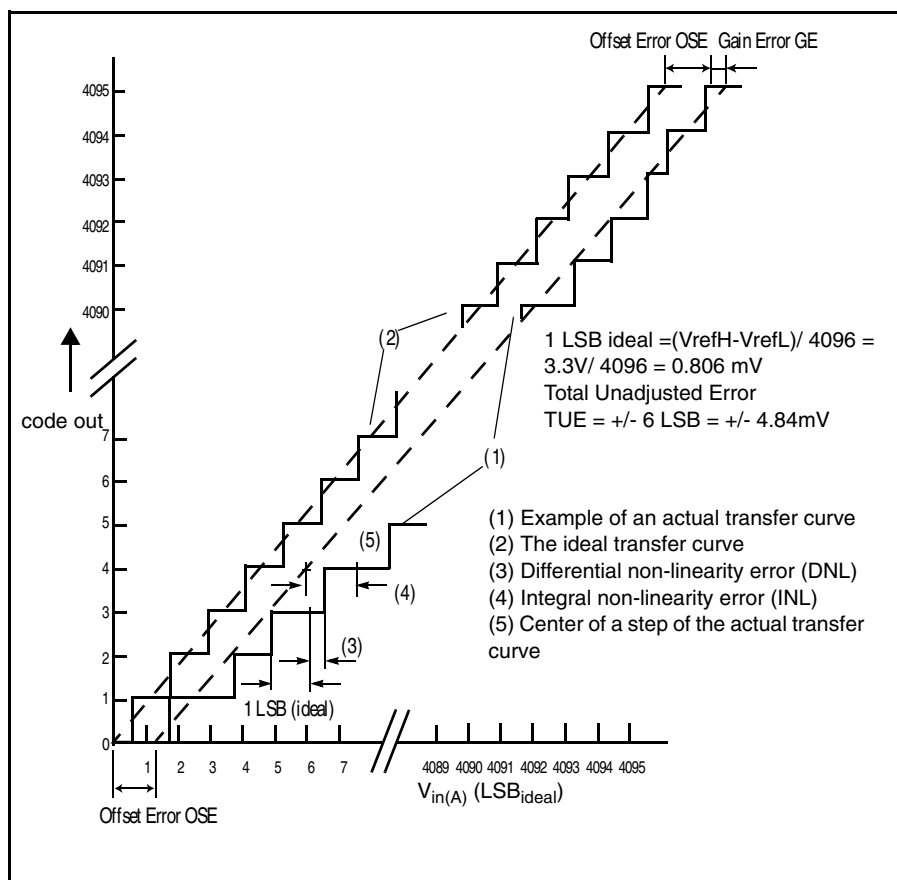


Figure 5. ADC characteristics and error definitions

Table 21. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
t_{conv}	Conversion time ⁴	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard channels)	80 MHz	1	—	—	μ s
	Total Conversion time $t_{sample} + t_{conv}$ (for extended channels)		1.5	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁵	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁵	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁵	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD} ⁵	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
	Max positive/negative injection	—	–5	—	5	mA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection ⁶	—	+/-4	—	LSB
$t_{recovery}$	STOP mode to Run mode recovery time	—	—	—	< 1	μ s

1. Active ADC Input, $V_{inA} < [\min(ADC_ADV, IO_Supply_A,B,C)]$. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A , B, C and ADC_Supply .
2. The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See [Figure 2](#)
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: 'Absolute maximum ratings') must be honored to meet TUE spec quoted here

NOTE

The ADC input pins sit across all three I/O segments, VDD_HV_A , VDD_HV_B and VDD_HV_C .

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	μA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage ¹	-42	—	42	mV
V_H	Analog comparator hysteresis ² <ul style="list-style-type: none"> CR0[HYSTCTR] = 00 CR0[HYSTCTR] = 01 CR0[HYSTCTR] = 10 CR0[HYSTCTR] = 11 	—	1	25	mV
		—	20	50	mV
		—	40	70	mV
		—	60	105	mV
		—	—	—	—
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1, 3}	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	—	5	21	μs
	Analog comparator initialization delay, High speed mode ⁴	—	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	—	100		μs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00

2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}-0.6\text{V}$

3. Full swing = V_{IH} , V_{IL}

4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

5. $1 \text{ LSB} = V_{\text{reference}}/64$

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{osc1} ¹	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	μA
		Clock stopped			200	nA

1. V_{dd}=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	μs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN} ¹	Jitter due to Fractional Mode (ps) J_{SDM} ²	Jitter due to Fractional Mode J_{SSCG} (ps) ³	1 Sigma Random Jitter J_{RJ} (ps) ⁴	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	$\pm(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ})$
Long Term Jitter (Integer Mode)				40	$\pm(N \times J_{RJ})$
Long Term jitter (Fractional Mode)				100	$\pm(N \times J_{RJ})$

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

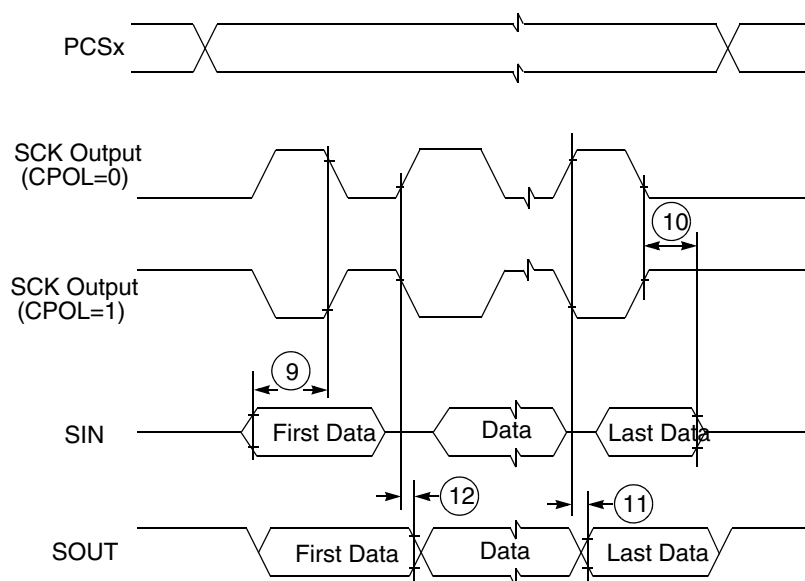


Figure 9. DSPI classic SPI timing — master, CPHA = 1

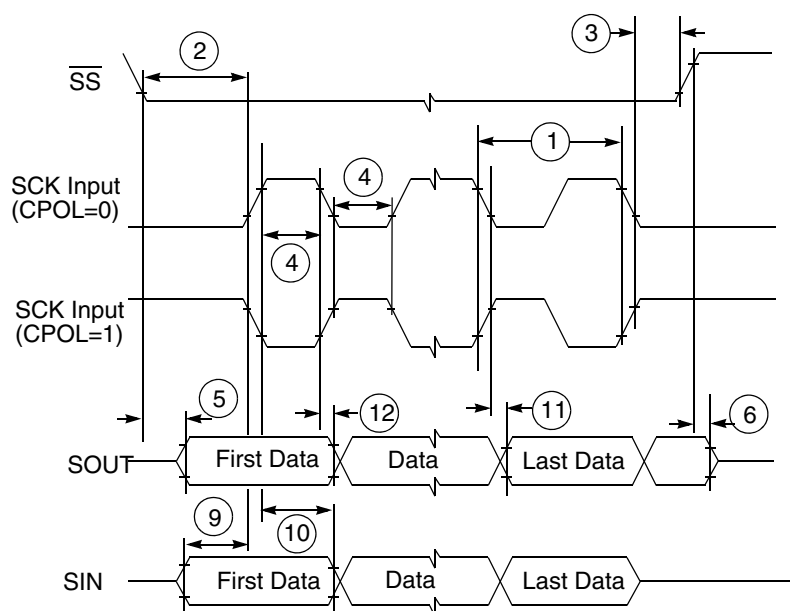


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMII. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

MediaLB (MLB) electrical specifications

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 45. MLB 3-Pin 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}		3	ns	V_{IL} to V_{IH}
MLBCLK fall time	t_{mckf}		3	ns	V_{IH} to V_{IL}
MLBCLK low time ¹	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	4	—	ns	2

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 46. MLB 3-Pin 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency ¹	f_{mck}	45.056 -	- 51.2	MHz MHz	1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz
MLBCLK rise time	f_{mckr}		1	ns	V_{IL} to V_{IH}
MLBCLK fall time	f_{mckf}		1	ns	V_{IH} to V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	2
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	3

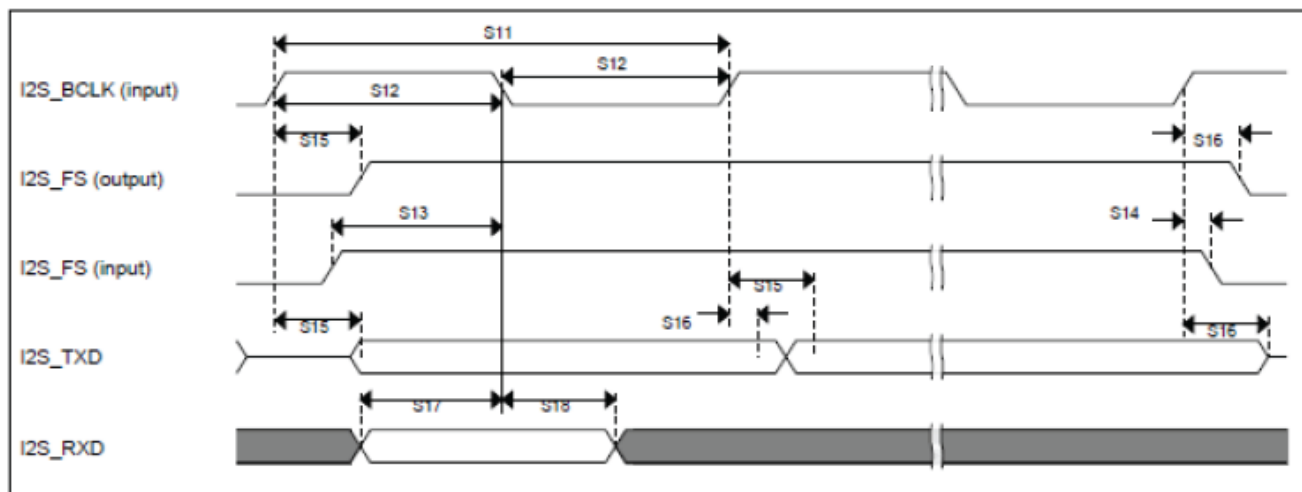


Figure 27. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 50. JTAG pin AC electrical characteristics ¹

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time ²	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20 ³	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600 ⁴	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

- These specifications apply to JTAG boundary scan only.
- This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
- Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
- Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

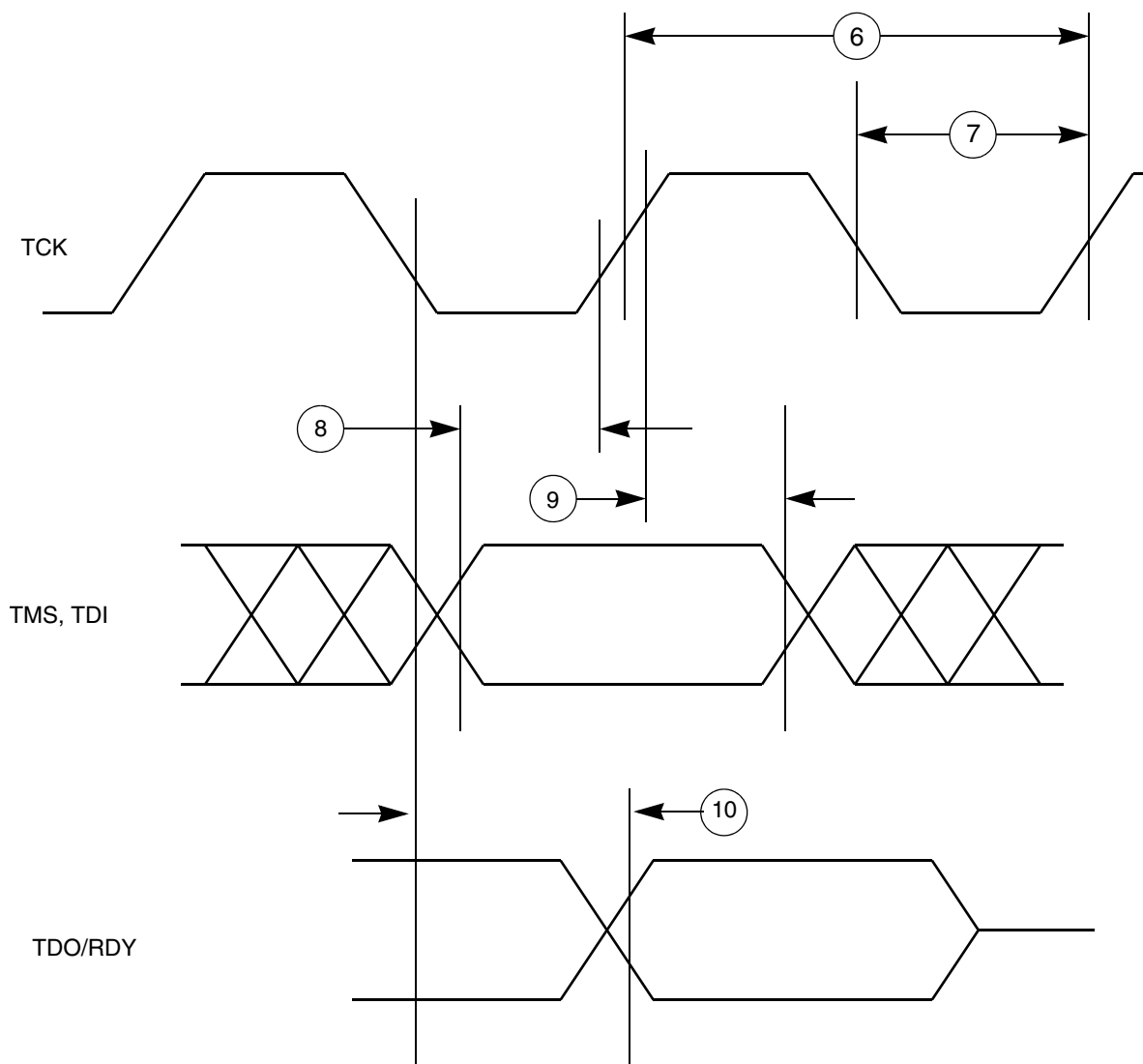


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI D}$	NMI pulse width that is passed	400	—	—	ns

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	18.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Reset sequence

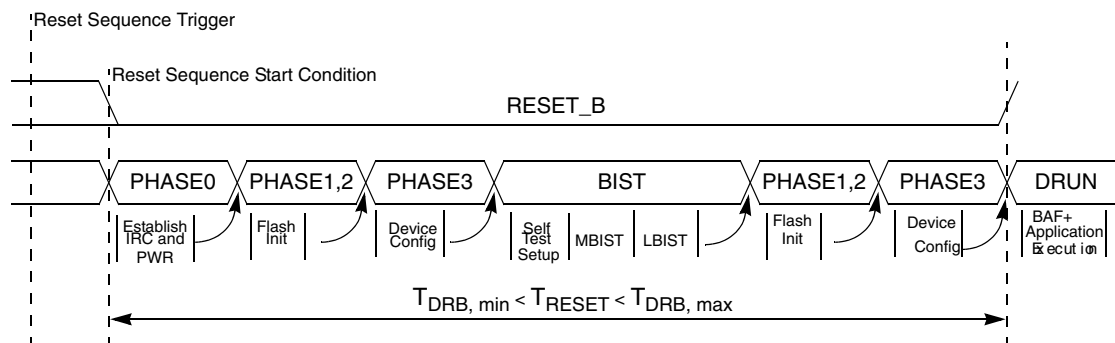


Figure 35. Destructive reset sequence, BIST enabled

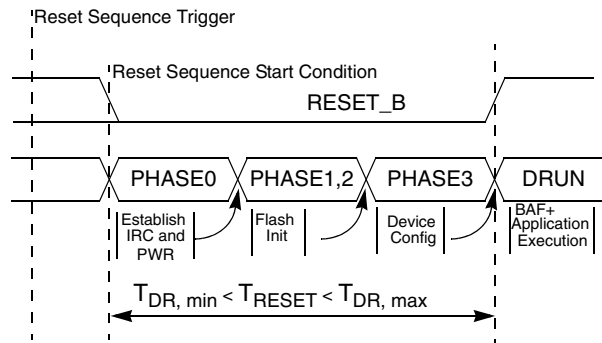


Figure 36. Destructive reset sequence, BIST disabled

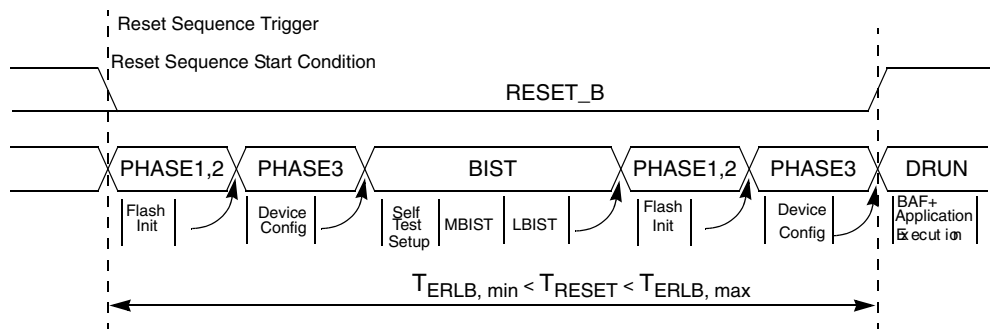


Figure 37. External reset sequence long, BIST enabled

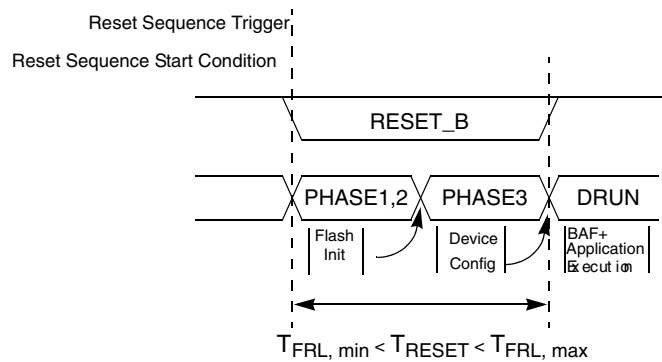


Figure 38. Functional reset sequence long

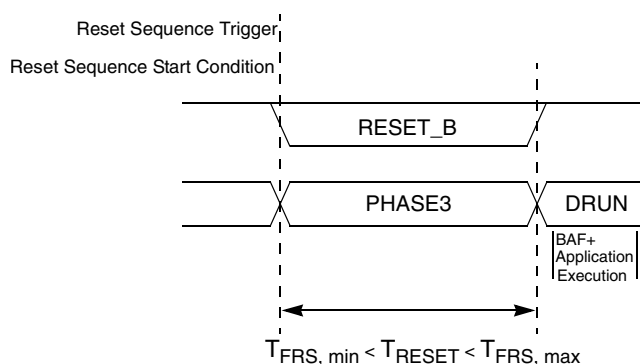


Figure 39. Functional reset sequence short

The reset sequences shown in [Figure 38](#) and [Figure 39](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 56. Revision History

Rev. No.	Date	Substantial Changes
1	14 March 2013	Initial Release
1.1	16 May 2013	Updated Pinouts section
2	22 May 2014	<ul style="list-style-type: none"> Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet Revised the feature list. Revised Introduction section to remove classification information. Updated optional information in the ordering information figure. Revised Absolute maximum rating section: <ul style="list-style-type: none"> Removed category column from table Added footnote at Ta Revised Recommended operating conditions section <ul style="list-style-type: none"> Added notes Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V) Updated table: Recommended operating conditions (VDD_HV_x = 5 V) Revised Voltage regulator electrical characteristics <ul style="list-style-type: none"> Updated text describing bipolar transistors Updated figure: Voltage regulator capacitance connection Updated table: Voltage regulator electrical specifications Removed Brownout information Revised Voltage monitor electrical characteristics table
		<ul style="list-style-type: none"> Revised Supply current characteristics section <ul style="list-style-type: none"> Updated table: Current consumption characteristics Updated table: Low Power Unit (LPU) Current consumption characteristics STANDBY Current consumption characteristics

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> In table: Functional Pad AC Specifications @ 3.3 V Range <ul style="list-style-type: none"> Updated values for symbol 'pad_sr_hv (output)' In table: DC electrical specifications @ 3.3V Range <ul style="list-style-type: none"> Updated values for VDD_HV_x, Vih, Vhys Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys In table: Functional Pad AC Specifications @ 5 V Range <ul style="list-style-type: none"> Updated values for symbol 'pad_sr_hv (output)' In table DC electrical specifications @ 5 V Range <ul style="list-style-type: none"> Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		<ul style="list-style-type: none"> In section: PORST electrical specifications <ul style="list-style-type: none"> In table: PORST electrical specifications <ul style="list-style-type: none"> Updated 'Min' value for $W_{NF\text{PORST}}$ Corrected 'Unit' for V_{IH} and V_{IL} In section: Peripheral operating requirements and behaviours <ul style="list-style-type: none"> Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) In section: Analogue Comparator (CMP) electrical specifications <ul style="list-style-type: none"> In table: Comparator and 6-bit DAC electrical specifications <ul style="list-style-type: none"> Updated 'Max' value of $I_{DDL\text{S}}$ Updated 'Min' and 'Max' for V_{AIO} and DNL Updated 'Description' 'Min' 'Max' of V_H Updated row for tDHS Added row for tDLS Removed row for VCMPOh and VCMPOI In section: Clocks and PLL interfaces modules <ul style="list-style-type: none"> Revised table: Main oscillator electrical characteristics In table: 16 MHz RC Oscillator electrical specifications <ul style="list-style-type: none"> Updated 'Max' of Tstartup In table: 128 KHz Internal RC oscillator electrical specifications <ul style="list-style-type: none"> Removed Uncalibrated 'Condition' for Fosc Updated 'Min' and 'Max' of Calibrated Fosc Updated 'Temperature dependence' and 'Supply dependence' In table: PLL electrical specifications <ul style="list-style-type: none"> Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption Removed 'Typ' value of Duty Cycle at pllclkout Removed 'Min' from calibration mode of Lock Time In table: Jitter calculation <ul style="list-style-type: none"> Added 1 Sigma Random Jitter value for Long term jitter
		<ul style="list-style-type: none"> In section Flash read wait state and address pipeline control settings <ul style="list-style-type: none"> Revised table: Flash Read Wait State and Address Pipeline Control Removed section: On-chip peripherals Added section: 'Reset sequence'
Rev4	Feb 10 2017	<ul style="list-style-type: none"> Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics Updated SIUL2_MSCRN[Src 1:0]=11 @25pF max value; SIUL2_MSCRN[Src 1:0]=11 @50pF min value; SIUL2_MSCRN[Src 1:0]=10 @25pF min and max values in AC specifications @ 3.3 V Range

Table continues on the next page...

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