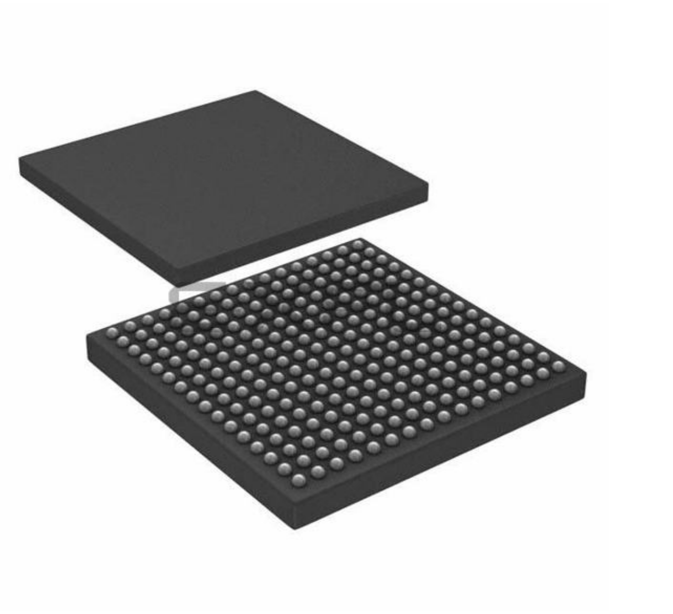

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/120MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747gk0ammj6

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Three System Timer Module (STM)
  - Four Software WatchDog Timers (SWT)
  - 96 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1) and 1149.7 (cJTAG)
- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS and TDM) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
  - ISO26262 ASIL compliance
- Multiple operating modes
  - Includes enhanced low power operation

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[3, 4]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[5]	Decoupling pin for low power regulators[6]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[7]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 µF capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA. SeeThermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
    - Control of external NPN ballast transistor
    - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

Table 13. ESD ratings (continued)

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
		conforming to AEC-Q100-002			
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
VDD_LV	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x[1]	I/O Supply Voltage	4.5	5.5	V
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VSS_LV- 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x	VDD_HV_x + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VSS_LV - 0.3	0.4 * VDD_HV_x	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VSS_LV - 0.3	0.35*VDD_HV_x	V
Pull_IIH (pad_i_hv)	Weak Pullup Current Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2 * VDD_HV_x 0.1*VDD_HV_x	V

Table continues on the next page...

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11)	38	132	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11)	48	220	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10)	19	66	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

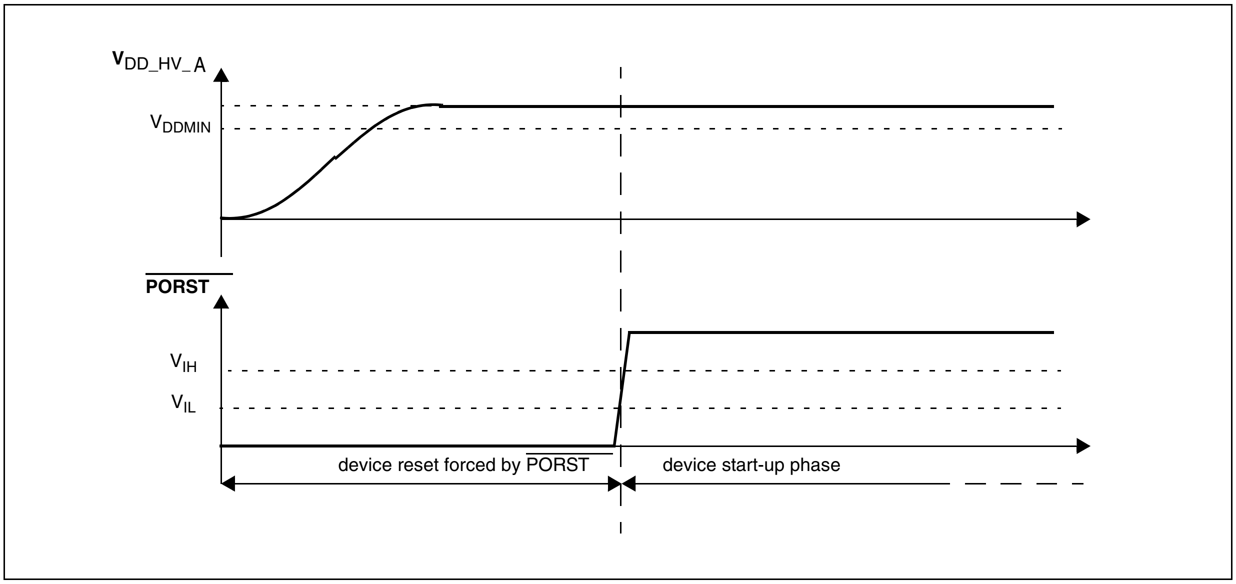

Figure 3. Start-up reset requirements

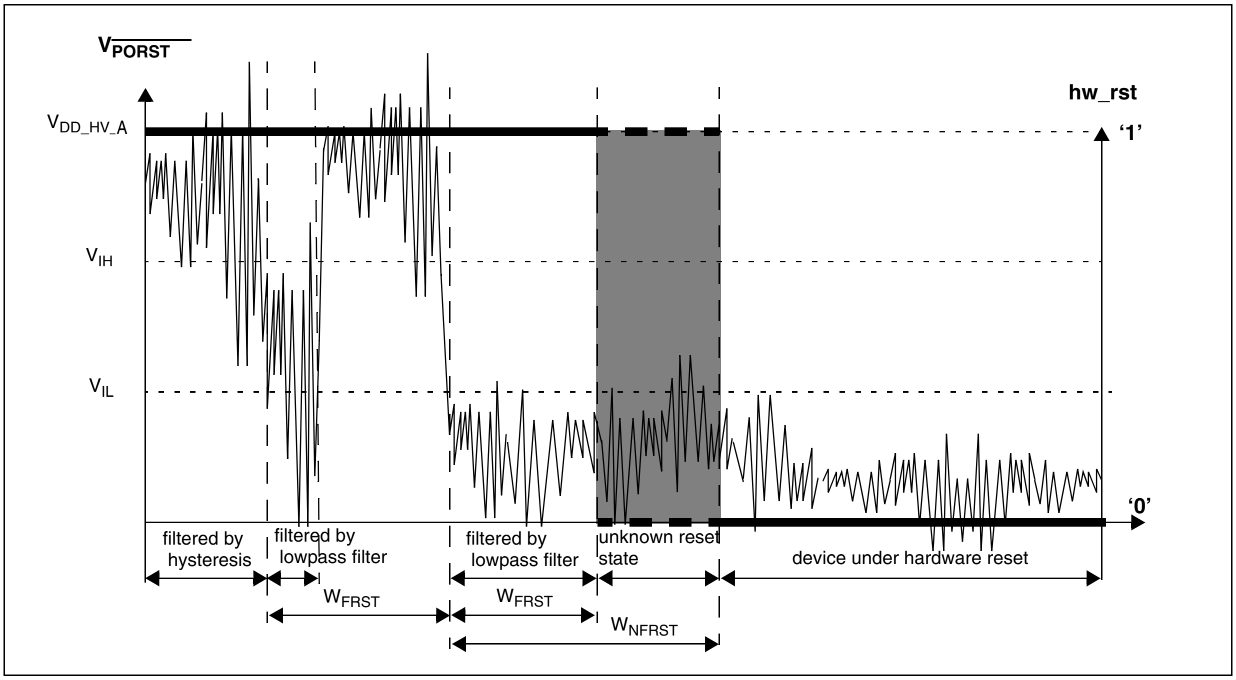

Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD\_HV\_A}$ +0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1]	Device under power-on reset $V_{DD\_HV\_A}= V_{DD\_POR}$ $V_{OL} = 0.35*V_{DD\_HV\_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD\_HV\_A}= V_{DD\_POR}$ $V_{OL} = 0.35*V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\lvert I_{WPU} \rvert$	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	μA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{PORST}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{PORST}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD\_HV\_A}$	—	V
V_{IL}	Input low level	—	0.35 x $V_{DD\_HV\_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 26. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 27. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 28	ps	NON SSCG mode
TIE			See Table 28		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 28. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/-(J_{SN}+J_{SDM}+J_{SSCG}+N[4] xJ_{RJ})
Long Term Jitter (Integer Mode)				40	+/-(N x J_{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J_{RJ})

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

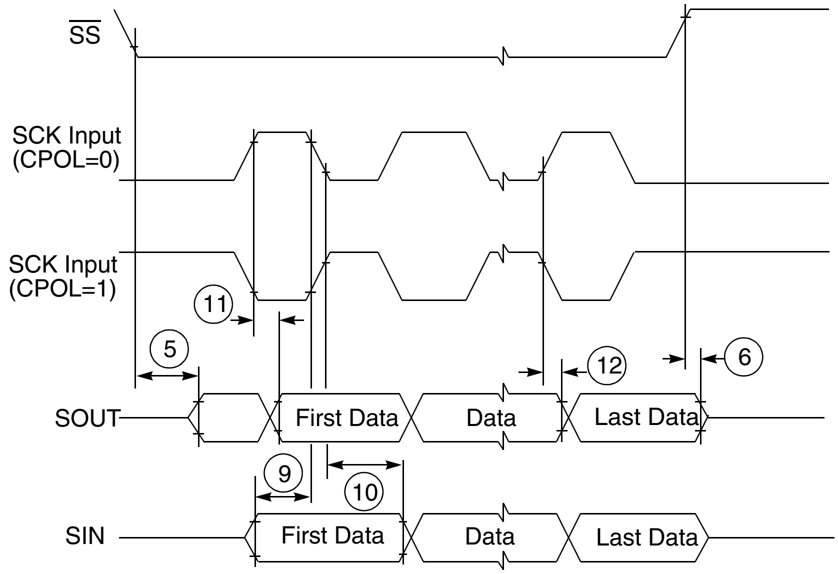

Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

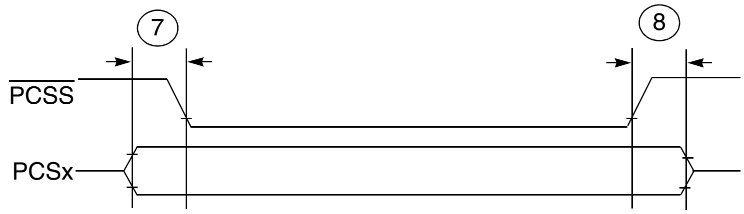

Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

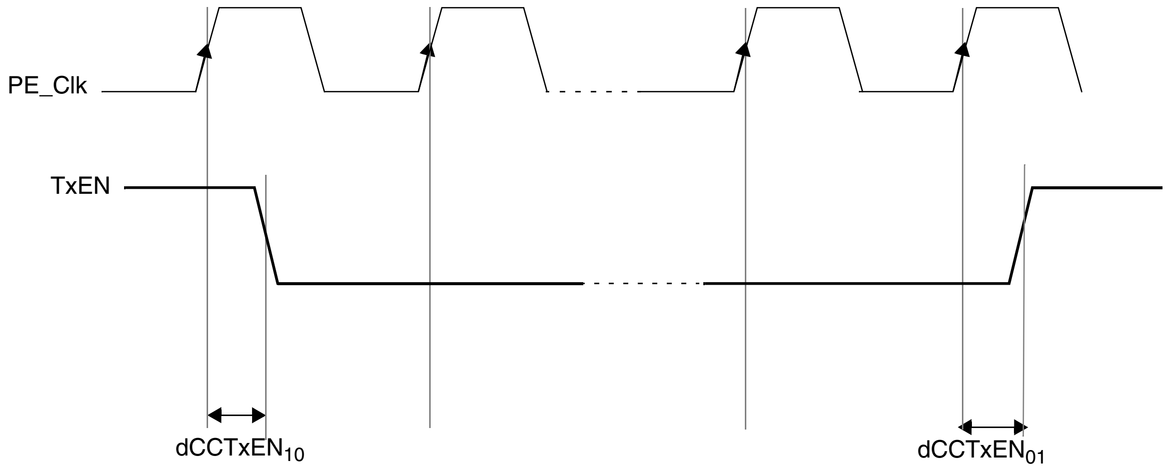

Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

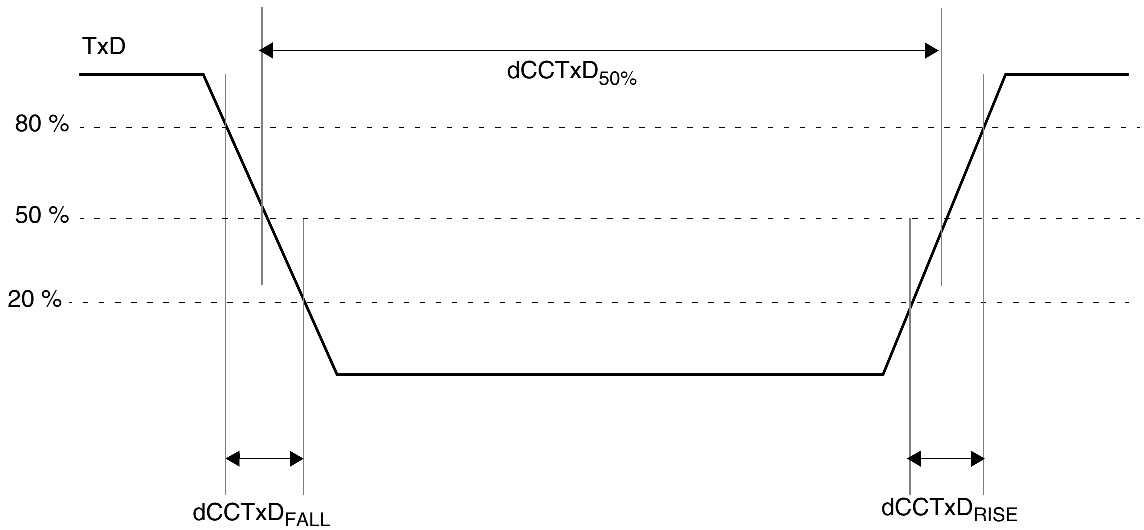

Figure 19. TxD Signal

Table 39. TxD output characteristics

Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}+dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9[2]	ns

Table continues on the next page...

6.4.5 MediaLB (MLB) electrical specifications

6.4.5.1 MLB 3-pin interface DC characteristics

The section lists the MLB 3-pin interface electrical characteristics.

Table 44. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	μA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

6.4.5.2 MLB 3-pin interface electrical specifications

This section describes the timing electrical information of the MLB module.

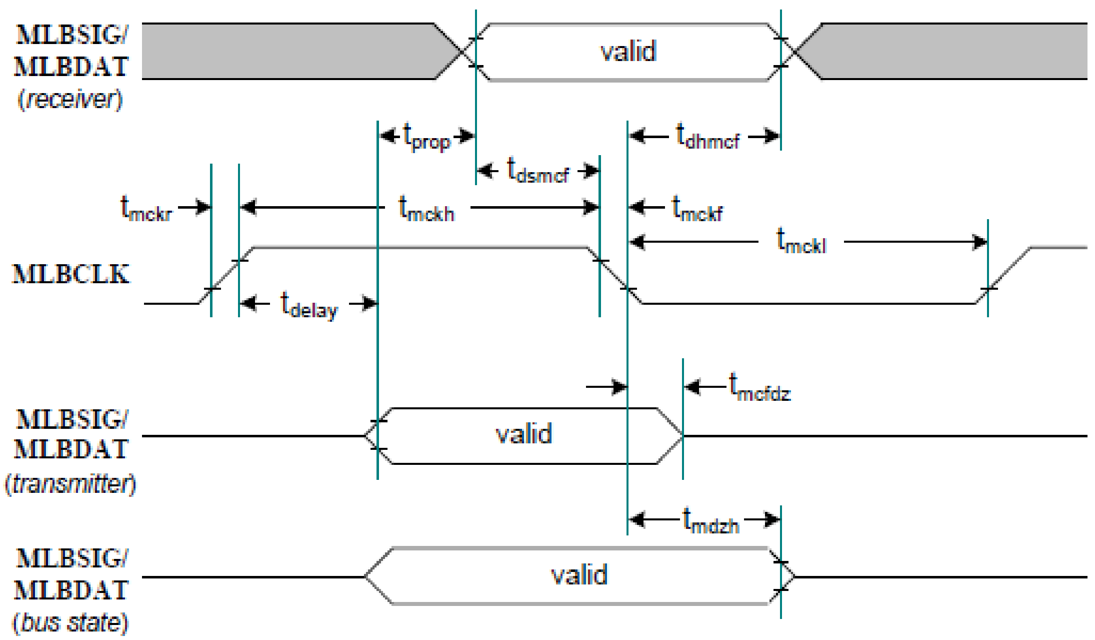

Figure 24. MediaLB 3-Pin Timing

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.
2. MLBCLK low/high time includes the pluse width variation.
3. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

6.4.6 USB electrical specifications

6.4.6.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

6.4.6.2 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 47. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

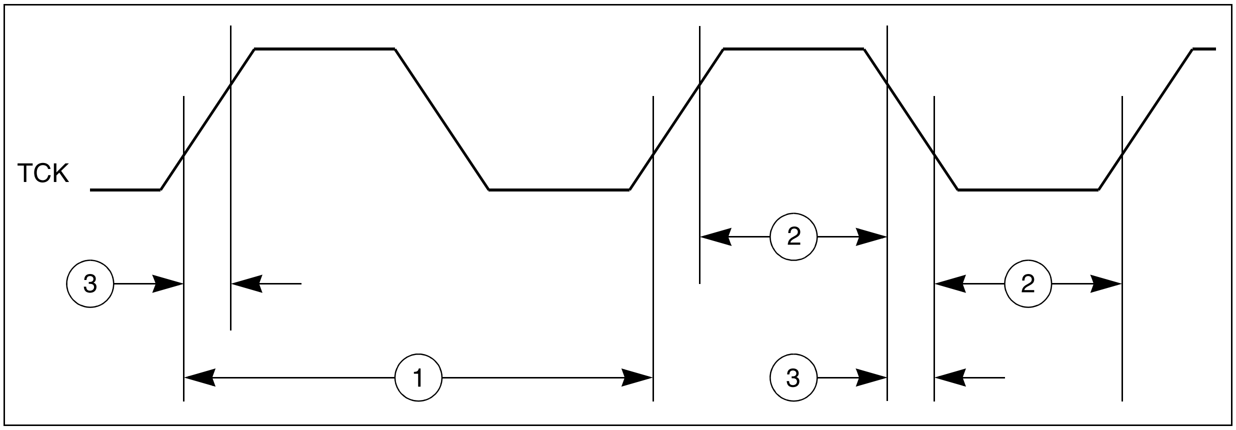

Figure 28. JTAG test clock input timing

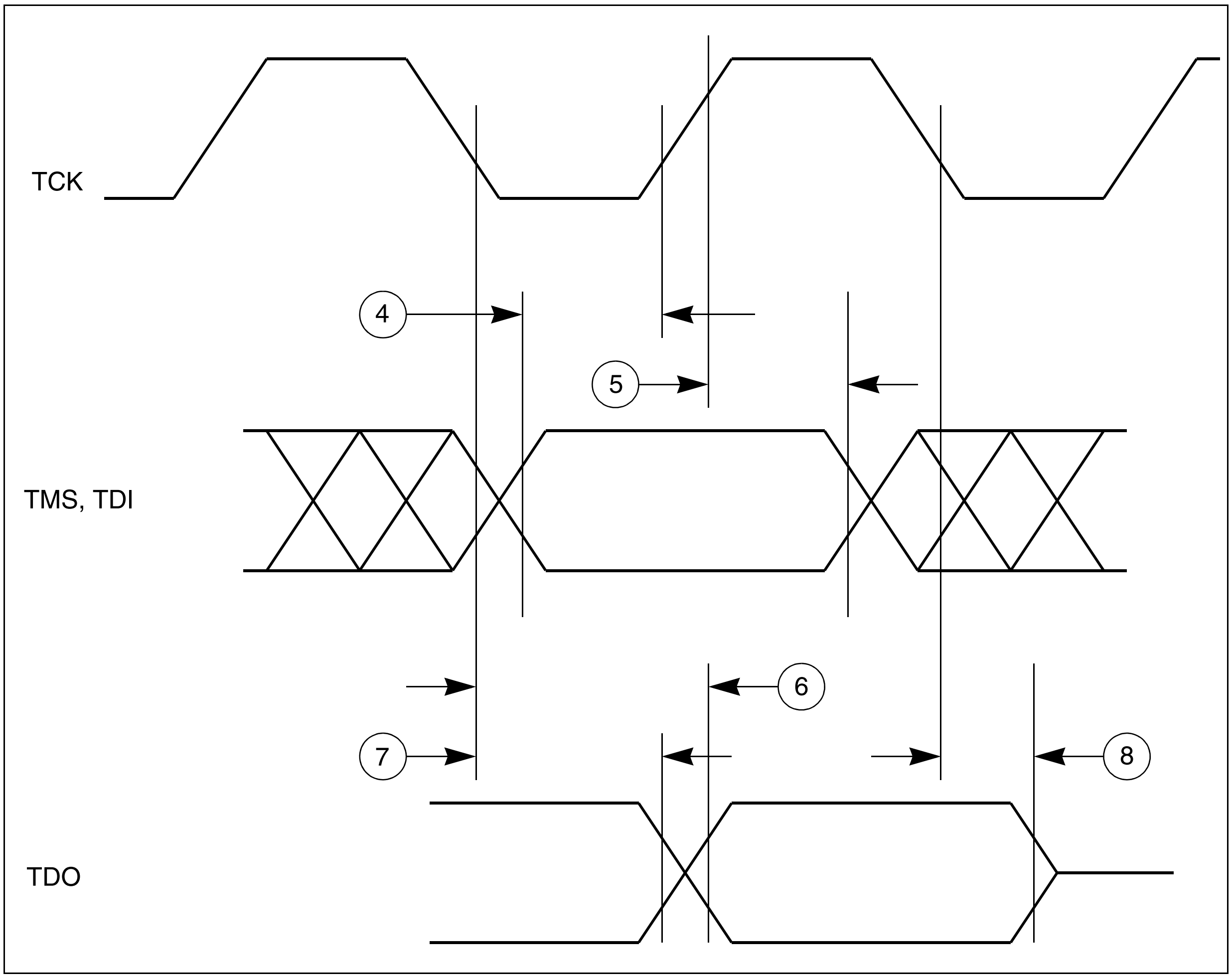

Figure 29. JTAG test access port timing

Table 51. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{MSEO}$, and $\overline{EVTO}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

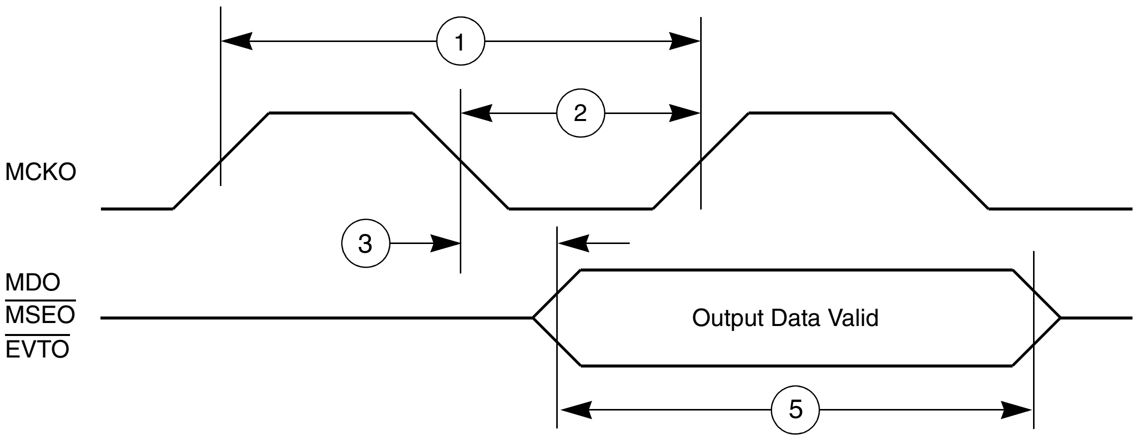

Figure 31. Nexus output timing

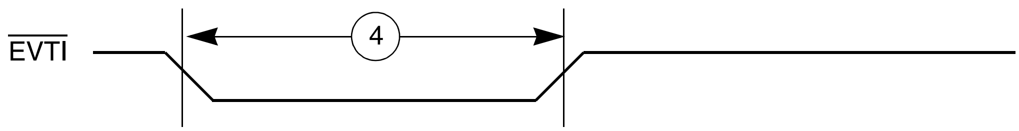

Figure 32. Nexus EVTI Input Pulse Width

Board type	Symbol	Description	176LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	18.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

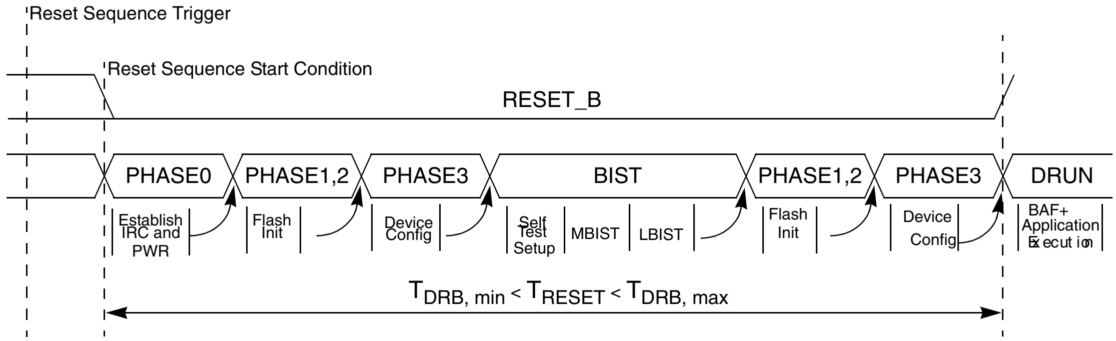

Figure 35. Destructive reset sequence, BIST enabled

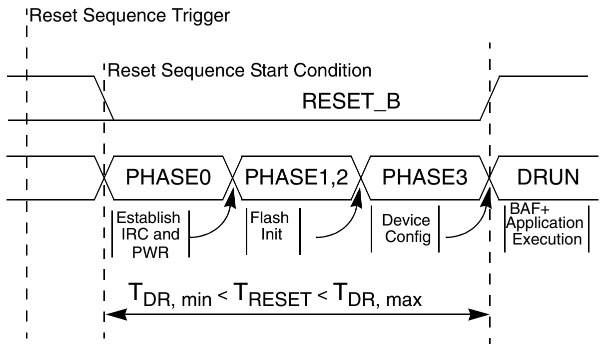

Figure 36. Destructive reset sequence, BIST disabled

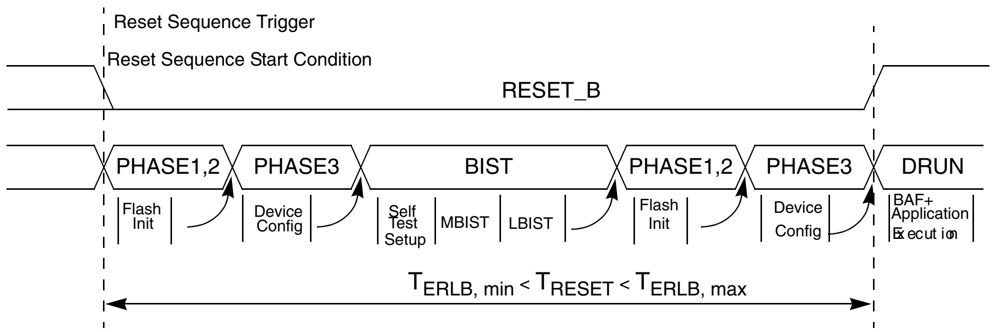

Figure 37. External reset sequence long, BIST enabled

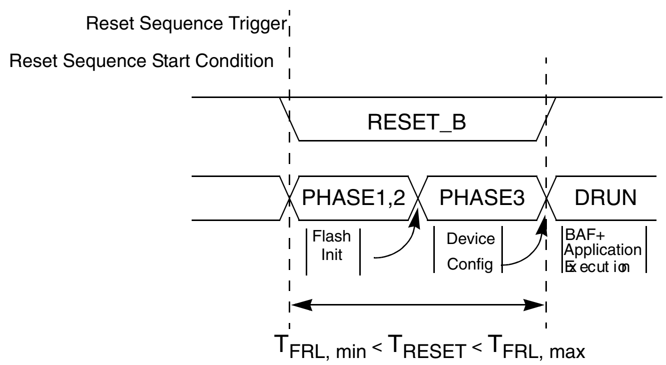

Figure 38. Functional reset sequence long