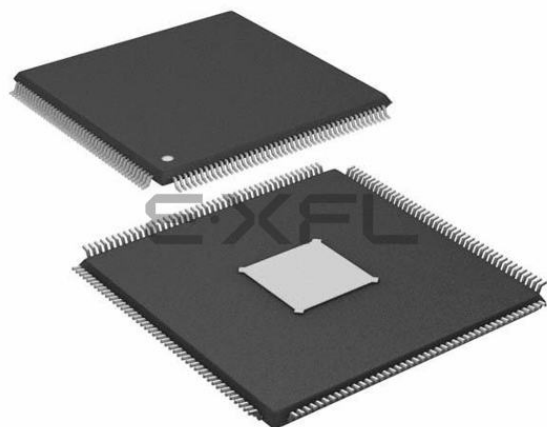




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747gk1cku6

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

Table 6. Recommended operating conditions ($V_{DD_HV_x} = 3.3\text{ V}$) (continued)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3\text{ V}$
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
5. $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
6. This supply is shorted $V_{DD_HV_A}$ on lower packages.

NOTE

If $V_{DD_HV_A}$ is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. $V_{DD_HV_FLA}$ should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
$V_{DD_HV_A}$ $V_{DD_HV_B}$ $V_{DD_HV_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD_HV_FLA}$ ³	HV flash supply voltage	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	HV ADC supply voltage	—	$\max(V_{DD_H_V_A}, V_{DD_H_V_B}, V_{DD_H_V_C}) - 0.05$	5.5	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
$V_{IN1_CMP_REF}$ ⁵	Analog Comparator DAC reference voltage	—	3.15	5.5	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When V_{DD_HV} is in 5 V range, $V_{DD_HV_FLA}$ cannot be supplied externally. This pin is decoupled with C_{flash_reg} .
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. This supply is shorted $V_{DD_HV_A}$ on lower packages.

Table 8. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{HV_VDD_A}$	VDD_HV_A supply capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{HV_VDD_B}$	VDD_HV_B supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
$C_{HV_VDD_C}$	VDD_HV_C supply capacitor ⁵	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
C_{HV_ADC0} C_{HV_ADC1}	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	μF
C_{HV_ADR} ⁶	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	μF
$V_{DD_HV_BALLAST}$ ⁷	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C_BALLAST}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{C_BALLAST}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time after main supply stabilization	$C_{fp_reg} = 3 \mu F$	—	74	—	μs
t_{ramp}	Load current transient	I_{load} from 15% to 55% $C_{fp_reg} = 3 \mu F$		1.0		μs

- Split capacitance on each pair VDD_LV pin should sum up to a total value of C_{fp_reg}
- Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
- Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
- It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FL A pin and the routing inductance should be less than 1nH.
- For VDD_HV_A, VDD_HV_B, and VDD_HV_C, 1 μF on each side of the chip
 - 0.1 μF close to each VDD/VSS pin pair.
 - 10 μF near for each power supply source
 - For VDD_LV, 0.1 μF close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
 - For VDD_LV, 0.1 μF close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
- Only applicable to ADC1

Table 9. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up ¹	Mask Opt	Reset Type	Min	Typ	Max	V
V _{HVD_LV_cold}	LV supply high voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.325	1.345	1.375	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.345	1.365	1.395	V
V _{LVD_LV_PD2_hot}	LV supply low voltage monitoring, detecting in the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.125	1.143	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.145	1.163	1.180	V
V _{LVD_LV_PD1_hot}	LV supply low voltage monitoring, detecting in the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.114	1.137	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.134	1.157	1.180	V
V _{LVD_LV_PD0_hot}	LV supply low voltage monitoring, detecting in the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.114	1.137	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.134	1.157	1.180	V
V _{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Powerup	2.700	2.850	3.000	V
		Rise	Untrimmed				2.750	2.900	3.050	V
V _{LVD_IO_A_LO} ²	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Powerup	2.750	2.923	3.095	V
			Trimmed				2.978	3.039	3.100	V
		Rise	Untrimmed				2.780	2.953	3.125	V
			Trimmed				3.008	3.069	3.130	V
V _{LVD_IO_A_HI} ²	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Functional	Disabled at Start			
			4.060				4.151	4.240	V	
		Rise	Trimmed				Disabled at Start			
			4.115				4.201	4.3	V	
V _{LVD_LV_PD2_cold}	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.14	1.158	1.175	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.16	1.178	1.195	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. There is no voltage monitoring on the V_{DD_HV_ADC0}, V_{DD_HV_ADC1}, V_{DD_HV_B} and V_{DD_HV_C} I/O segments. For applications requiring monitoring of these segments, either connect these to V_{DD_HV_A} at the PCB level or monitor externally.

General

- x FlexCAN state machines clocked (other FLEXCAN clock gated), 4 x LINFlexD transmitting (Other clock gated), 1x eMIOS clocked (used OPWFMB mode) (Others clock gated), FIRC, SIRC, FXOSC, SXOSC, PLL running, BCTU, DMAMUX, ACOMP clock gated. All others modules clock gated if not specifically mentioned. I/O supply current excluded
6. Recommended Transistors: MJD31 @ 85°C, 105°C and 125°C.
 7. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @ 120Mhz (Instruction and Data cache enabled), Platform @ 120MHz, SRAMs accessed in parallel, Flash access (prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT (ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting (others DSPIs clocked), 2 x SPI transmitting (others clocked), 4 x FlexCAN state machines working (others clocked), 9x LINFlexD transmitting (others clocked), 1x eMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC, CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
 8. Recommended Transistors: BCP56, BCP68 or MJD31 @ 85°C, BCP56, BCP68 or MJD31 @ 105°C and MJD31 @ 125°C.
 9. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @ 80Mhz (Instruction and Data cache enabled), Platform @ 80MHz, SRAMs accessed in parallel, Flash access (prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT (ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting (others DSPIs clocked), 2 x SPI transmitting (others clocked), 4 x FlexCAN state machines working (others clocked), 9x LINFlexD transmitting (others clocked), 1x eMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC, CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
 10. Recommended Transistors: BCP56, BCP68 or MJD31 @ 85°C, 105°C and 125°C
 11. Internal structures hold the input voltage less than $V_{DD_HV_ADC_REF} + 1.0$ V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
 12. This value is the total current for two ADCs. Each ADC might consume up to 2mA at max.

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM, but only one RAM being accessed	$T_a = 25^\circ\text{C}$ SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	8.9		mA
		$T_a = 25^\circ\text{C}$ SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON		10.2		
		$T_a = 85^\circ\text{C}$	—	12.5	22	
		$T_a = 105^\circ\text{C}$	—	14.5	24	
		$T_a = 125^\circ\text{C}$ ² SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	16	26	
LPU_STOP	with 256K RAM	$T_a = 25^\circ\text{C}$	—	0.535		mA
		$T_a = 85^\circ\text{C}$	—	0.72	6	
		$T_a = 105^\circ\text{C}$	—	1	8	
		$T_a = 125^\circ\text{C}$ ²	—	1.6	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming $T_a = T_j$, as the device is in static (fully clock gated) mode. Assumes maximum θ_{JA} of 2s2p board. See [Thermal attributes](#)

Table 13. ESD ratings (continued)

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
		conforming to AEC-Q100-002			
V _{ESD(CDM)}	Electrostatic discharge (Charged Device Model)	T _A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 14. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns) ¹ L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCrN[Src 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry ²	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00 ³
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input) ⁴		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.

3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

5.2 DC electrical specifications @ 3.3V Range

Table 15. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
VDD	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x ¹	I/O Supply Voltage	3.15	3.63	V
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	$0.72 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	$VSS_LV - 0.3$	$0.45 \cdot VDD_HV_x$	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	$0.11 \cdot VDD_HV_x$		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	$0.67 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	$VSS_LV - 0.3$	$0.35 \cdot VDD_HV_x$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	$0.57 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	$VSS_LV - 0.3$	$0.4 \cdot VDD_HV_x$	V
Vhys	CMOS Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x$		V
Pull_IH (pad_i_hv)	Weak Pullup Current Low	15		μA
Pull_IH (pad_i_hv)	Weak Pullup Current High		55	μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ³ Low	28		μA
Pull_IL (pad_i_hv)	Weak Pulldown Current ² High		85	μA
Pull_Ioh	Weak Pullup Current ⁴	15	50	μA
Pull_Iol	Weak Pulldown Current ⁵	15	50	μA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μA
Voh	Output High Voltage ⁶	$0.8 \cdot VDD_HV_x$	—	V
Vol	Output Low Voltage ⁷	—	$0.2 \cdot VDD_HV_x$	V

Table continues on the next page...

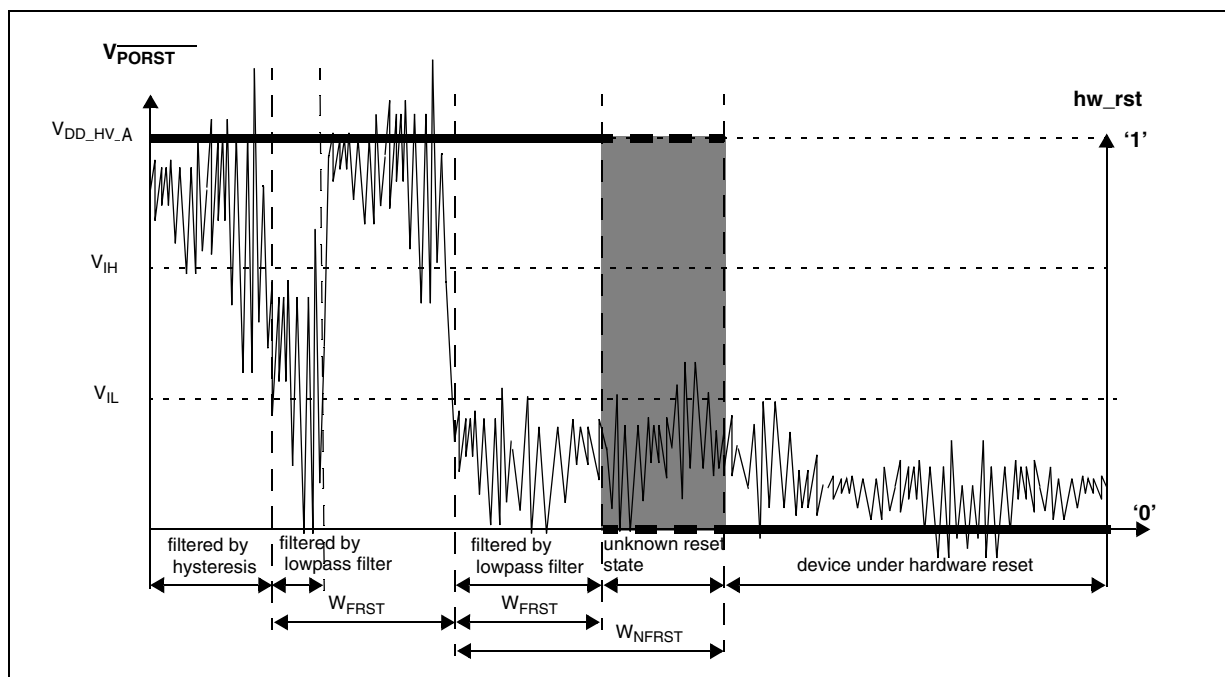


Figure 4. Noise filtering on reset signal

Table 18. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD_HV_A} + 0.4$	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	-0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current ¹	Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \cdot V_{DD_HV_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD_HV_A} = V_{DD_POR}$ $V_{OL} = 0.35 \cdot V_{DD_HV_IO}$	11	—	—	mA
W_{FRST}	RESET input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET input not filtered pulse	—	2000	—	—	ns
I_{WPUL}	Weak pull-up current absolute value	RESET pin $V_{IN} = V_{DD}$	23	—	82	μA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V _{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V _{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t _{cst}	Crystal Start-up Time ^{1, 2}				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F _{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
T _{startup}	Startup time	—		—	1.5	us
T _{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T _{LTJIT}	Long term jitter		—	—	0.2	%

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

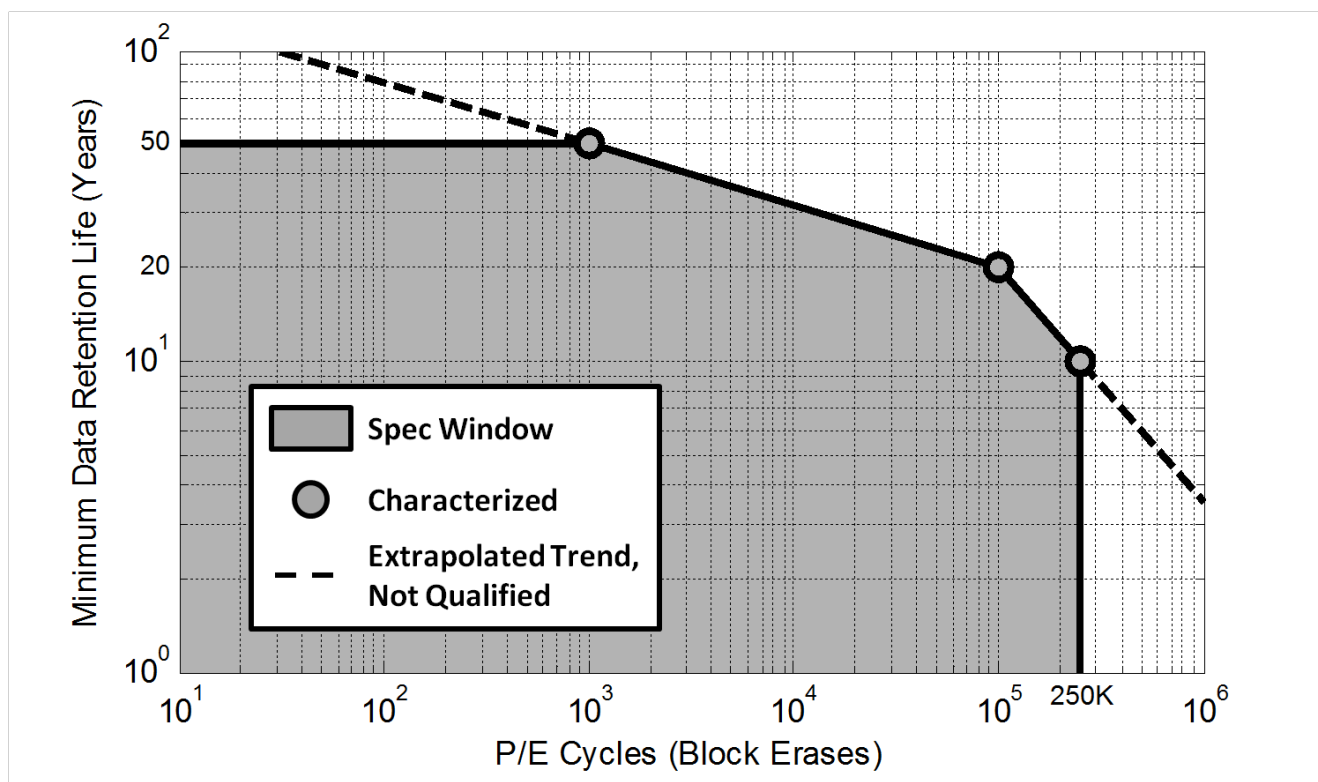
6.3.3 Flash memory module life specifications

Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.5 Flash memory AC timing specifications

Table 33. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	μs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	μs
t_{drvc}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	μs

Table 35. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	-5	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11 ¹	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-5	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	4	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	4	—	16 ¹	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	-2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10 ¹	—	
			Master (MTFE = 1, CPHA = 1)	-2	—	-2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see [Table 35](#)

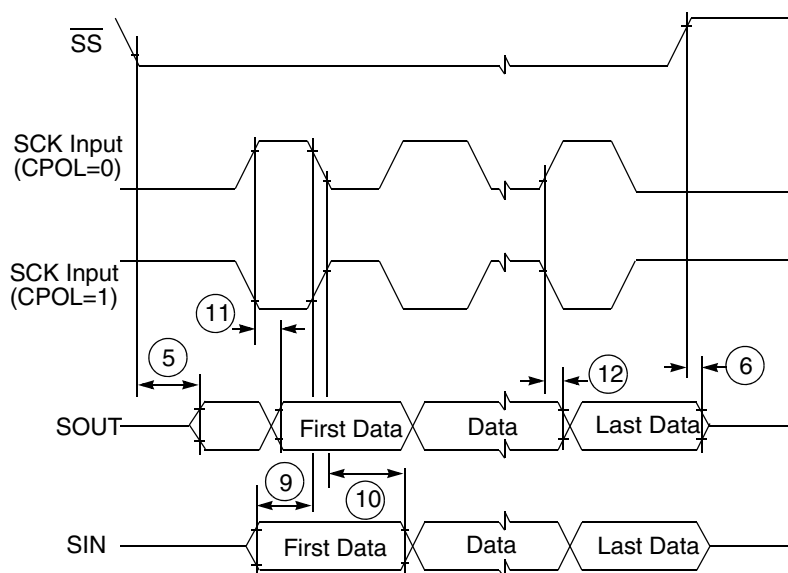


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

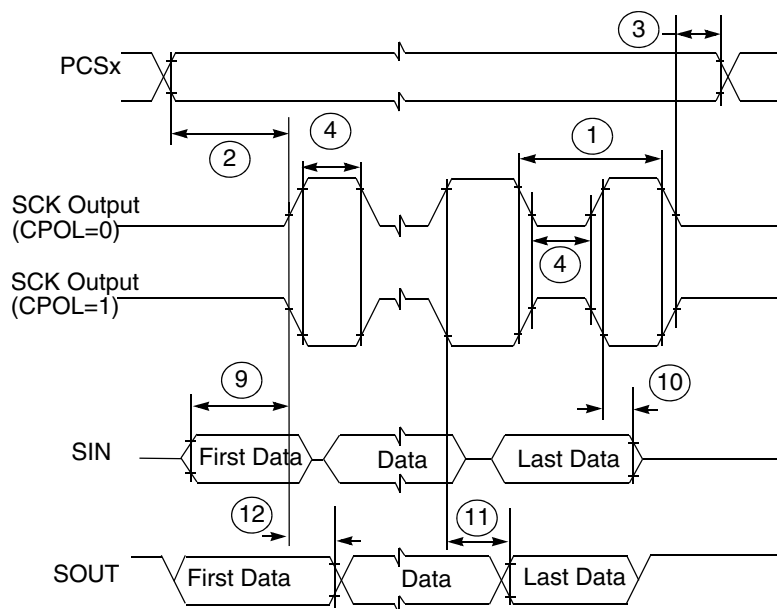


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

Reset sequence

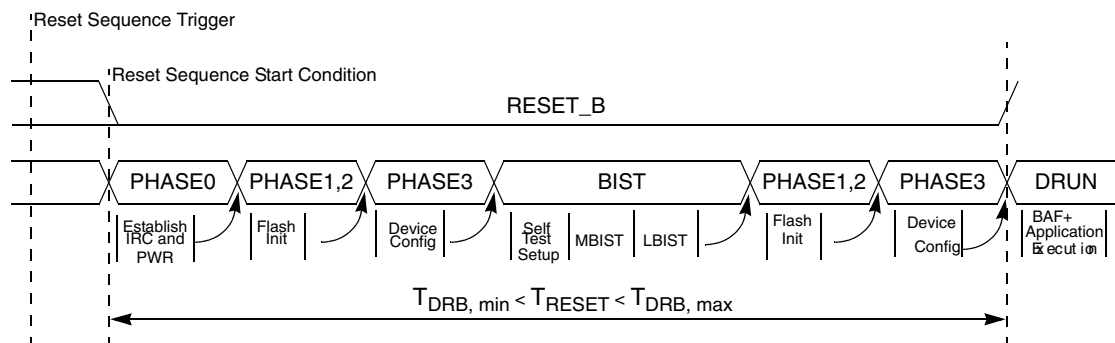


Figure 35. Destructive reset sequence, BIST enabled

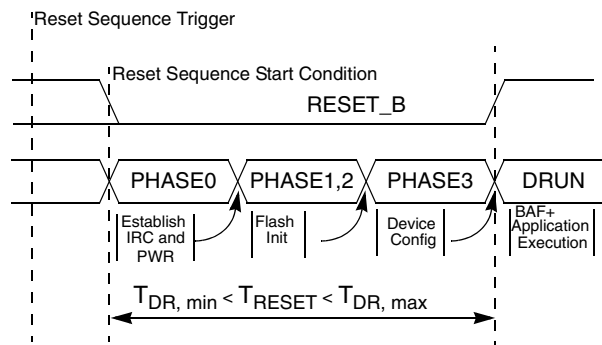


Figure 36. Destructive reset sequence, BIST disabled

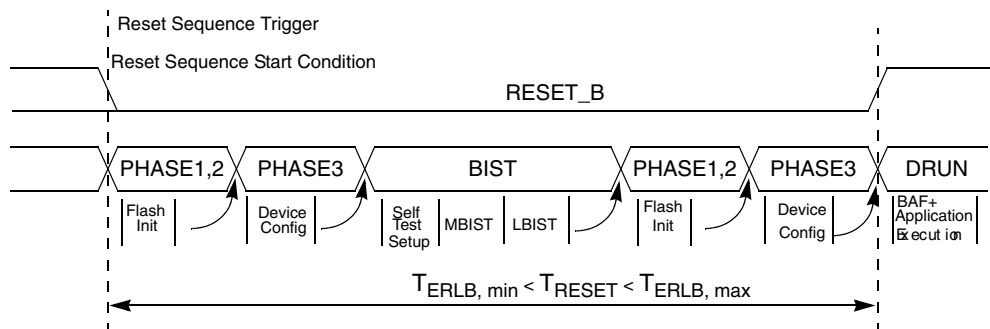


Figure 37. External reset sequence long, BIST enabled

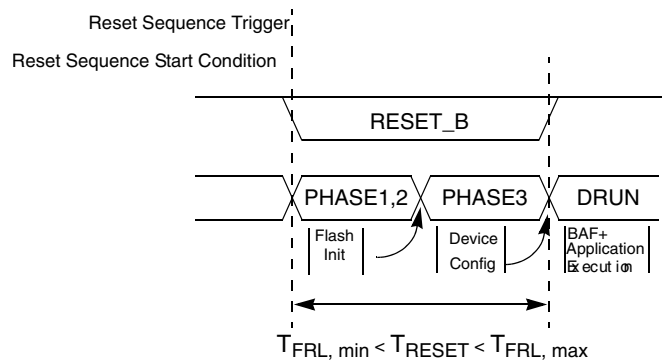


Figure 38. Functional reset sequence long

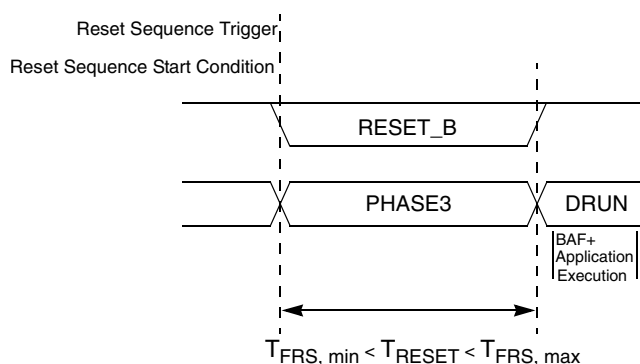


Figure 39. Functional reset sequence short

The reset sequences shown in [Figure 38](#) and [Figure 39](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 56. Revision History

Rev. No.	Date	Substantial Changes
1	14 March 2013	Initial Release
1.1	16 May 2013	Updated Pinouts section
2	22 May 2014	- Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet - Revised the feature list. - Revised Introduction section to remove classification information. - Updated optional information in the ordering information figure. - Revised Absolute maximum rating section: - Removed category column from table - Added footnote at Ta - Revised Recommended operating conditions section - Added notes - Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V) - Updated table: Recommended operating conditions (VDD_HV_x = 5 V) - Revised Voltage regulator electrical characteristics - Updated text describing bipolar transistors - Updated figure: Voltage regulator capacitance connection - Updated table: Voltage regulator electrical specifications - Removed Brownout information - Revised Voltage monitor electrical characteristics table
		- Revised Supply current characteristics section - Updated table: Current consumption characteristics - Updated table: Low Power Unit (LPU) Current consumption characteristics - STANDBY Current consumption characteristics

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Removed row for symbol 'V_{SS_LV}' - Removed footnote from 'Max' column of symbols 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}'
		- In section: Recommended operating conditions - In table: Recommended operating conditions (V_{DD_HV_x} = 5 V) - Added footnote to 'Conditions' column - Updated footnote for 'Min' column - Removed footnote from symbols 'V_{DD_HV_A}', 'V_{DD_HV_B}' and 'V_{DD_HV_C}' - Removed row for symbol: 'V_{SS_HV}' - Updated 'Parameter' column for symbol 'V_{DD_HV_ADC1_REF}' - Updated 'Min' column of symbol 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' - Updated 'Parameter', 'Min' 'Max' column for symbol 'V_{SS_HV_ADC0}' and 'V_{SS_HV_ADC1}' - Added footnote to symbol 'V_{DD_LV}' - Removed row for symbol 'V_{SS_LV}' - Added row for symbol 'V_{IN1_CMP_REF}' and corresponding footnotes to the symbol - In section: Voltage regulator electrical characteristics - In table: Voltage regulator electrical specifications - Added note to symbol 'Cbe_fpreg' - In section: Voltage monitor electrical characteristics - In table: Voltage monitor electrical characteristics - Updated column 'Parameter', 'Min' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{HVD_LV_cold}' and 'V_{LVD_IO_A_HI}' - Updated column 'Parameter', 'Min' and 'Typ' (of fall/rise trimmed condition) for symbol 'V_{LVD_LV_PD2_hot}', 'V_{LVD_LV_PD2_cold LV}' - Updated column 'Parameter' for symbol 'V_{LVD_LV_PD0_hot}' - Updated column 'Typ' and 'Max' (of fall/rise trimmed condition) for symbol 'V_{LVD_FLASH}' - Updated footnote on symbol 'V_{LVD_IO_A_LO}' and 'V_{LVD_IO_A_HI}'
		- In section: Supply current characteristics - In table: Current consumption characteristics - Updated column 'Typ' for symbol 'I_{DD_FULL}' for temperature 85, 105, 125 - Updated column 'Typ' for symbol 'I_{DD_GWY}' for temperature 85, 105, 125 and column 'Max' for temperature 105 - Updated column 'Typ' for symbol 'I_{DD_BODY1}' for temperature 85, 105, 125 - Updated column 'Typ' for symbol 'I_{DD_BODY2}' for temperature 85, 105, 125 and 'Max' for temperature 125 - Added 'Typ' value for temperature 25 for symbol 'I_{DD_STOP}' - Updated column 'Typ' and 'Max' for symbol 'I_{DD_STOP}' for temperature 85, 105, 125 - In table: Low Power Unit (LPU) Current consumption characteristics - Updated column 'Typ' for symbol 'LPU_RUN' for temperature 25 and 125 - Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_RUN' - Updated column 'Typ' for symbol 'LPU_STOP' for temperature 25 and 125 - Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_STOP' - In table: STANDBY Current consumption characteristics - Updated to have one STANDBY - In section: I/O parameters

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- In table: Functional Pad AC Specifications @ 3.3 V Range - Updated values for symbol 'pad_sr_hv (output)' - In table: DC electrical specifications @ 3.3V Range - Updated values for VDD_HV_x, Vih, Vhys - Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys - In table: Functional Pad AC Specifications @ 5 V Range - Updated values for symbol 'pad_sr_hv (output)' - In table DC electrical specifications @ 5 V Range - Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		- In section: PORST electrical specifications - In table: PORST electrical specifications - Updated 'Min' value for $W_{NF\text{PORST}}$ - Corrected 'Unit' for V_{IH} and V_{IL} - In section: Peripheral operating requirements and behaviours - Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) - In section: Analogue Comparator (CMP) electrical specifications - In table: Comparator and 6-bit DAC electrical specifications - Updated 'Max' value of $I_{DDL\text{S}}$ - Updated 'Min' and 'Max' for V_{AIO} and DNL - Updated 'Description' 'Min' 'Max' of V_H - Updated row for tDHS - Added row for tDLS - Removed row for VCMPOh and VCMPOI - In section: Clocks and PLL interfaces modules - Revised table: Main oscillator electrical characteristics - In table: 16 MHz RC Oscillator electrical specifications - Updated 'Max' of Tstartup - In table: 128 KHz Internal RC oscillator electrical specifications - Removed Uncalibrated 'Condition' for Fosc - Updated 'Min' and 'Max' of Calibrated Fosc - Updated 'Temperature dependence' and 'Supply dependence' - In table: PLL electrical specifications - Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption - Removed 'Typ' value of Duty Cycle at pllclkout - Removed 'Min' from calibration mode of Lock Time - In table: Jitter calculation - Added 1 Sigma Random Jitter value for Long term jitter
		- In section Flash read wait state and address pipeline control settings - Revised table: Flash Read Wait State and Address Pipeline Control - Removed section: On-chip peripherals - Added section: 'Reset sequence'
Rev4	Feb 10 2017	- Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics - Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics - Updated SIUL2_MSCRN[Src 1:0]=11 @25pF max value; SIUL2_MSCRN[Src 1:0]=11 @50pF min value; SIUL2_MSCRN[Src 1:0]=10 @25pF min and max values in AC specifications @ 3.3 V Range

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Updated VIH min and VIL max values in Main oscillator electrical characteristics - Replaced ipp_sre[1:0] by SIUL2_MSCRn[SRC 1:0] in AC specifications @ 3.3 V Range, DC electrical specifications @ 3.3V Range - Functional reset sequence short, unsecure boot corrected Reset sequence duration - Added NVM memory map and RAM memory map Family comparison - Added BAF execution duration section BAF execution duration - Supply names (VDD_LV, VSS_LV replace dvss, avss, dvdd, avdd) corrected in Jitter calculation table PLL electrical specifications - Updated Ordering information: Fab and Mask version indicator - Updated tpsus typical and max values Flash memory AC timing specifications - Added Notes on IBIS models use in AC specifications @3.3 V Range AC specifications @ 3.3 V Range - Updated Vol value in DC electrical specifications @ 3.3V Range DC electrical specifications @ 3.3V Range - Added Notes on IBIS models in Functional Pad AC Specifications @ 5 V Range AC specifications @ 5 V Range - Updated Vol values in DC electrical specifications @5V Range DC electrical specifications @ 5 V Range - Updated IDD Current values Supply current characteristics - Updated STANDBY current consumption with FIRC ON Supply current characteristics - Thermal numbers update for 256MAPBGA Thermal attributes - POR_HV Trim values removed Voltage monitor electrical characteristics - ADC analog pad leakage for 105 C added ADC electrical specifications - IDD STANDBY0, 1, 2 and 3 added Supply current characteristics
Rev5	July 31 2017	- Updated Standby2 value to 125 C in Standby current consumption characteristics - Corrected typo in Note from "case" to "cause" Voltage regulator electrical characteristics - Updated propagation delay from 14 to 21 in ACMP electrical specifications

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