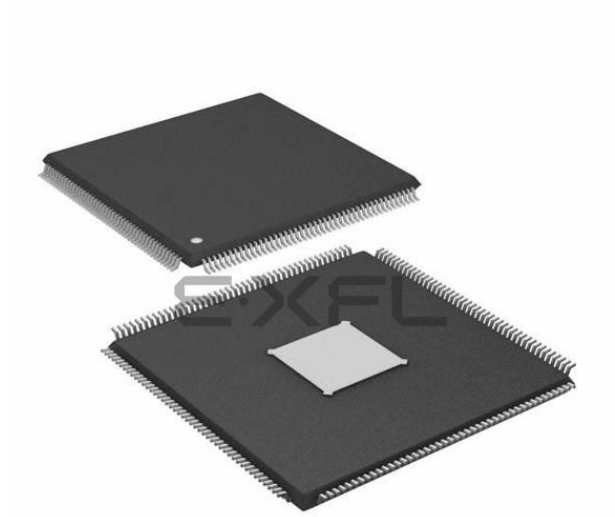

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747gk1mku6

1 Block diagram

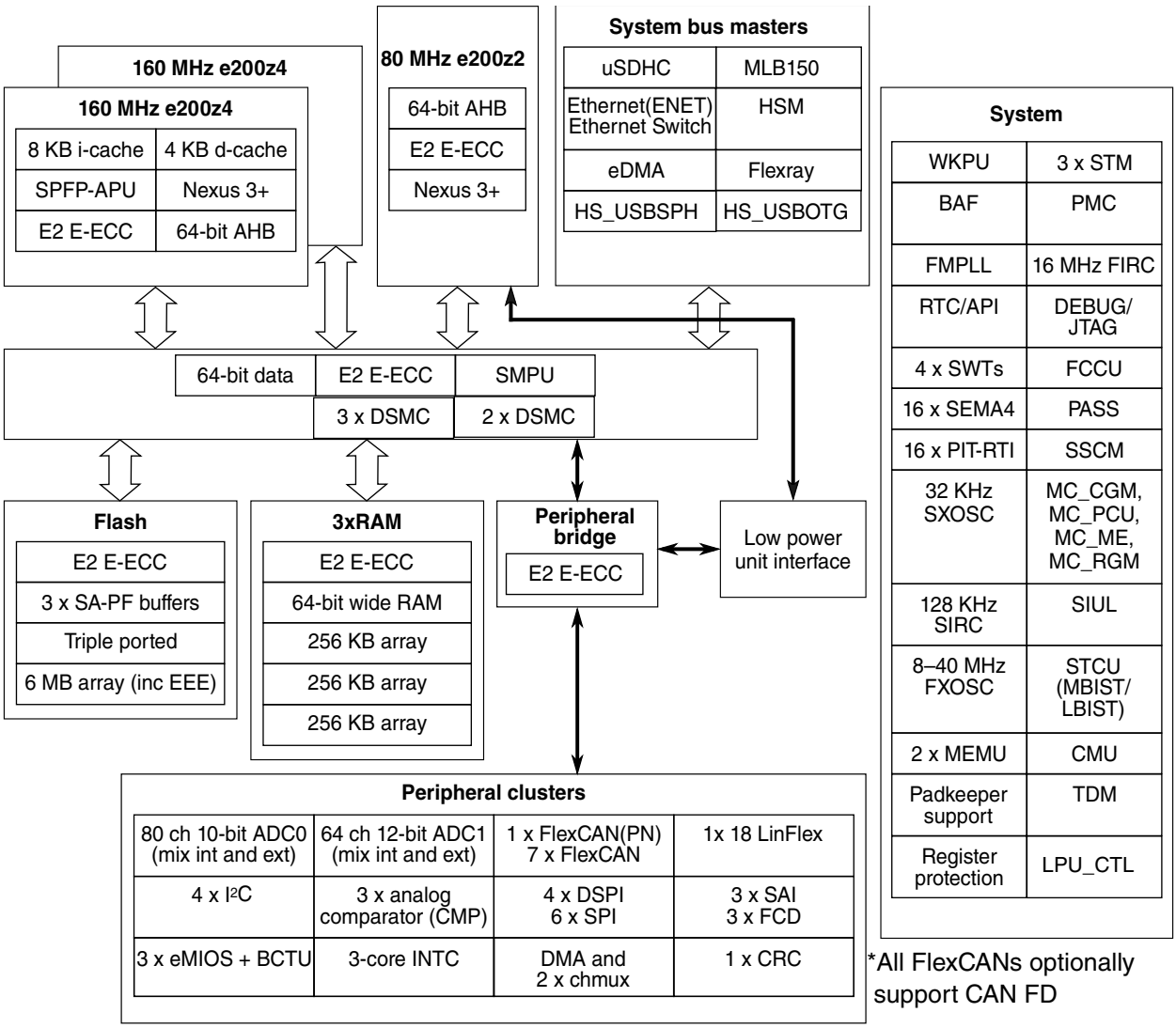


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

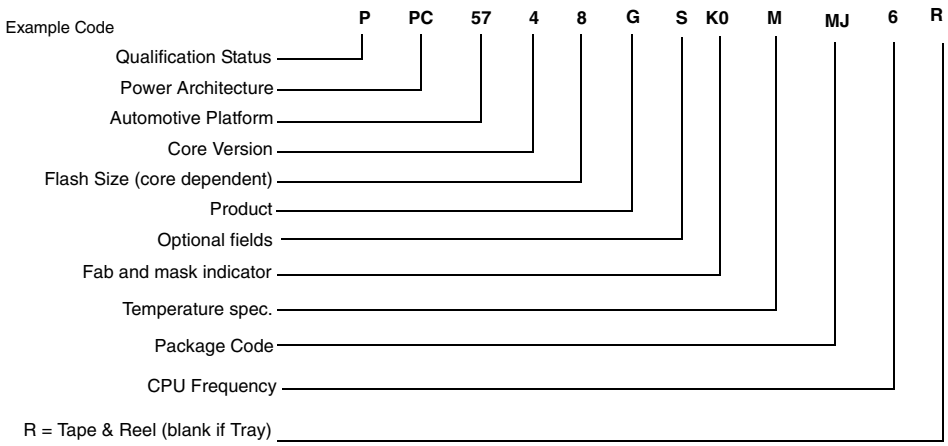
Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

3.2 Ordering Information



Qualification Status
P = Engineering samples
S = Automotive qualified

PC = Power Architecture

Automotive Platform
57 = Power Architecture in 55nm

Core Version
4 = e200z4 Core Version (highest core version in the case of multiple cores)

Flash Memory Size
6 = 3 MB
7 = 4 MB
8 = 6 MB

Product Version
C = Body Control Feature Set
G = Gateway Feature Set

Optional fields
Blank = Feature not available
S = HSM (Security Module)
F = CAN FD
B = Both HSM and CAN FD
T = HSM and 2nd Ethernet
G = CAN FD and 2nd Ethernet
H = HSM, CAN FD, and 2nd Eternet

Fab and mask version indicator
K=TSMC Fab
#=Version of maskset
0=0N65H
1=1N81M
0A=0N78S

Package Code
KU = 176 LQFP EP
MJ = 256 MAPBGA
MN = 324 MAPBGA

CPU Frequency
2 = Each z4 operates up to 120 MHz
6 = Each z4 operates up to 160 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Temperature spec.
C = -40.C to +85.C Ta
V = -40.C to +105.C Ta
M = -40.C to +125.C Ta

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[3, 4]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[5]	Decoupling pin for low power regulators[6]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[7]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 µF capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA. SeeThermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
  - Control of external NPN ballast transistor
  - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
VDD_LV	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x[1]	I/O Supply Voltage	4.5	5.5	V
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VSS_LV- 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x	VDD_HV_x + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VSS_LV - 0.3	0.4 * VDD_HV_x	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VSS_LV - 0.3	0.35*VDD_HV_x	V
Pull_IIH (pad_i_hv)	Weak Pullup Current Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2 * VDD_HV_x 0.1*VDD_HV_x	V

Table continues on the next page...

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{PORST}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{PORST}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD\_HV\_A}$	—	V
V_{IL}	Input low level	—	0.35 x $V_{DD\_HV\_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Table 30. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max	Units
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

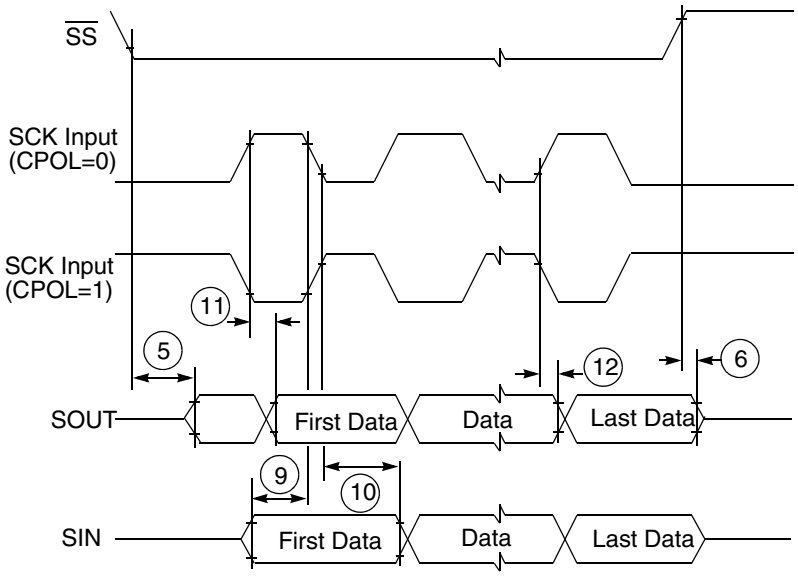


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

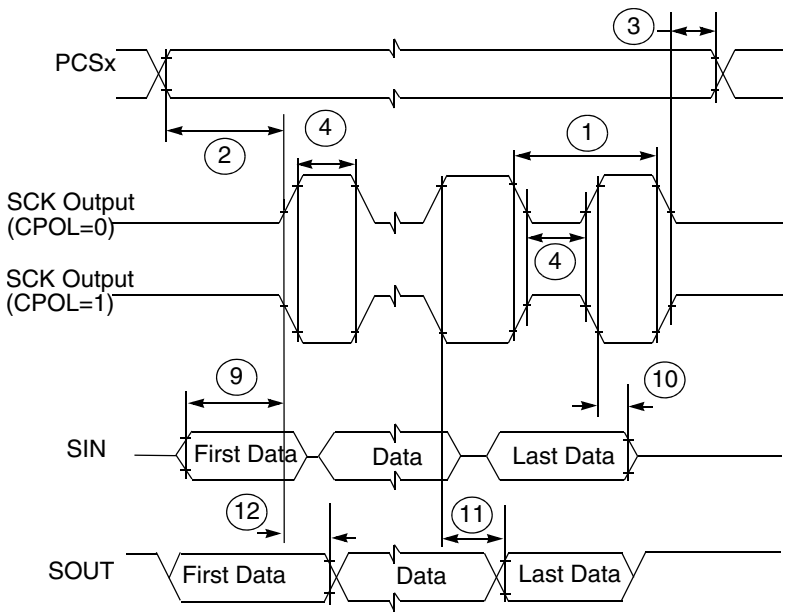
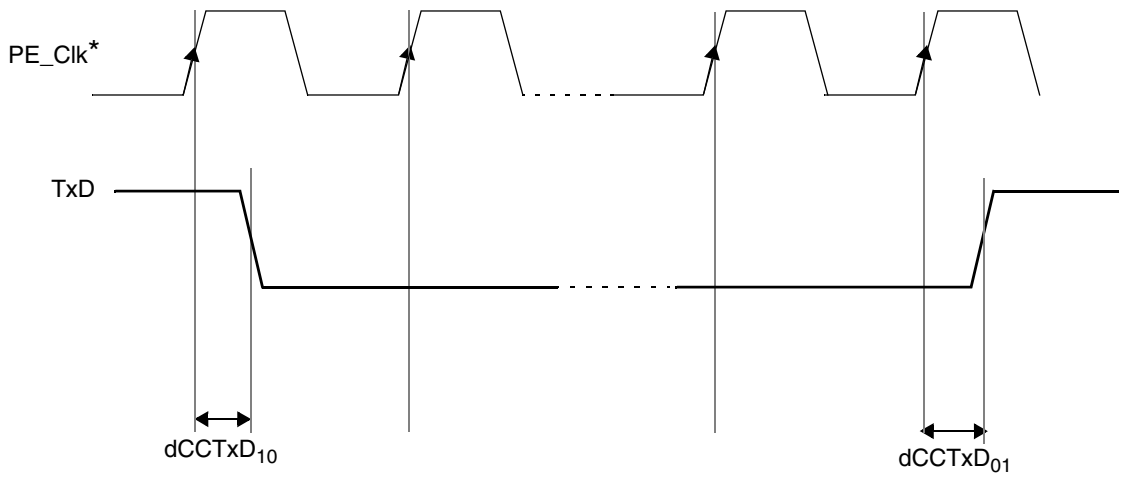


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

Table 39. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMII. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

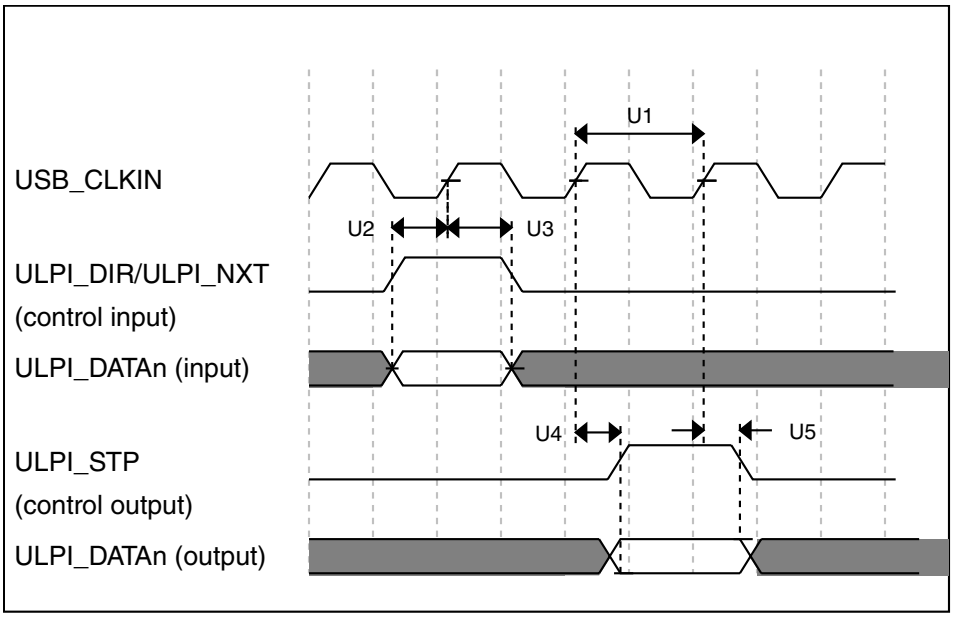


Figure 25. ULPI timing diagram

6.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 48. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

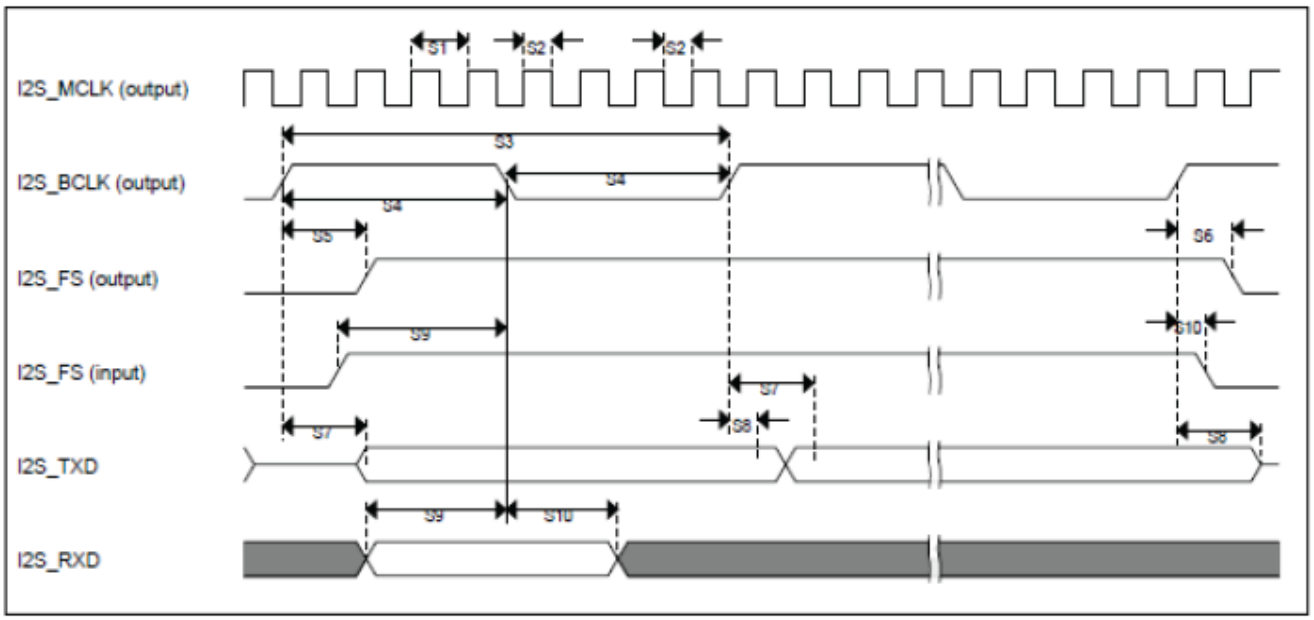


Figure 26. Master mode SAI Timing

Table 49. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

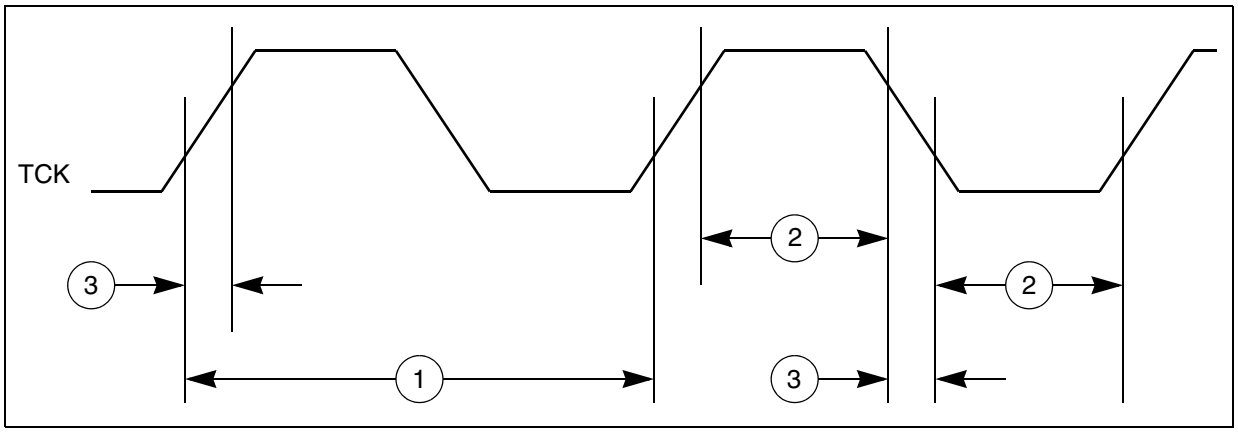


Figure 28. JTAG test clock input timing

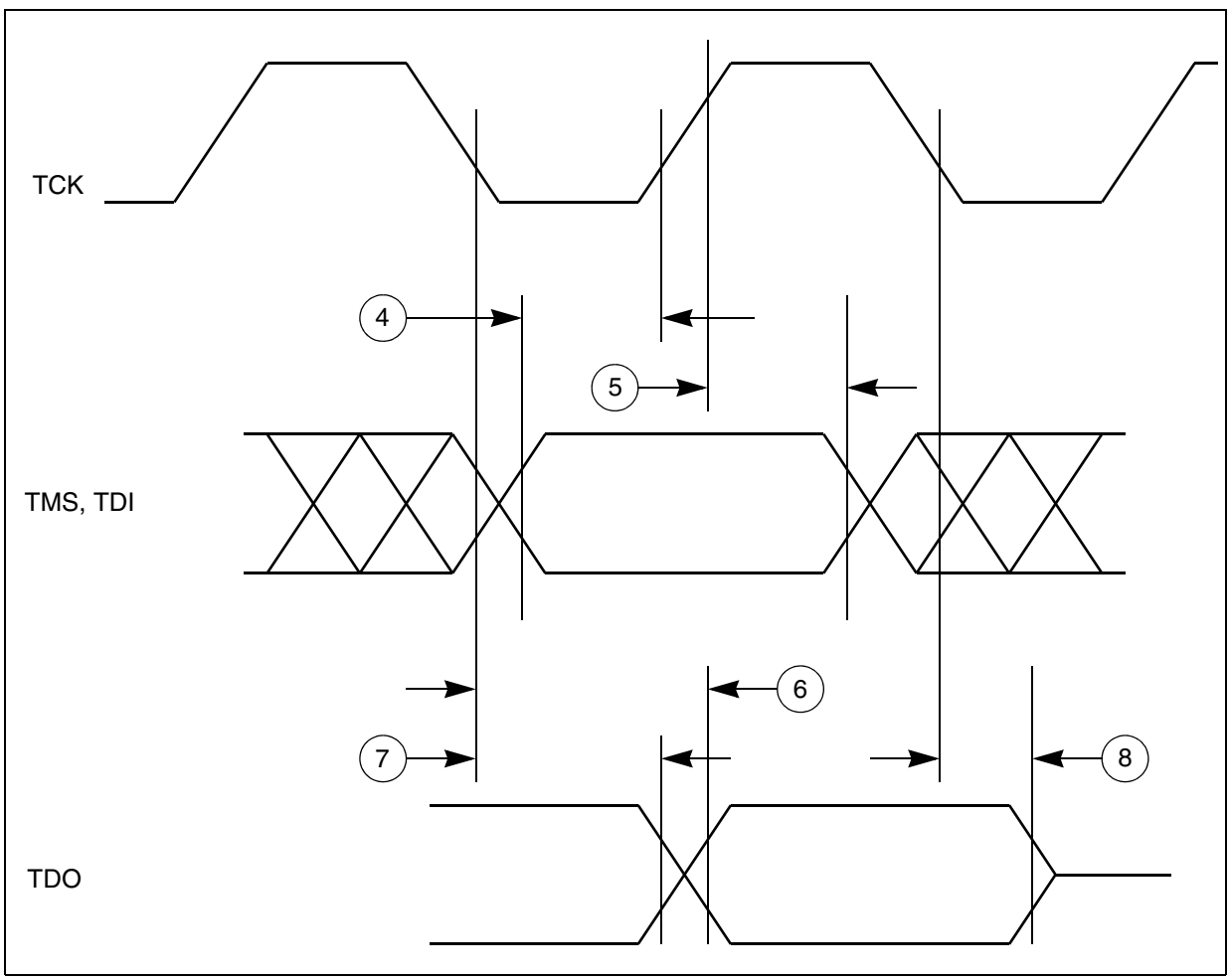


Figure 29. JTAG test access port timing

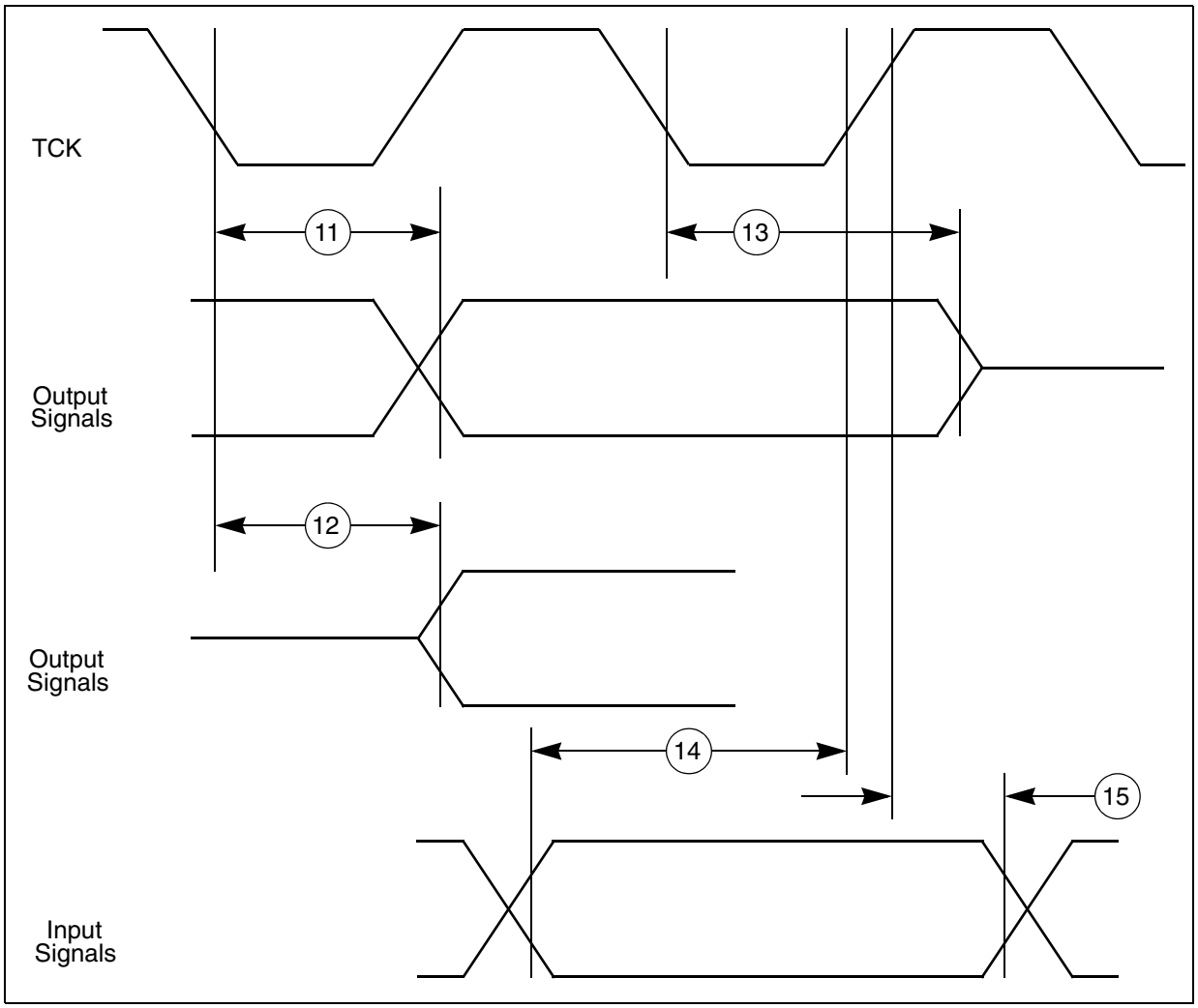


Figure 30. JTAG boundary scan timing

6.5.2 Nexus timing

Table 51. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

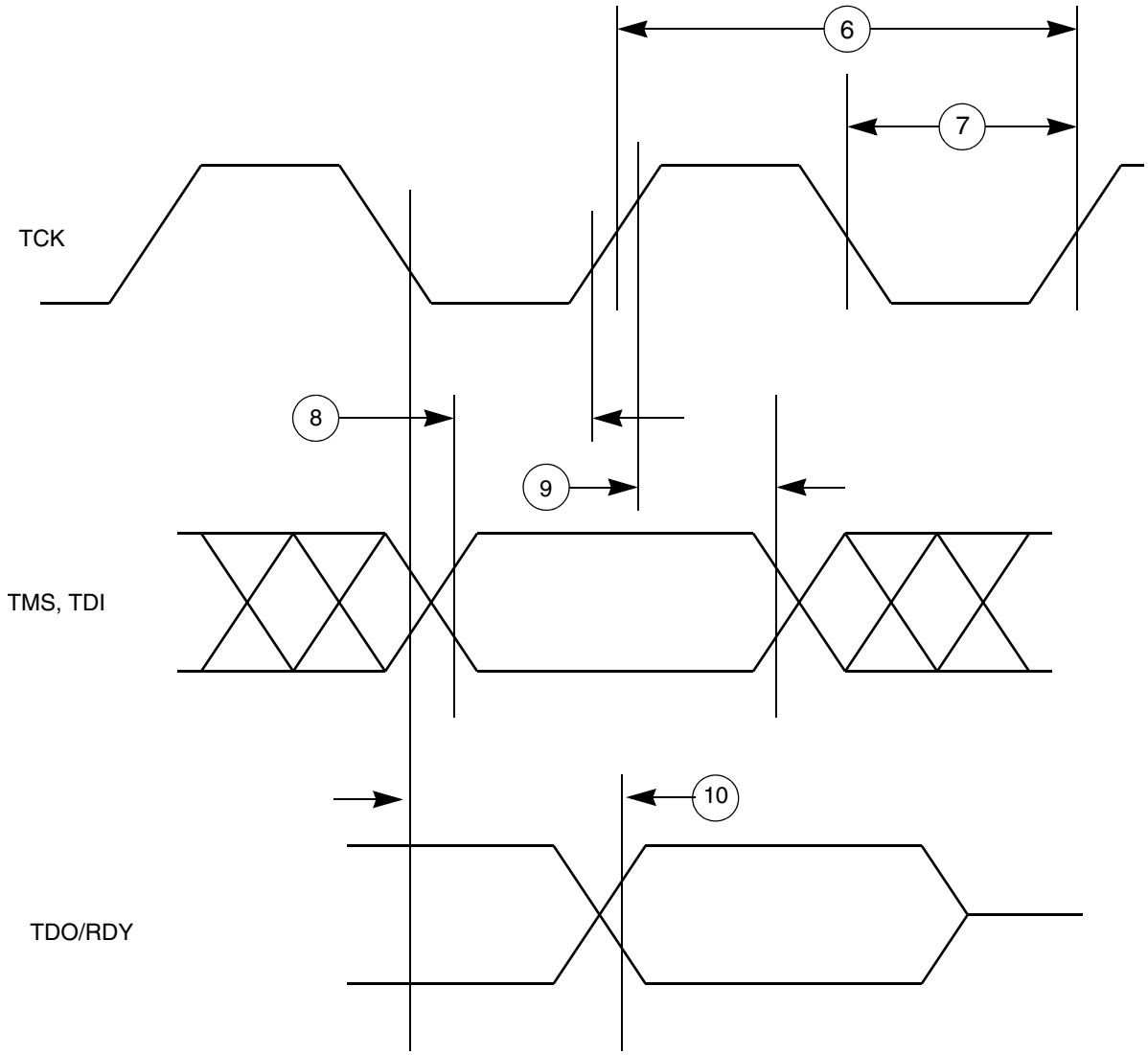


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

Table 54 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 54. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ [1]	Max	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T_{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T_{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T_{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

10.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 55. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	-	200	-	µs
BAF execution time (boot header at last location)	-	320	-	µs

10.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 54.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 54 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed row for symbol 'V_{SS_LV}' • Removed footnote from 'Max' column of symbols '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$'
		• In section: Recommended operating conditions • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V) • Added footnote to 'Conditions' cloumn • Updated footnote for 'Min' column • Removed footnote from symbols '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$' • Removed row for symbol: 'V_{SS_HV}' • Updated 'Parameter' column for symbol '$V_{DD\_HV\_ADC1\_REF}$' '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}' • Updated 'Min' columnn of symbol '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$' • Updated 'Parameter', 'Min' 'Max' column for symbol '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$' • Added footnote to symbol 'V_{DD_LV}' • Removed row for symbol 'V_{SS_LV}' • Added row for symbol '$V_{IN1\_CMP\_REF}$' and corresponding footnotes to the symbol • In section: Voltage regulator electrical characteristics • In table: Voltage regulator electrical specifications • Added note to symbol 'Cbe_fpreg' • In section: Voltage monitor electrical characteristics • In table: Voltage monitor electrical characteristics • Updated column 'Parameter', 'Min' and 'Max' (of fall/rise trimmed condition) for symbol '$V_{HVD\_LV\_cold}$' and '$V_{LVD\_IO\_A\_HI}$' • Updated column 'Parameter', 'Min' and 'Typ' (of fall/rise trimmed condition) for symbol) '$V_{LVD\_LV\_PD2\_hot}$', '$V_{LVD\_LV\_PD2\_cold\ LV}$' • Updated column 'Parameter' for symbol '$V_{LVD\_LV\_PD0\_hot}$' • Updated column 'Typ' and 'Max' (of fall/rise trimmed condition) for symbol) 'V_{LVD_FLASH}' • Updated footnote on symbol '$V_{LVD\_IO\_A\_LO}$' and '$V_{LVD\_IO\_A\_HI}$'
		• In section: Supply current characteristics • In table: Current consumption characteristics • Updated column 'Typ' for symbol 'I_{DD_FULL}' for temperature 85, 105, 125 • Updated column 'Typ' for symbol 'I_{DD_GWY}' for temperature 85, 105, 125 and column 'Max' for temperature 105 • Updated column 'Typ' for symbol 'I_{DD_BODY1}' for temperature 85, 105, 125 • Updated column 'Typ' for symbol 'I_{DD_BODY2}' for temperature 85, 105, 125 and 'Max' for temperature 125 • Added 'Typ' value for temperature 25 for symbol 'I_{DD_STOP}' • Updated column 'Typ' and 'Max' for symbol 'I_{DD_STOP}' for temperature 85, 105, 125 • In table: Low Power Unit (LPU) Current consumption characteristics • Updated column 'Typ' for symbol 'LPU_RUN' for tempeature 25 and 125 • Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_RUN' • Updated column 'Typ' for symbol 'LPU_STOP' for tempeature 25 and 125 • Added 'Typ' and 'Max' value for temperature 85 and 105 for symbol 'LPU_STOP' • In table: STANDBY Current consumption characteristics • Updated to have one STANDBY • In section: I/O parameters

Table continues on the next page...

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