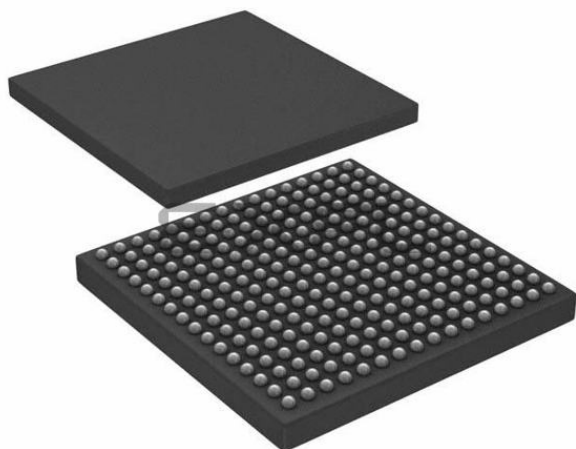




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5747gk1mmj6

- Timer
 - 16 Periodic Interrupt Timers (PITs)
 - Three System Timer Module (STM)
 - Four Software WatchDog Timers (SWT)
 - 96 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1) and 1149.7 (cJTAG)
- Security
 - Hardware Security Module (HSMv2)
 - Password and Device Security (PASS and TDM) supporting advanced censorship and life-cycle management
 - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
 - ISO26262 ASIL compliance
- Multiple operating modes
 - Includes enhanced low power operation

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison¹

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
CPUs	e200z4	e200z4	e200z4	e200z4	e200z4
	e200z2	e200z2	e200z4	e200z4	e200z4
			e200z2	e200z2	e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4
			e200z4	e200z4	e200z4
Maximum Operating Frequency ²	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)
	80MHz (z2)	80MHz (z2)	160MHz (z4)	160MHz (z4)	160MHz (z4)
			80MHz (z2)	80MHz (z2)	80MHz (z2)
Flash memory	4 MB	6 MB	3 MB	4 MB	6 MB
EEPROM support	32 KB to 128 KB emulated		32 KB to 192 KB emulated		
RAM	512 KB	768 KB			
ECC	End to End				
SMPU	24 entry		32 entry		
DMA	32 channels				
10-bit ADC	48 Standard channels 32 External channels				
12-bit ADC	16 Precision channels 16 Standard channels 32 External channels				
AnalogComparator	3				
BCTU	1				
SWT	2		4 ³		
STM	2		3		
PIT-RTI	16 channels PIT 1 channels RTI				
RTC/API	Yes				
Total Timer I/O ⁴	96 channels 16-bits				
LINFlexD	1 M/S, 15 M		1 M/S, 17 M		
FlexCAN	8 with optional CAN FD support				
DSPI/SPI	4 x DSPI				
	6 x SPI				

Table continues on the next page...

Table 1. MPC5748G Family Comparison¹ (continued)

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
I ² C	4				
SAI/I ² S	3				
FXOSC	8 - 40 MHz				
SXOSC	32 KHz				
FIRC	16 MHz				
SIRC	128 KHz				
FMPLL	Yes				
LPU	Yes				
FlexRay 2.1 (dual channel)	Yes, 128 MB				
MLB150	0			1	
USB 2.0 SPH	0			1	
USB 2.0 OTG	0			1	
SDHC	1				
Ethernet (RMII, MII + 1588, Multi queue AVB support)	Up to 2				
3 Port L2 Ethernet Switch	Optional				
CRC	1				
MEMU	2				
STCU	1				
HSM-v2 (security)	Optional				
Censorship	Yes				
FCCU	1				
Safety level	Specific functions ASIL-B certifiable				
User MBIST	Yes				
User LBIST	Yes				
I/O Retention in Standby	Yes				
GPIO ⁵	Up to 264 GPI and up to 246 GPIO				
Debug	JTAGC, cJTAG				
Nexus	Z4 N3+ Z2 N3+				
Packages	176 LQFP-EP 256 BGA, 324 BGA				

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterisation.
3. Additional SWT included when HSM option selected
4. Refer device datasheet and reference manual for information on to timer channel configuration and functions.

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 10. Current consumption characteristics (continued)

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
		T _a = 105 °C	—	114	206	mA
		T _a = 125 °C ⁴	—	131	277	mA
I _{DD_STOP}	STOP mode Operating current	T _a = 25 °C V _{DD_LV} = 1.25 V	—	11	—	mA
		T _a = 85 °C V _{DD_LV} = 1.25 V	—	19.8	105	
		T _a = 105 °C V _{DD_LV} = 1.25 V		29	145	
		T _a = 125 °C ⁴ V _{DD_LV} = 1.25 V	—	45	160	
I _{DD_HV_ADC_REF} ^{11, 12}	ADC REF Operating current	T _a = 25 °C 2 ADCs operating at 80 MHz V _{DD_HV_ADC_REF} = 3.6 V	—	200	400	μA
		T _a = 125 °C ⁴ 2 ADCs operating at 80 MHz V _{DD_HV_ADC_REF} = 5.5 V	—	200	400	
I _{DD_HV_ADCx} ¹²	ADC HV Operating current	T _a = 25 °C ADC operating at 80 MHz V _{DD_HV_ADC} = 3.6 V	—	1	2	mA
		T _a = 125 °C ⁴ ADC operating at 80 MHz V _{DD_HV_ADC} = 5.5 V	—	1.2	2	
I _{DD_HV_FLASH}	Flash Operating current during read access	T _a = 125 °C ⁴ 3.3 V supplies x MHz frequency	—	40	45	mA

1. The content of the Conditions column identifies the components that draw the specific current.
2. ALL Modules enabled at maximum frequency: 2 x e200Z4 @160 MHz, e200Z2 at 80 MHz, Platform @160MHz, DMA (SRAM to SRAM), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), ENET0 transmitting, MLB transmitting, FlexRay transmitting, USB-SPH transmitting (USB-OTG only clocked), 2 x I2C transmitting (rest clocked), 1 x SAI transmitting (rest clocked), ADC0 converting using BCTU triggers triggered through PIT (other ADC clocked), RTC running, 3 x STM running, 2 x DSPI transmitting (rest clocked), 2 x SPI transmitting (rest clocked), 4 x CAN state machines working(rest clocked), 9 x LINFlexD transmitting (rest clocked), 1 x eMIOS clocked (used OPWFMB mode) (Others clock gated), SDHC, 3 x CMP only clocked, FIRC, SIRC, FXOSC, SXOSC, PLL running. All others modules clock gated if not specifically mentioned. I/O supply current excluded.
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C.
4. T_j=150°C. Assumes T_a=125°C
 - Assumes maximum θJA. See [Thermal attributes](#)
5. Enabled Modules in Gateway mode: 2 x e200Z4 @160 MHz (Instruction and Data cache enabled), Platform @160MHz, e200Z2 at 80 MHz(Instruction cache enabled), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), ENET0 transmitting, MLB transmitting, FlexRay transmitting, USB-SPH Transmitting, USB-OTG clocked, 2 x I2C transmitting, (2 x I2C clock gated), 1 x SAI transmitting (2 x SAI clock gated), ADC0 converting in continuous mode (ADC1 clock gated), PIT clocked, RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(Other DSPS clock gated), 2 x SPI transmitting(Other SPIs clock gated), 4

Table 12. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions ¹	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	71	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	175	800	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	338	1725	
		$T_a = 125\text{ }^{\circ}\text{C}$	—	750	2775	
STANDBY1	STANDBY with 64K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	72	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	176	815	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	350	1775	
		$T_a = 125\text{ }^{\circ}\text{C}$	—	825	3000	
STANDBY2	STANDBY with 128K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	75	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	182	830	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	366	1825	
		$T_a = 125\text{ }^{\circ}\text{C}$	—	900	3250	
STANDBY3	STANDBY with 256K RAM	$T_a = 25\text{ }^{\circ}\text{C}$	—	80	—	μA
		$T_a = 85\text{ }^{\circ}\text{C}$	—	197	860	
		$T_a = 105\text{ }^{\circ}\text{C}$	—	400	1875	
		$T_a = 125\text{ }^{\circ}\text{C}$	—	975	3500	
STANDBY3	FIRC ON	$T_a = 25\text{ }^{\circ}\text{C}$	—	500	—	μA

1. The content of the Conditions column identifies the components that draw the specific current.

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts $\times$ ($n + 1$) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 13. ESD ratings

Symbol	Parameter	Conditions ¹	Class	Max value ²	Unit
$V_{\text{ESD(HBM)}}$	Electrostatic discharge (Human Body Model)	$T_A = 25\text{ }^{\circ}\text{C}$	H1C	2000	V

Table continues on the next page...

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
VDD_LV	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x ¹	I/O Supply Voltage	4.5	5.5	V
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	$0.7 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	$VSS_LV - 0.3$	$0.45 \cdot VDD_HV_x$	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x$		V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	$0.55 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	$VSS_LV - 0.3$	$0.4 \cdot VDD_HV_x$	V
Vhys	CMOS Input Buffer Hysteresis	$0.09 \cdot VDD_HV_x$		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	$0.65 \cdot VDD_HV_x$	$VDD_HV_x + 0.3$	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	$VSS_LV - 0.3$	$0.35 \cdot VDD_HV_x$	V
Pull_IIH (pad_i_hv)	Weak Pullup Current Low	23		μA
Pull_IIH (pad_i_hv)	Weak Pullup Current High		82	μA
Pull_IIL (pad_i_hv)	Weak Pulldown Current ³ Low	40		μA
Pull_IIL (pad_i_hv)	Weak Pulldown Current ² High		130	μA
Pull_Ioh	Weak Pullup Current ⁴	30	80	μA
Pull_Iol	Weak Pulldown Current ⁵	30	80	μA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	μA
Voh	Output High Voltage ⁶	$0.8 \cdot VDD_HV_x$	—	V
Vol	Output Low Voltage ⁷ Output Low Voltage ⁸	—	$0.2 \cdot VDD_HV_x$ $0.1 \cdot VDD_HV_x$	V

Table continues on the next page...

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

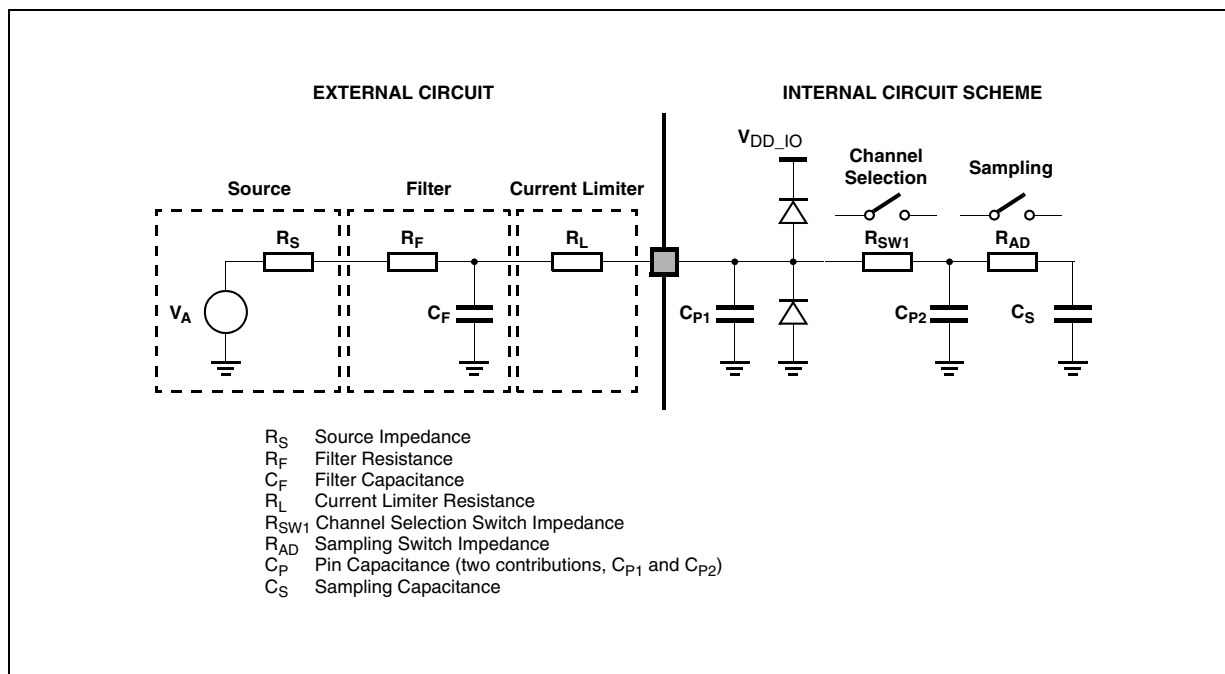


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 20. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK ² frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time ⁴	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time $t_{sample} + t_{conv}$ (for standard and extended channels)	80 MHz	1.5 ⁵	—	—	μ s
	Total Conversion time $t_{sample} + t_{conv}$ (for precision channels)		1	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1} ⁶	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2} ⁶	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1} ⁶	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	k Ω
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	μA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage ¹	-42	—	42	mV
V_H	Analog comparator hysteresis ² - CR0[HYSTCTR] = 00 - CR0[HYSTCTR] = 01 - CR0[HYSTCTR] = 10 - CR0[HYSTCTR] = 11	—	1	25	mV
		—	20	50	mV
		—	40	70	mV
		—	60	105	mV
		—	—	—	—
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) ^{1, 3}	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) ^{1, 3}	—	5	21	μs
	Analog comparator initialization delay, High speed mode ⁴	—	4		μs
	Analog comparator initialization delay, Low speed mode ⁴	—	100		μs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	μA
	5V Reference Voltage	—	10	16	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ⁵
DNL	6-bit DAC differential non-linearity	-0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00

2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}-0.6V$

3. Full swing = V_{IH} , V_{IL}

4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

5. 1 LSB = $V_{reference}/64$

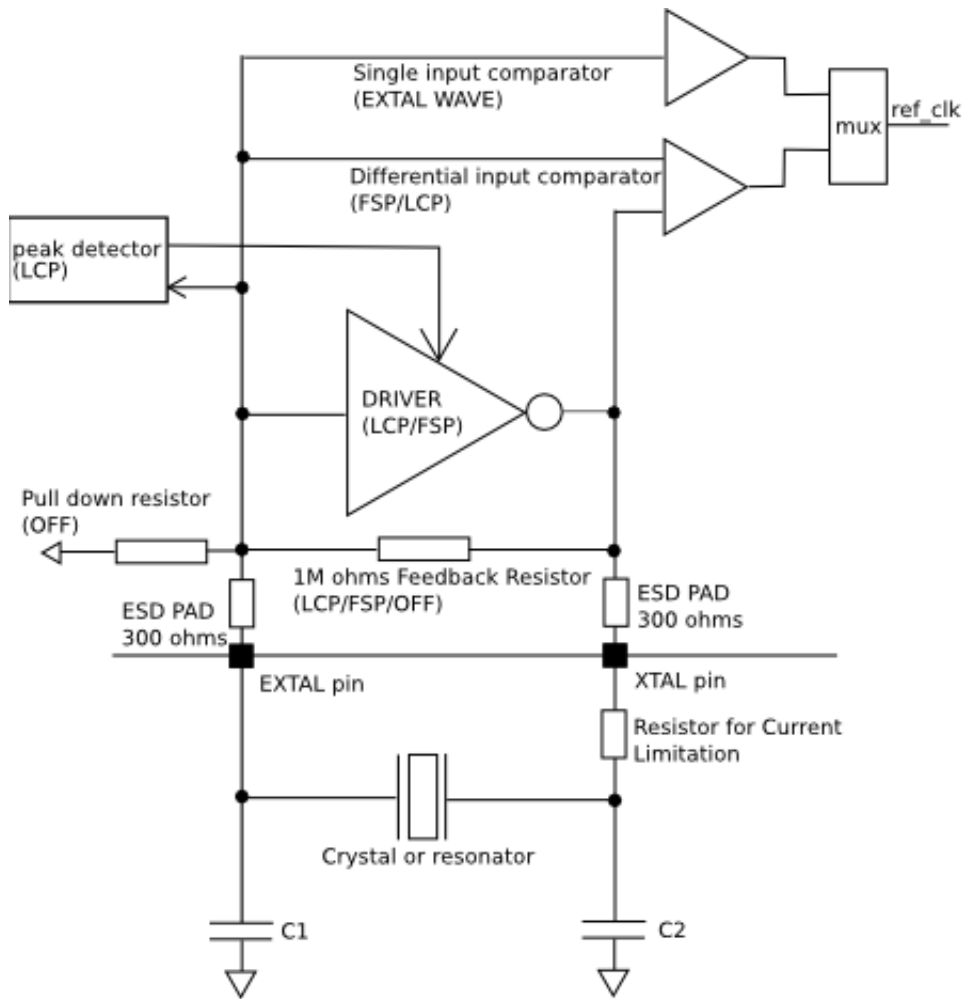


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V _{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V _{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t _{cst}	Crystal Start-up Time ^{1, 2}				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F _{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
T _{startup}	Startup time	—		—	1.5	us
T _{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T _{LTJIT}	Long term jitter		—	—	0.2	%

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

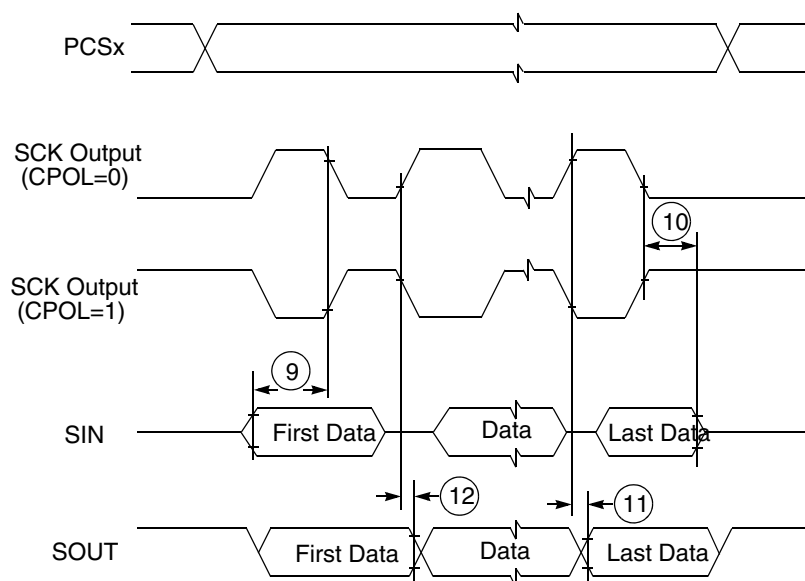


Figure 9. DSPI classic SPI timing — master, CPHA = 1

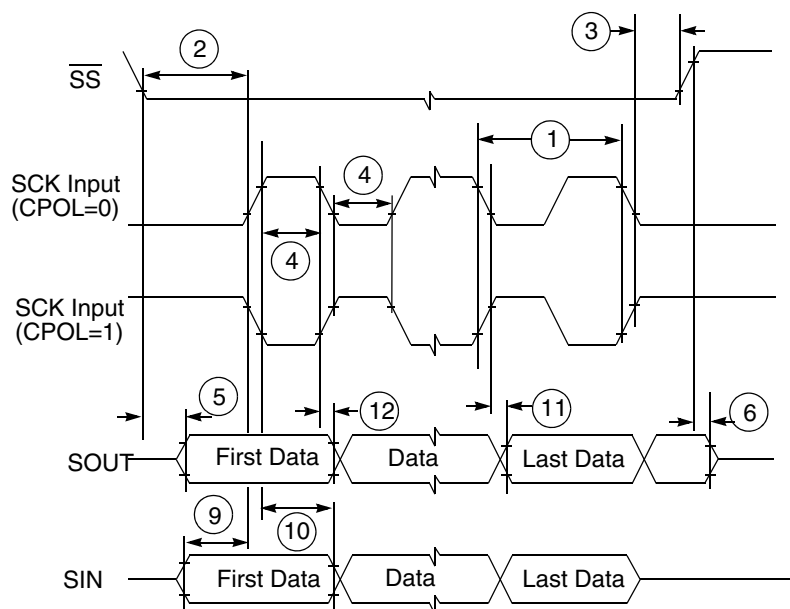


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

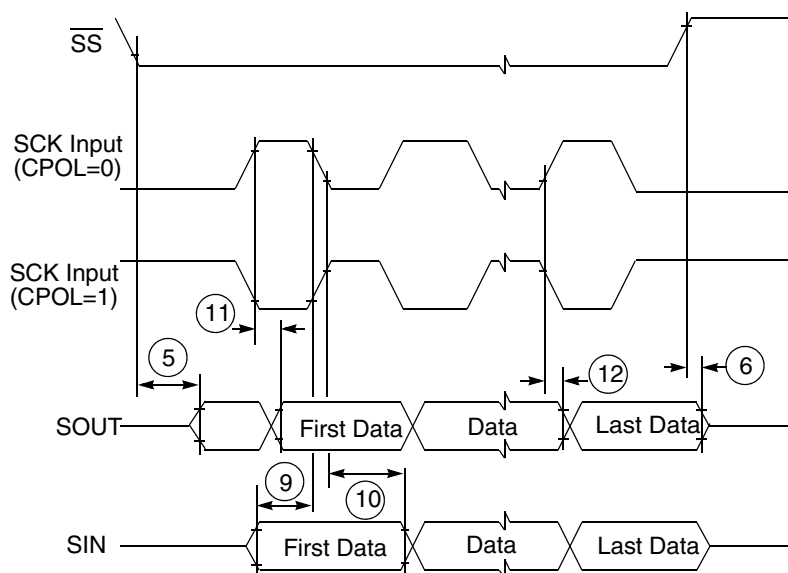


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

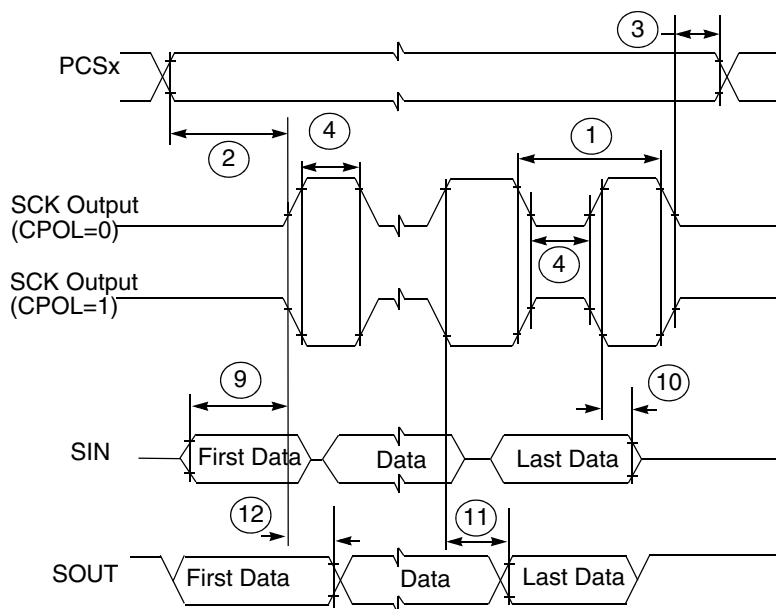


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMII. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

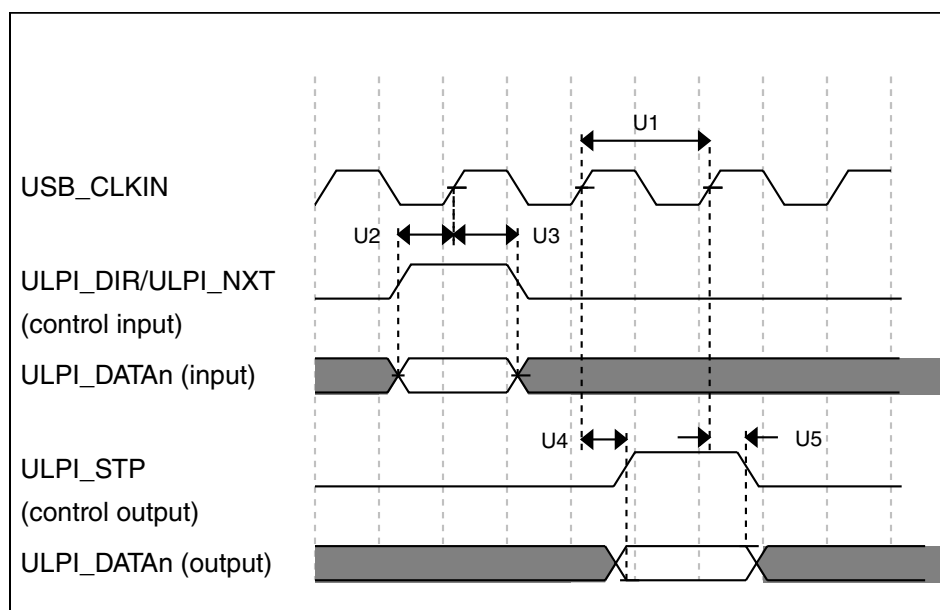


Figure 25. ULPI timing diagram

6.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 48. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

[Table 54](#) specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in [Reset sequence description](#).

Table 54. RESET sequences

No.	Symbol	Parameter	T _{Reset}			Unit
			Min	Typ ¹	Max	
1	T _{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T _{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T _{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T _{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T _{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

10.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 55. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	-	200	-	μs
BAF execution time (boot header at last location)	-	320	-	μs

10.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in [Table 54](#).

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in [Table 54](#) are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

Reset sequence

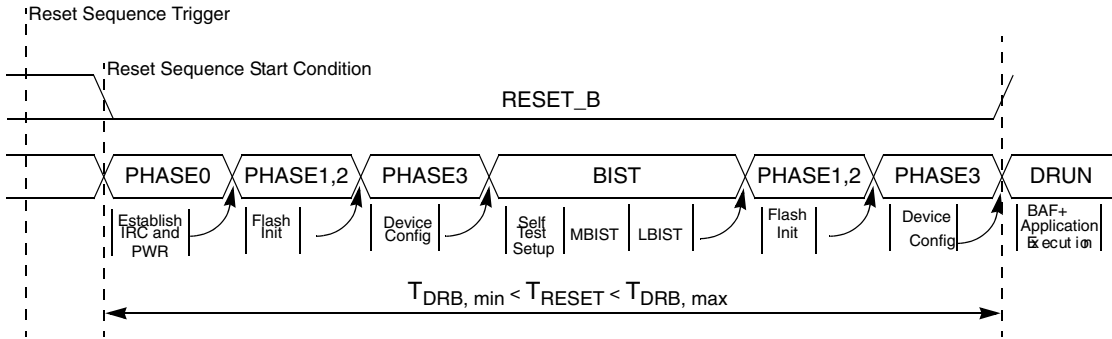


Figure 35. Destructive reset sequence, BIST enabled

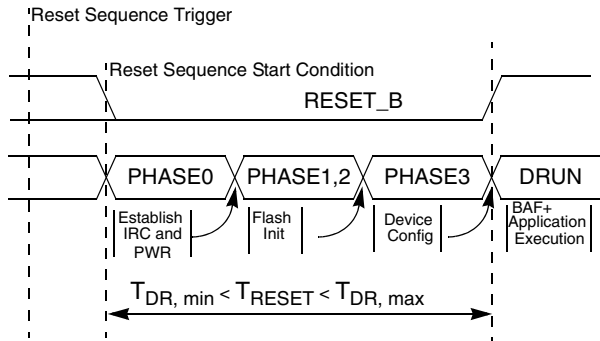


Figure 36. Destructive reset sequence, BIST disabled

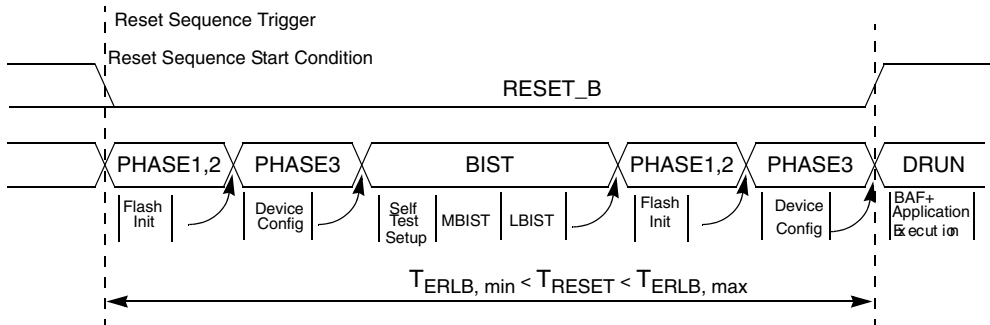


Figure 37. External reset sequence long, BIST enabled

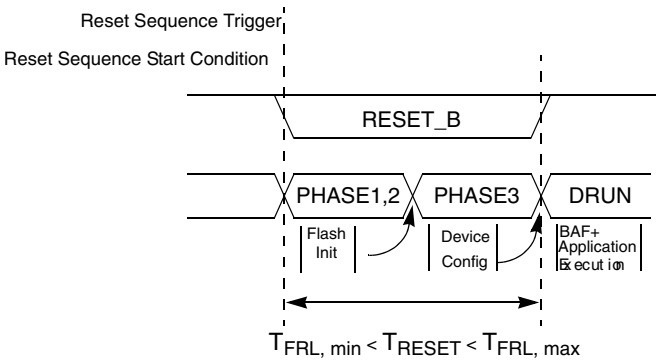


Figure 38. Functional reset sequence long

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- Revised Electromagnetic Interference (EMI) characteristics section - Revised DC electrical specifications @ 3.3V Range table for naming conventions. - Revised DC electrical specifications @ 5 V Range table for naming conventions - Deleted MLB 6-pin Electrical Specifications - Removed PORST characteristics from Functional reset pad electrical characteristics table - Added section PORST electrical characteristics - Revised Input impedance and ADC accuracy section to remove SNR, THD, SINAD, ENOB, - Revised 32 kHz oscillator electrical specifications table to remove 'Vpp' row. - Updated 16 MHz RC Oscillator electrical specifications table for statuptime, cycle to cycle jitter, and lonf term jitter - Updated 128 KHz Internal RC oscillator electrical specifications table. - Updated PLL electrical specifications table - Added Jitter Calculation table - Added Percentage of Sample exceeding specified value of jitter table
		- Revised Memory interfaces section - Revised Communication interfaces section - Updated note - Added Continuous SCK timing table - Added DSPI high speed mode I/Os table - Updated input transition value in section MLB 3-pin interface electrical specifications - Deleted MLB 6-pin interface DC characteristics section - Deleted MLB 6-pin interface AC characteristics section - Updated JTAG pin AC electrical characteristics table - Revised table under Thermal attributes section - Updated Obtaining package dimensions section for Freescale Document numbers
3	12 May 2015	- Editorial updates throughout the sections - Renamed '176 LQFP' package to '176 LQFP-EP' - Added following sections: - Block diagram - Family comparison - Ordering Information - In table: Absolute maximum ratings as follows: - Removed row for symbol: 'V_{SS_HV}' - Added symbol: 'V_{DD_LV}' - Updated 'Max' column for symbol 'V_{INA}' - Added footnote to 'Conditions' column - Removed footnote from 'Max' column - In section: Recommended operating conditions - Added opening text: "The following table describes the operating conditions ... " - Added note: "V_{DD_HV_A}, V_{DD_HV_B} and V_{DD_HV_C} are all ... " - In table: Recommended operating conditions (V_{DD_HV_x} = 3.3 V) - Added footnote to 'Conditions' cloumn - Updated footnote for 'Min' column - Removed footnote from symbols 'V_{DD_HV_A}', 'V_{DD_HV_B}', and 'V_{DD_HV_C}' - Removed row for symbol: 'V_{SS_HV}' - Updated 'Parameter' column for symbol 'V_{DD_HV_FLTA}', 'V_{DD_HV_ADC1_REF}', 'V_{DD_LV}' - Updated 'Min' column for symbol 'V_{DD_HV_ADC0}' and 'V_{DD_HV_ADC1}' - Updated 'Parameter' 'Min' 'Max' column for symbol 'V_{SS_HV_ADC0}' and 'V_{SS_HV_ADC1}' - Added footnote to symbol 'V_{DD_LV}' - Removed footnote from symbol 'V_{IN1_CMP_REF}'

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		- In table: Functional Pad AC Specifications @ 3.3 V Range - Updated values for symbol 'pad_sr_hv (output)' - In table: DC electrical specifications @ 3.3V Range - Updated values for VDD_HV_x, Vih, Vhys - Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys - In table: Functional Pad AC Specifications @ 5 V Range - Updated values for symbol 'pad_sr_hv (output)' - In table DC electrical specifications @ 5 V Range - Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		- In section: PORST electrical specifications - In table: PORST electrical specifications - Updated 'Min' value for $W_{NF\text{PORST}}$ - Corrected 'Unit' for V_{IH} and V_{IL} - In section: Peripheral operating requirements and behaviours - Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) - In section: Analogue Comparator (CMP) electrical specifications - In table: Comparator and 6-bit DAC electrical specifications - Updated 'Max' value of $I_{DDL\text{S}}$ - Updated 'Min' and 'Max' for V_{AIO} and DNL - Updated 'Description' 'Min' 'Max' of V_H - Updated row for tDHS - Added row for tDLS - Removed row for VCMPOh and VCMPOI - In section: Clocks and PLL interfaces modules - Revised table: Main oscillator electrical characteristics - In table: 16 MHz RC Oscillator electrical specifications - Updated 'Max' of Tstartup - In table: 128 KHz Internal RC oscillator electrical specifications - Removed Uncalibrated 'Condition' for Fosc - Updated 'Min' and 'Max' of Calibrated Fosc - Updated 'Temperature dependence' and 'Supply dependence' - In table: PLL electrical specifications - Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption - Removed 'Typ' value of Duty Cycle at pllclkout - Removed 'Min' from calibration mode of Lock Time - In table: Jitter calculation - Added 1 Sigma Random Jitter value for Long term jitter
		- In section Flash read wait state and address pipeline control settings - Revised table: Flash Read Wait State and Address Pipeline Control - Removed section: On-chip peripherals - Added section: 'Reset sequence'
Rev4	Feb 10 2017	- Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics - Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics - Updated SIUL2_MSCRn[Src 1:0]=11 @25pF max value; SIUL2_MSCRn[Src 1:0]=11 @50pF min value; SIUL2_MSCRn[Src 1:0]=10 @25pF min and max values in AC specifications @ 3.3 V Range

Table continues on the next page...