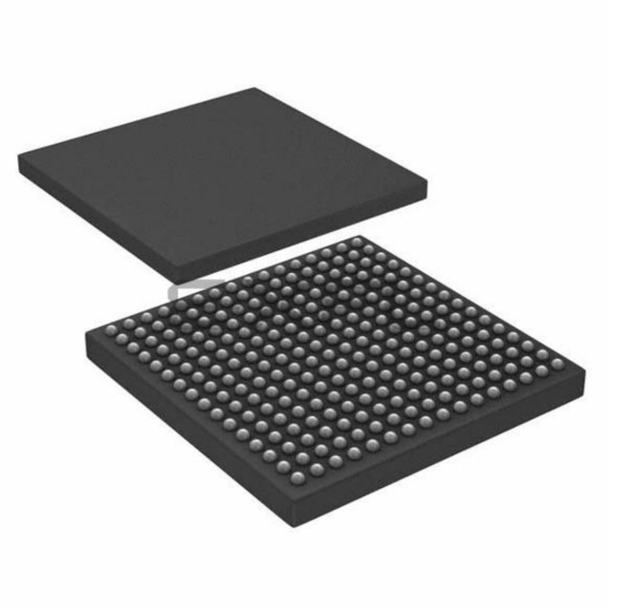
NXP USA Inc. - SPC5748CK1MMJ6R Datasheet



Details	
Product Status	Active
Core Processor	e200z2, e200z4
Core Size	32-Bit Dual-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5748ck1mmj6r

1 Block diagram

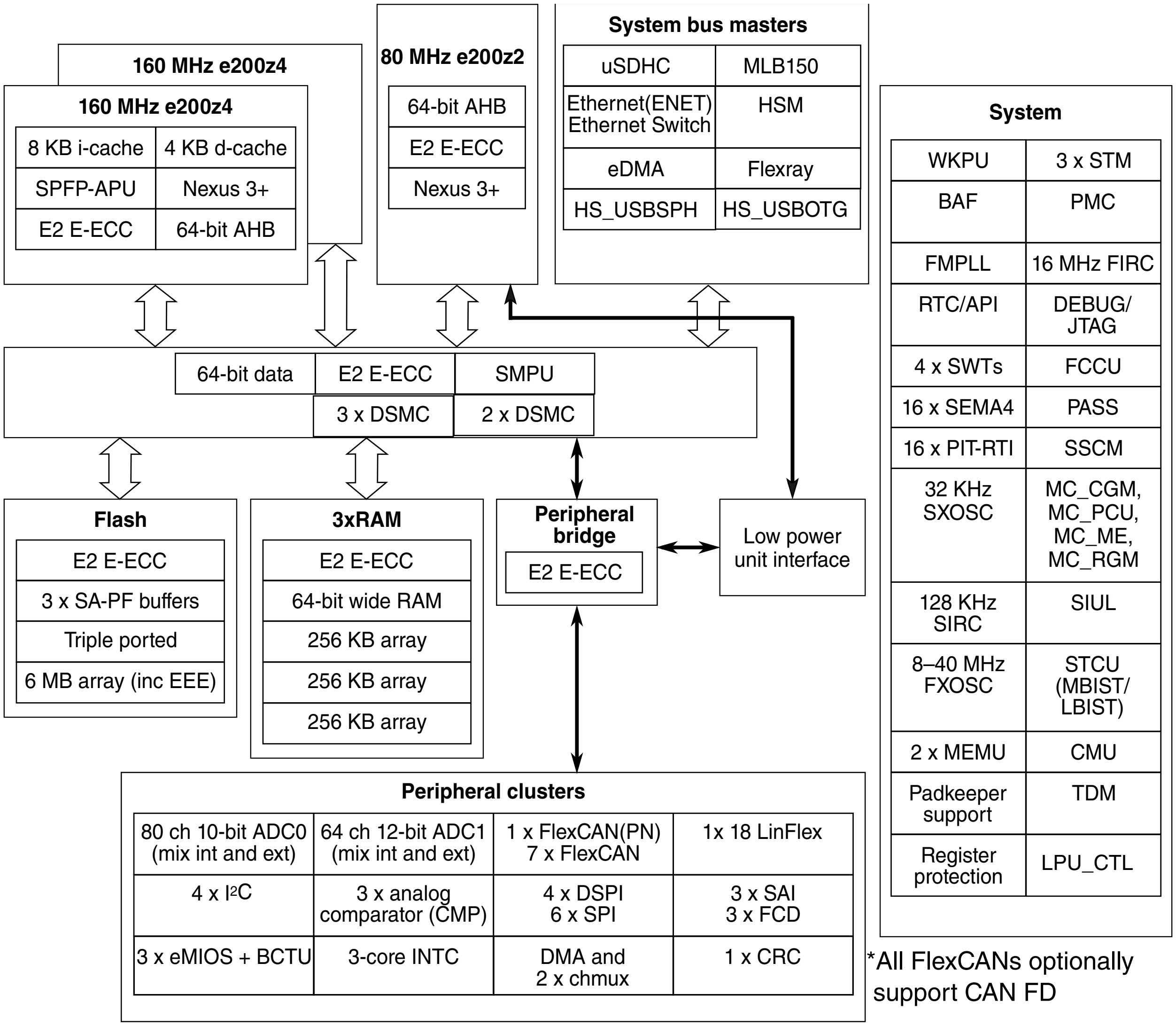


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison[1]

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
CPUs	e200z4 e200z2	e200z4 e200z2	e200z4 e200z4 e200z2	e200z4 e200z4 e200z2	e200z4 e200z4 e200z2
FPU	e200z4	e200z4	e200z4 e200z4	e200z4 e200z4	e200z4 e200z4
Maximum Operating Frequency[2]	160MHz (z4) 80MHz (z2)	160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)
Flash memory	4 MB	6 MB	3 MB	4 MB	6 MB
EEPROM support	32 KB to 128 KB emulated		32 KB to 192 KB emulated		
RAM	512 KB	768 KB			
ECC	End to End				
SMPU	24 entry		32 entry		
DMA	32 channels				
10-bit ADC	48 Standard channels 32 External channels				
12-bit ADC	16 Precision channels 16 Standard channels 32 External channels				
AnalogComparator	3				
BCTU	1				
SWT	2		4[3]		
STM	2		3		
PIT-RTI	16 channels PIT 1 channels RTI				
RTC/API	Yes				
Total Timer I/O[4]	96 channels 16-bits				
LINFlexD	1 M/S, 15 M		1 M/S, 17 M		
FlexCAN	8 with optional CAN FD support				
DSPI/SPI	4 x DSPI 6 x SPI				

Table continues on the next page...

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	3.6	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[5, 6]	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
  - Control of external NPN ballast transistor
  - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

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[1] BCP56, MCP68 and MJD31are guaranteed ballasts.

Table 15. DC electrical specifications @ 3.3V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
	Output Low Voltage[8]		0.1 *VDD_HV_x	
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10)	10.5	60	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 16. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 17. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
VDD_LV	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x[1]	I/O Supply Voltage	4.5	5.5	V
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VSS_LV- 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x	VDD_HV_x + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VSS_LV - 0.3	0.4 * VDD_HV_x	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VSS_LV - 0.3	0.35*VDD_HV_x	V
Pull_IIH (pad_i_hv)	Weak Pullup Current Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2 * VDD_HV_x 0.1*VDD_HV_x	V

Table continues on the next page...

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11)	38	132	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11)	48	220	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10)	19	66	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

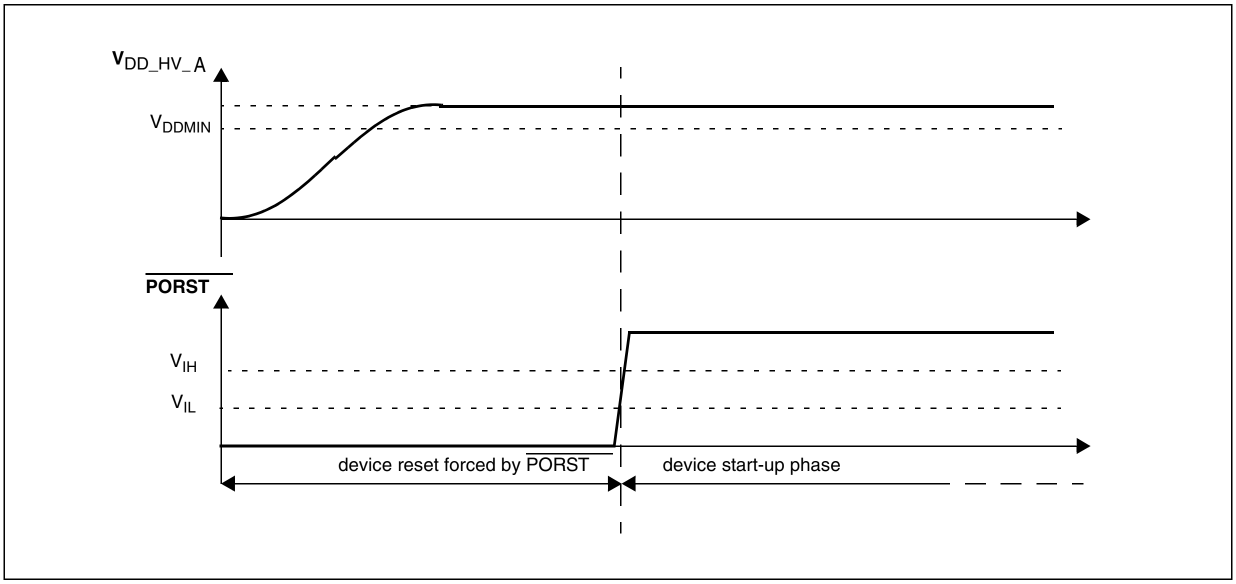

Figure 3. Start-up reset requirements

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD\_HV\_A}$	—	V
V_{IL}	Input low level	—	0.35 x $V_{DD\_HV\_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2 - 10$	$t_{SCK}/2 + 10$	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	SS inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8[1]	—	

Table continues on the next page...

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

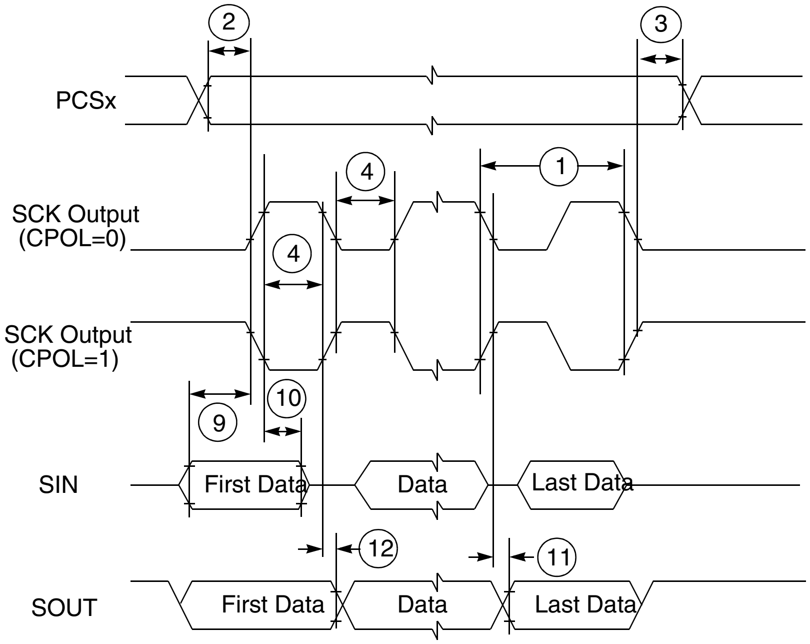

Figure 8. DSPI classic SPI timing — master, CPHA = 0

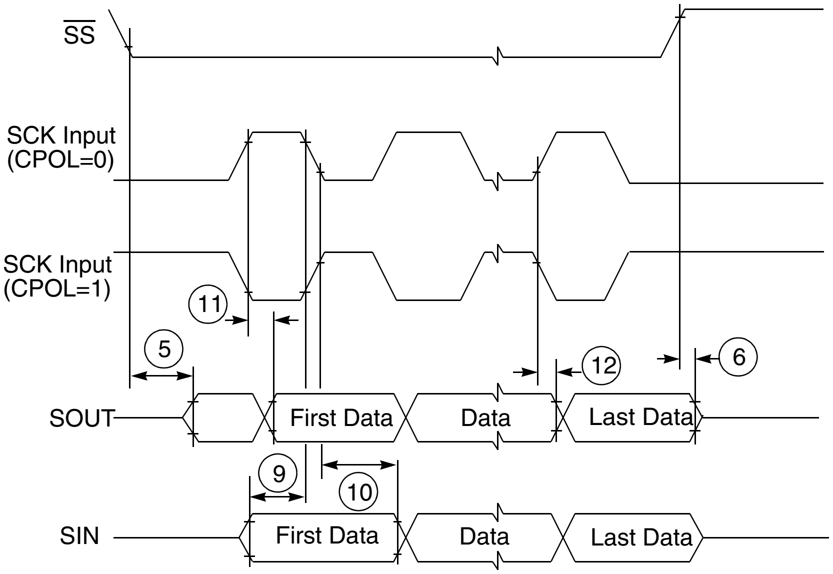

Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

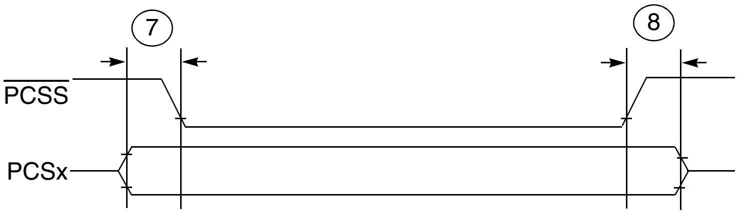

Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

6.4.3 uSDHC specifications

Table 41. uSDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
	Card input clock				
SD1	fpp	Clock frequency (Identification mode)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (SD\SDIO high speed)	0	40	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f_{OD}	Clock frequency (MMC full speed)	0	40	MHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	6.5	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

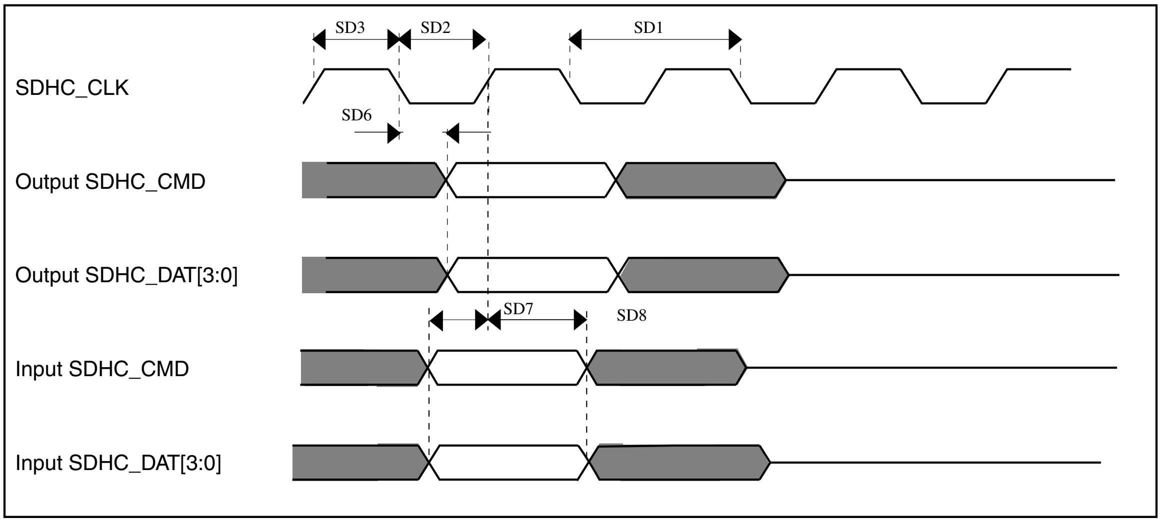

Figure 21. uSDHC timing

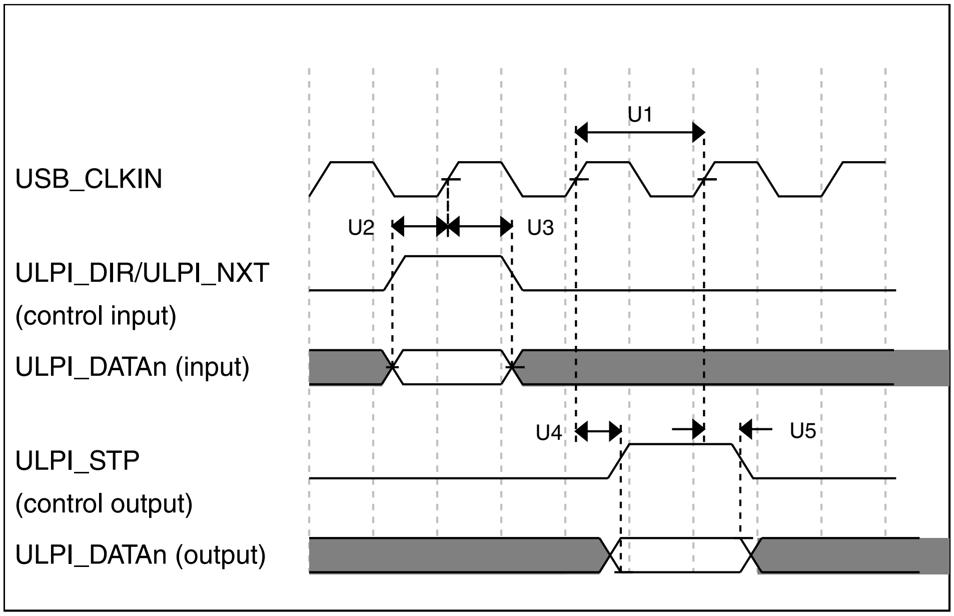

Figure 25. ULPI timing diagram

6.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 48. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

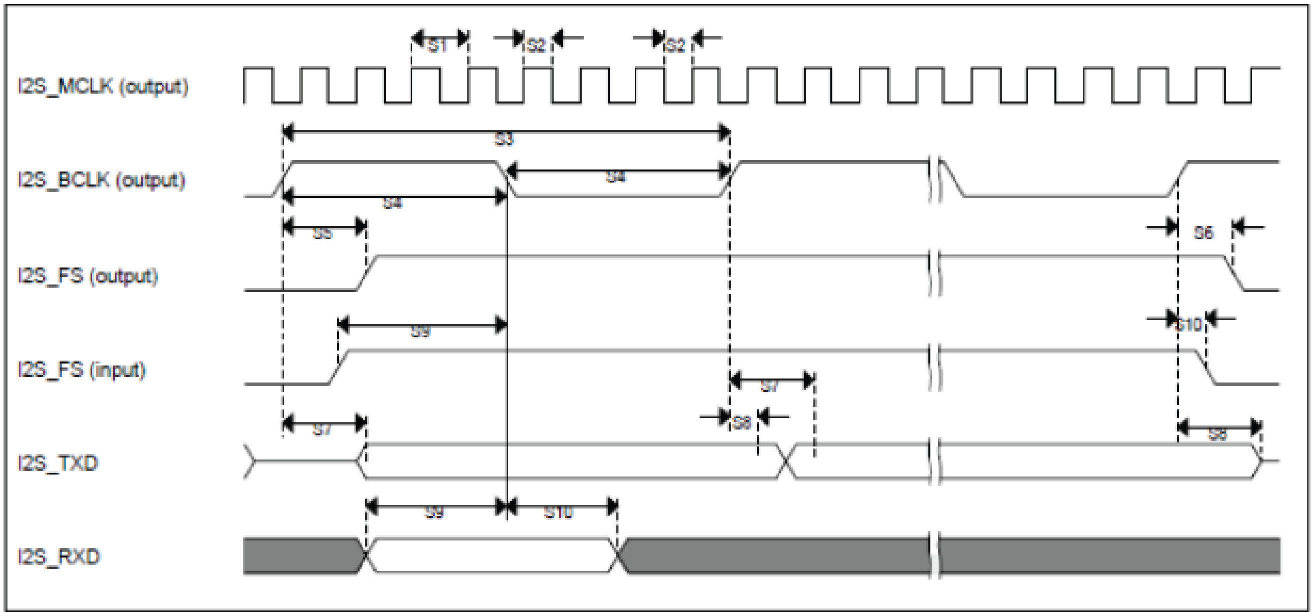

Figure 26. Master mode SAI Timing

Table 49. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

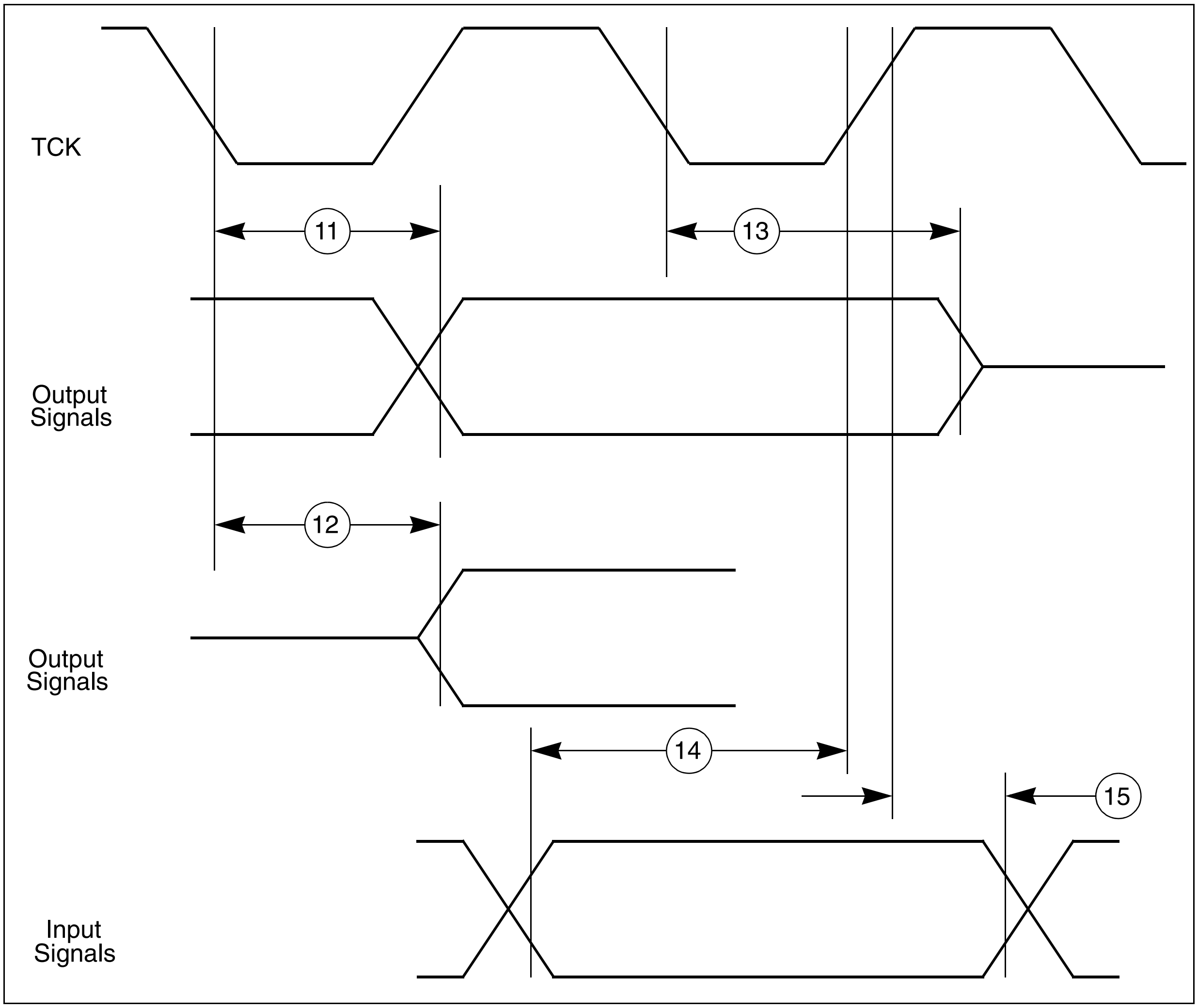

Figure 30. JTAG boundary scan timing

6.5.2 Nexus timing

Table 51. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

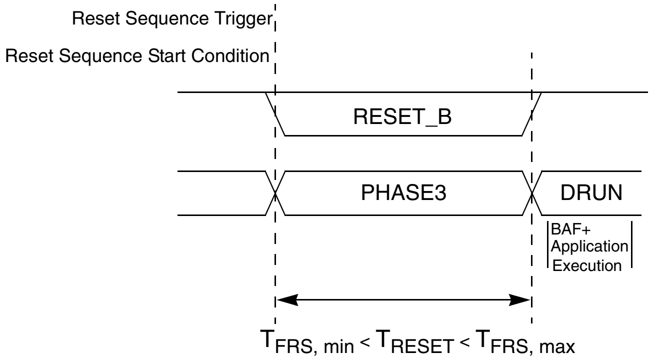

Figure 39. Functional reset sequence short

The reset sequences shown in Figure 38 and Figure 39 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 56. Revision History

Rev. No.	Date	Substantial Changes
1	14 March 2013	Initial Release
1.1	16 May 2013	Updated Pinouts section

2	22 May 2014	• Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet
		• Revised the feature list.
		• Revised Introduction section to remove classification information.
		• Updated optional information in the ordering information figure.
		• Revised Absolute maximum rating section:
		  • Removed category column from table
		  • Added footnote at Ta
		• Revised Recommended operating conditions section
		  • Added notes
		  • Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V)
		  • Updated table: Recommended operating conditions (VDD_HV_x = 5 V)
		• Revised Voltage regulator electrical characteristics
		  • Updated text describing bipolar transistors
		  • Updated figure: Voltage regulator capacitance connection
		  • Updated table: Voltage regulator electrical specifications
		  • Removed Brownout information
		• Revised Voltage monitor electrical characteristics table

		• Revised Supply current characteristics section
		  • Updated table: Current consumption characteristics
		  • Updated table: Low Power Unit (LPU) Current consumption characteristics
		  • STANDBY Current consumption characteristics

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Revised Electromagnetic Interference (EMI) characteristics section • Revised DC electrical specifications @ 3.3V Range table for naming convections. • Revised DC electrical specifications @ 5 V Range table for naming conventions • Deleted MLB 6-pin Electrical Specifications • Removed PORST characteristics from Functional reset pad electrical characteristics table • Added section PORST electrical characteristics • Revised Input impedance and ADC accuracy section to remove SNR, THD, SINAD, ENOB, • Revised 32 kHz oscillator electrical specifications table to remove 'Vpp' row. • Updated 16 MHz RC Oscillator electrical specifications table for statuptime, cycle to cycle jitter, and lonf term jitter • Updated 128 KHz Internal RC oscillator electrical specifications table. • Updated PLL electrical specifications table • Added Jitter Calculation table • Added Percentage of Sample exceeding specified value of jitter table

		• Revised Memory interfaces section
		• Revised Communication interfaces section
		    • Updated note
		    • Added Continuous SCK timing table
		    • Added DSPI high speed mode I/Os table
		• Updated input transition value in section MLB 3-pin interface electrical specifications
		• Deleted MLB 6-pin interface DC characteristics section
		• Deleted MLB 6-pin interface AC characteristics section
		• Updated JTAG pin AC electrical characteristics table
		• Revised table under Thermal attributes section
		• Updated Obtaining package dimensions section for Freescale Document numbers

3	12 May 2015	• Editorial updates throughout the sections
		• Renamed '176 LQFP' package to '176 LQFP-EP'
		• Added following sections:
		    • Block diagram
		    • Family comparison
		    • Ordering Information
		• In table: Absolute maximum ratings as follows:
		    • Removed row for symbol: 'V_{SS_HV}'
		    • Added symbol: 'V_{DD_LV}'
		    • Updated 'Max' column for symbol 'V_{INA}'
		    • Added footnote to 'Conditions' column
		    • Removed footnote from 'Max' column
		• In section: Recommended operating conditions
		    • Added opening text: "The following table describes the operating conditions ... "
		    • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... "
		    • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)
		        • Added footnote to 'Conditions' cloumn
		        • Updated footnote for 'Min' column
		        • Removed footnote from symbols '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$'
		        • Removed row for symbol: 'V_{SS_HV}'
		        • Updated 'Parameter' column for symbol '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}'
		        • Updated 'Min' column for symbol '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$'
		        • Updated 'Parameter' 'Min' 'Max' column for symbol '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$'
		        • Added footnote to symbol 'V_{DD_LV} '
		        • Removed footnote from symbol '$V_{IN1\_CMP\_REF}$'

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Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In table: Functional Pad AC Specifications @ 3.3 V Range • Updated values for symbol 'pad_sr_hv (output)' • In table: DC electrical specifications @ 3.3V Range • Updtaed values for VDD_HV_x, Vih, Vhys • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys • In table: Functional Pad AC Specifications @ 5 V Range • Updated values for symbol 'pad_sr_hv (output)' • In table DC electrical specifications @ 5 V Range • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		• In section: PORST electrical specifications • In table: PORST electrical specifications • Updated 'Min' value for $W_{NFPORST}$ • Corrected 'Unit' for V_{IH} and V_{IL} • In section: Peripheral operating requirements and behaviours • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit) • In section: Analogue Comparator (CMP) electrical specifications • In table: Comparator and 6-bit DAC electrical specifications • Updated 'Max' value of I_{DDLS} • Updated 'Min' and 'Max' for V_{AIO} and DNL • Updated 'Descripton' 'Min' 'Max' od V_H • Updated row for tDHS • Added row for tDLS • Removed row for VCMPOh and VCMPOl • In section: Clocks and PLL interfaces modules • Revised table: Main oscillator electrical characteristics • In table: 16 MHz RC Oscillator electrical specifications • Updated 'Max' of Tstartup • In table: 128 KHz Internal RC oscillator electrical specifications • Removed Uncaliberated 'Condition' for Fosc • Updated 'Min' and 'Max' of Caliberated Fosc • Updated 'Temperature dependence' and 'Supply dependence' • In table: PLL electrical specifications • Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption • Removed 'Typ' value of Duty Cycle at pllclkout • Removed 'Min' from calibration mode of Lock Time • In table: Jitter calculation • Added 1 Sigma Random Jitter value for Long term jitter
		• In section Flash read wait state and address pipeline control settings • Revised table: Flash Read Wait State and Address Pipeline Control • Removed section: On-chip peripherals • Added section: 'Reset sequence'
Rev4	Feb 10 2017	• Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics • Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics • Updated SIUL2_MSCRn[SRC 1:0]=11@25pF max value; SIUL2_MSCRn[SRC 1:0]=11@50pF min value; SIUL2_MSCRn[SRC 1:0]=10@25pF min and max values in AC specifications @ 3.3 V Range

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