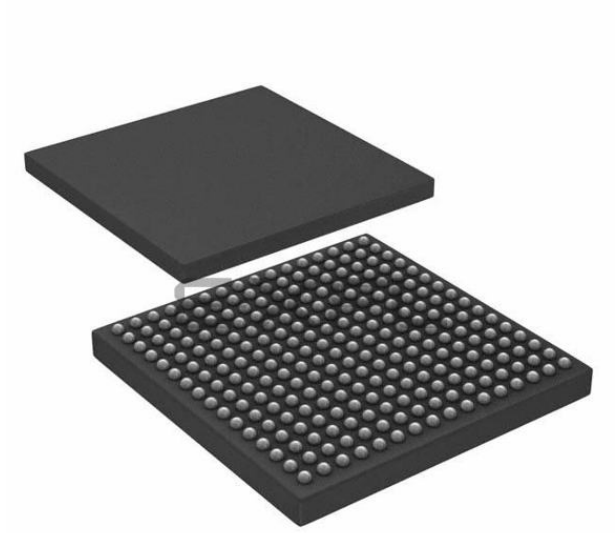

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5748ggk1mmj6

Table 1. MPC5748G Family Comparison[1] (continued)

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
I^2C	4				
SAI/I^2S	3				
FXOSC	8 - 40 MHz				
SXOSC	32 KHz				
FIRC	16 MHz				
SIRC	128 KHz				
FMPLL	Yes				
LPU	Yes				
FlexRay 2.1 (dual channel)	Yes, 128 MB				
MLB150	0		1		
USB 2.0 SPH	0		1		
USB 2.0 OTG	0		1		
SDHC	1				
Ethernet (RMII, MII + 1588, Muti queue AVB support)	Up to 2				
3 Port L2 Ethernet Switch	Optional				
CRC	1				
MEMU	2				
STCU	1				
HSM-v2 (security)	Optional				
Censorship	Yes				
FCCU	1				
Safety level	Specific functions ASIL-B certifiable				
User MBIST	Yes				
User LBIST	Yes				
I/O Retention in Standby	Yes				
GPIO[5]	Up to 264 GPI and up to 246 GPIO				
Debug	JTAGC, cJTAG				
Nexus	Z4 N3+ Z2 N3+				
Packages	176 LQFP-EP 256 BGA, 324 BGA				

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterisation.
3. Additional SWT included when HSM option selected
4. Refer device datasheet and reference manual for information on to timer channel configuration and functions.

5. Estimated I/O count for largest proposed packages based on multiplexing with peripherals.

Table 2. MPC5748G Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW	MPC5746	MPC5747	MPC5748
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	6	available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	6	available	available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	6	available	available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	available	available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	available	available	available
0x01280000	0x012BFFFF	256 KB code Flash block 10	7	not available	available	available
0x012C0000	0x012FFFFF	256 KB code flash block 11	7	not available	available	available
0x01300000	0x0133FFFF	256 KB code flash block 12	7	not available	available	available
0x01340000	0x0137FFFF	256 KB code flash block 13	7	not available	available	available
0x01380000	0x013BFFFF	256 KB code flash block 14	7	not available	not available	available
0x013C0000	0x013FFFFF	256 KB code flash block 15	7	not available	not available	available
0x01400000	0x0143FFFF	256 KB code flash block 16	8	not available	not available	available
0x01440000	0x0147FFFF	256 KB code flash block 17	8	not available	not available	available
0x01480000	0x014BFFFF	256 KB code flash block 18	8	not available	not available	available
0x14C0000	0x014FFFFF	256 KB code flash block 19	9	not available	not available	available
0x01500000	0x0153FFFF	256 KB code flash block 20	9	not available	not available	available
0x01540000	0x0157FFFF	256 KB code flash block 21	9	not available	not available	available

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[3, 4]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[5]	Decoupling pin for low power regulators[6]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[7]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 µF capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA. SeeThermal attributes

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{DD_FULL} 2, 3	RUN Full Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	219	292	mA
		T_a = 105°C	—	230	328	mA
		T_a = 125 °C	—	249	400	mA
I_{DD_GWY} 5, 6	RUN Gateway Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	183	260	mA
		T_a = 105°C	—	196	294	mA
		T_a = 125°C[4]	—	215	348	mA
$I_{DD\_BODY\_1}$ 7, 8	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	149	223	mA
		T_a = 105 °C	—	158	270	mA
		T_a = 125°C [4]	—	175	310	mA
IDD_BODY_2[9, 10]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	105	174	mA

Table continues on the next page...

x FlexCAN state machines clocked(other FLEXCAN clock gated), 4 x LINFlexD transmitting (Other clock gated), 1x eMIOS clocked(used OPWFMB mode) (Others clock gated), FIRC, SIRC, FXOSC, SXOSC, PLL running, BCTU, DMAMUX, ACMP clock gated. All others modules clock gated if not specifically mentioned. I/O supply current excluded

6. Recommended Transistors:MJD31@85°C, 105°C and 125°C.
7. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @120Mhz(Instruction and Data cache enabled),Platform@120MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFlexD transmitting (others clocked), 1xeMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
8. Recommended Transistors:BCP56, BCP68 or MJD31@85°C, BCP56, BCP68 or MJD31@105°C and MJD31@125°C.
9. Enabled Modules in Body mode enabled at maximum frequency:2 x e200Z4 @80Mhz(Instruction and Data cache enabled),Platform@80MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFlexD transmitting (others clocked), 1xeMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
10. Recommended Transistors:BCP56, BCP68 or MJD31@85°C, 105°C and 125°C
11. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
12. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.

Table 11. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM, but only one RAM being accessed	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	8.9		mA
		T_a = 25 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON		10.2		
		T_a = 85 °C	—	12.5	22	
		T_a = 105 °C	—	14.5	24	
		T_a = 125 °C [2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	16	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.535		mA
		T_a = 85 °C	—	0.72	6	
		T_a = 105 °C	—	1	8	
		T_a = 125 °C [2]	—	1.6	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11)	38	132	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11)	48	220	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10)	19	66	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

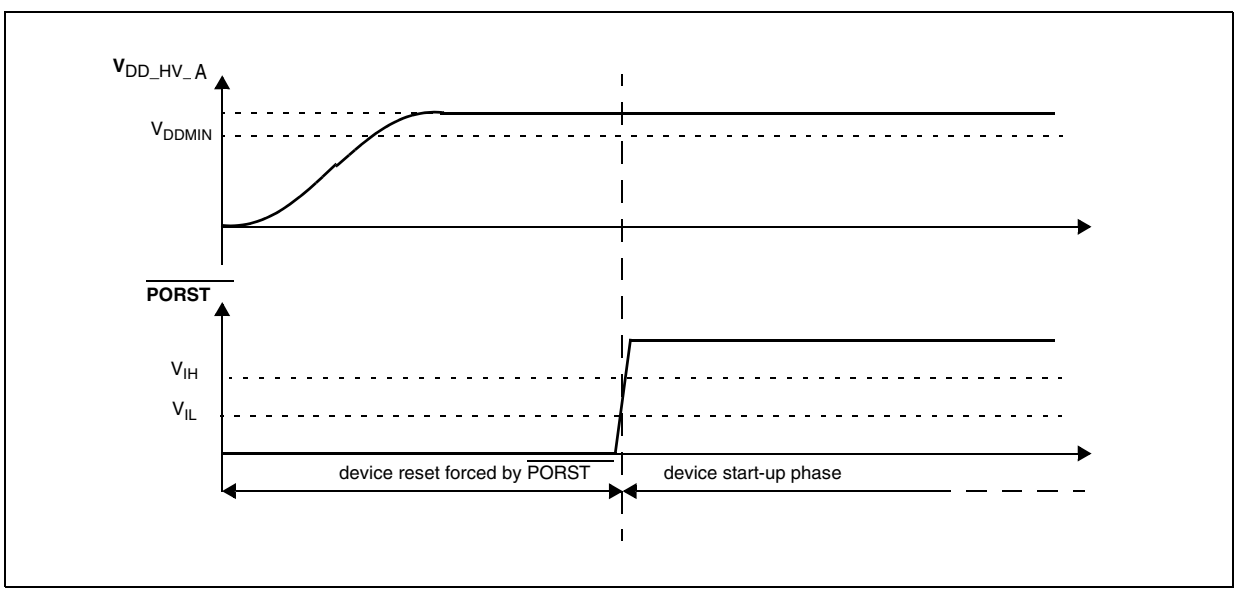


Figure 3. Start-up reset requirements

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{PORST}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{PORST}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD\_HV\_A}$	—	V
V_{IL}	Input low level	—	0.35 x $V_{DD\_HV\_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

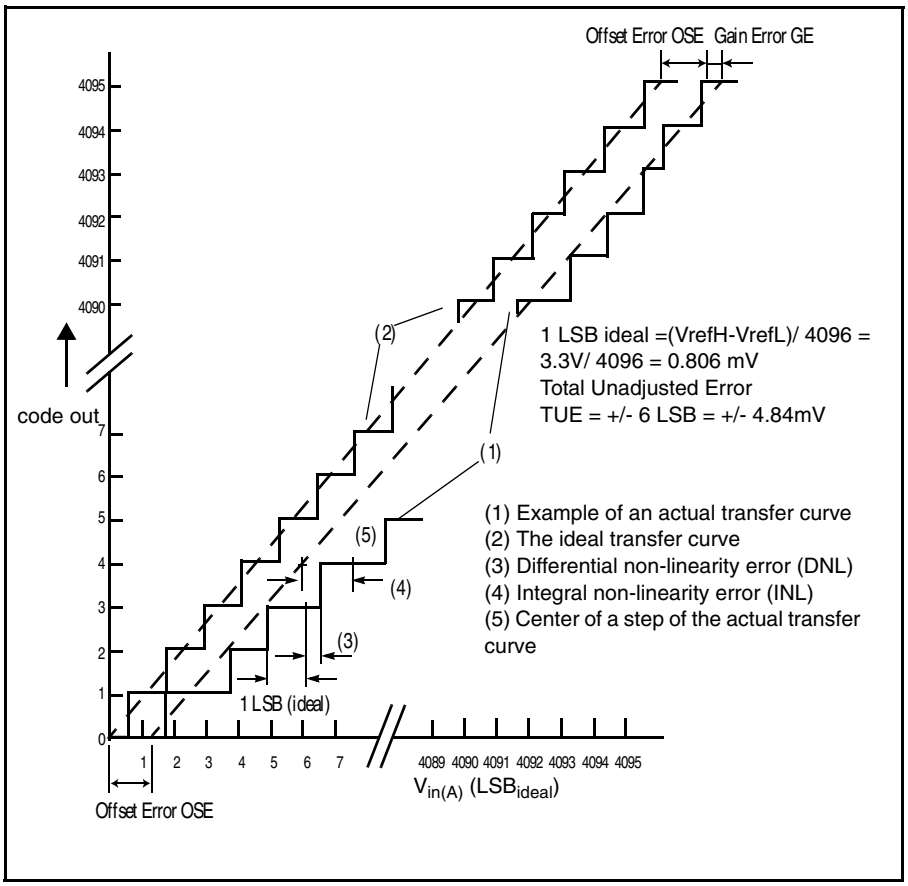


Figure 5. ADC characteristics and error definitions

6.1.2 Analog Comparator (CMP) electrical specifications

Table 22. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1\_CMP\_REF}$	V
V_{AIO}	Analog input offset voltage [1]	-42	—	42	mV
V_H	Analog comparator hysteresis [2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV
	• CR0[HYSTCTR] = 10	—	60	105	mV
	• CR0[HYSTCTR] = 11				
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	21	µs
	Analog comparator initialization delay, High speed mode[4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

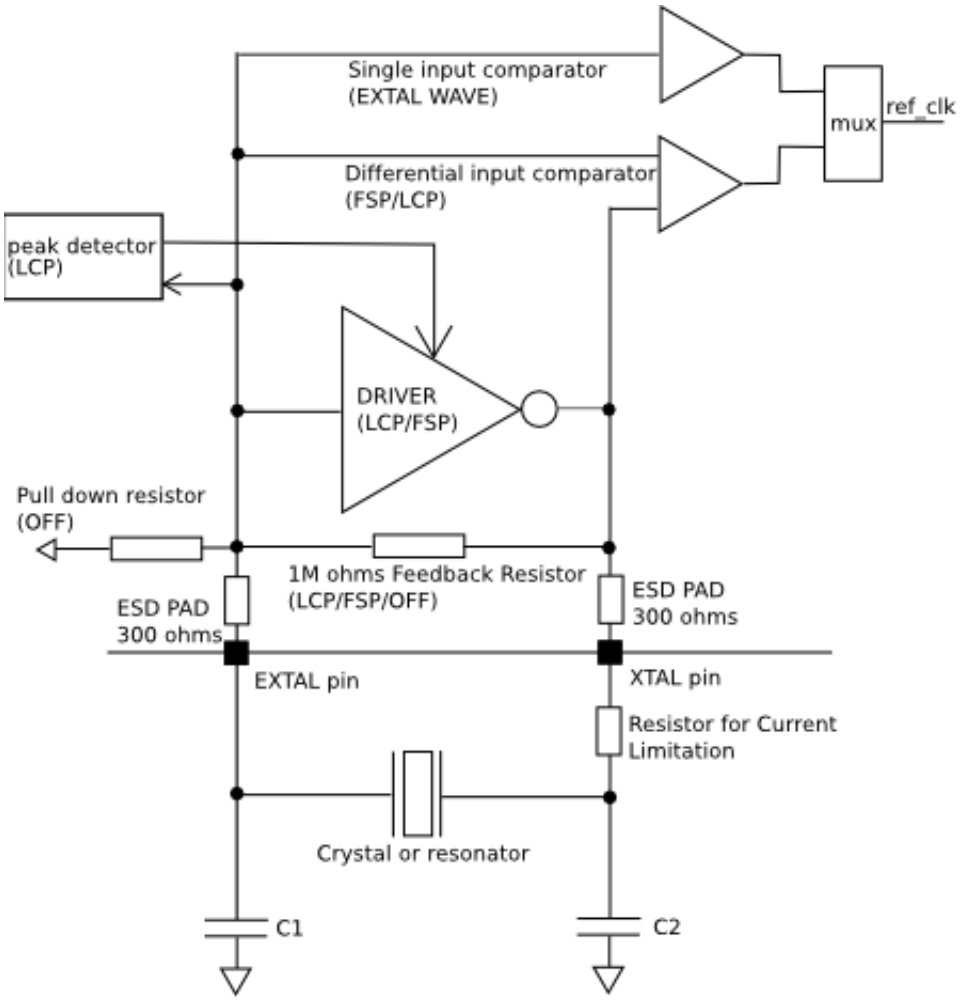


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		

Table continues on the next page...

Table 30. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 31. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max	Units
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

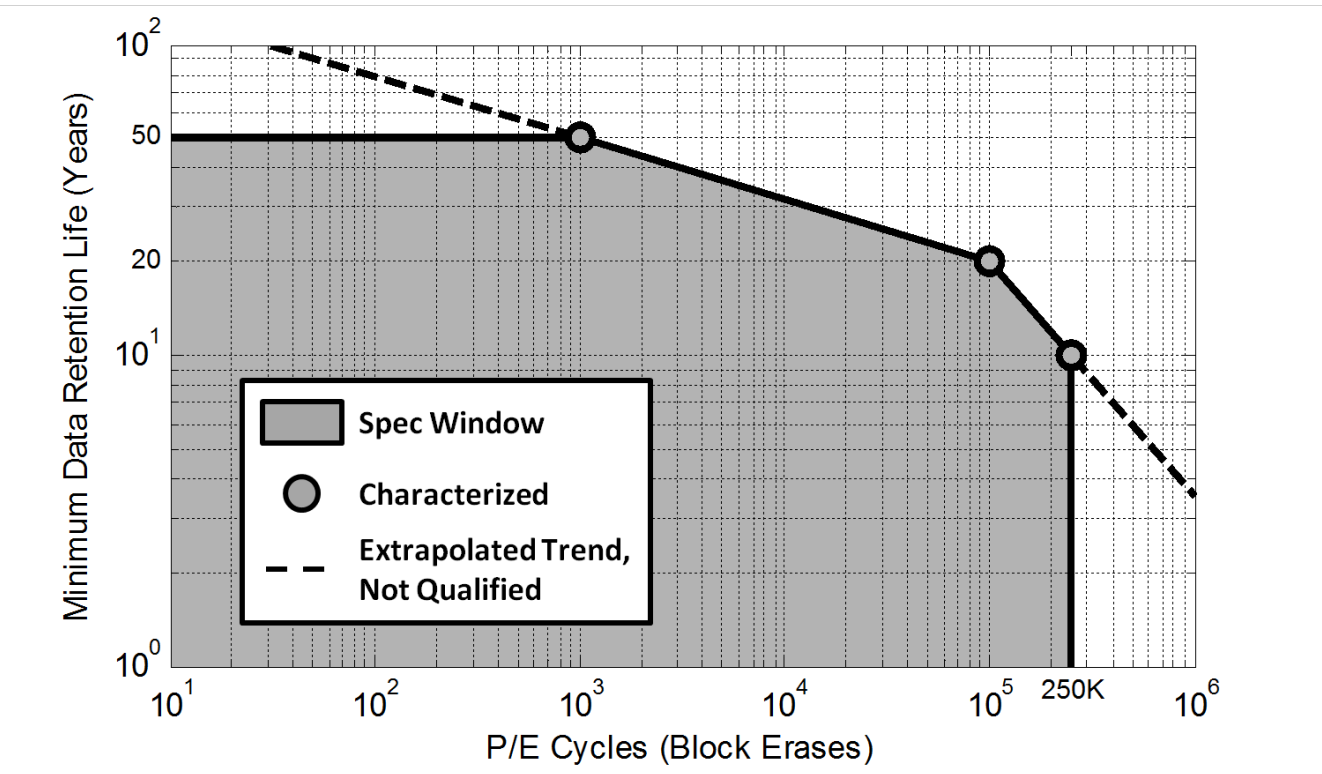
6.3.3 Flash memory module life specifications

Table 32. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.4.2.2 TxEN

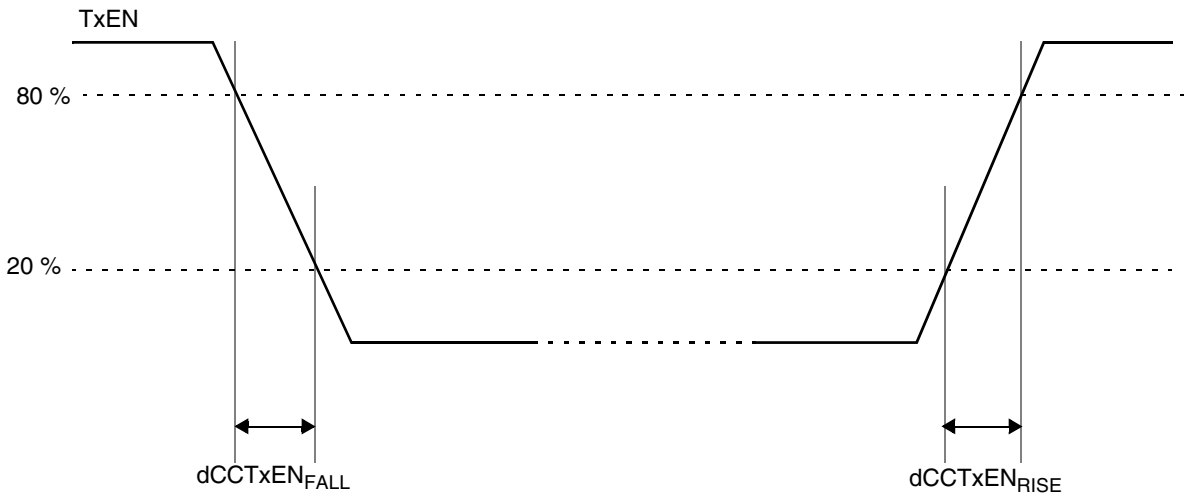


Figure 17. TxEN signal

Table 38. TxEN output characteristics[1]

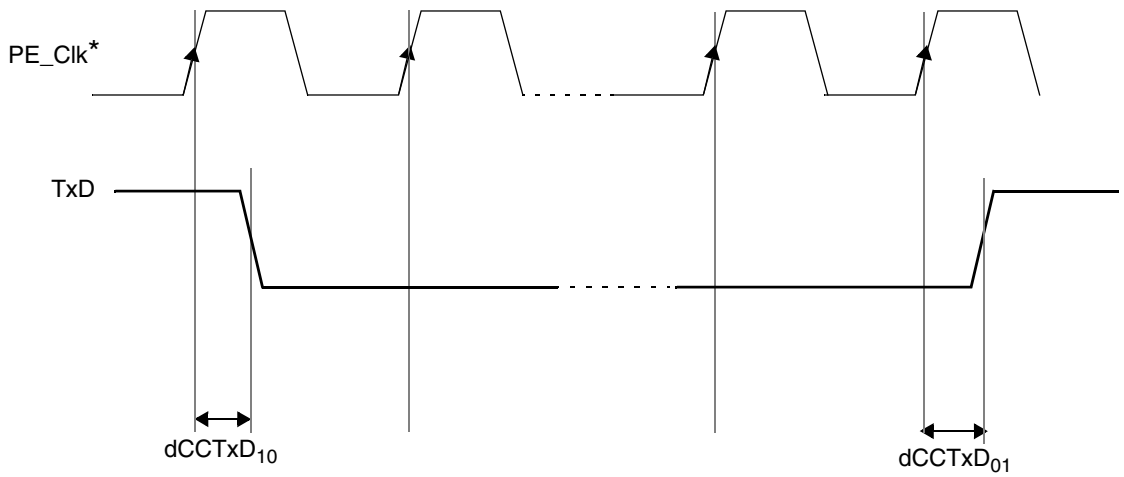
Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

Table 39. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.
2. MLBCLK low/high time includes the pluse width variation.
3. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

6.4.6 USB electrical specifications

6.4.6.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

6.4.6.2 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 47. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

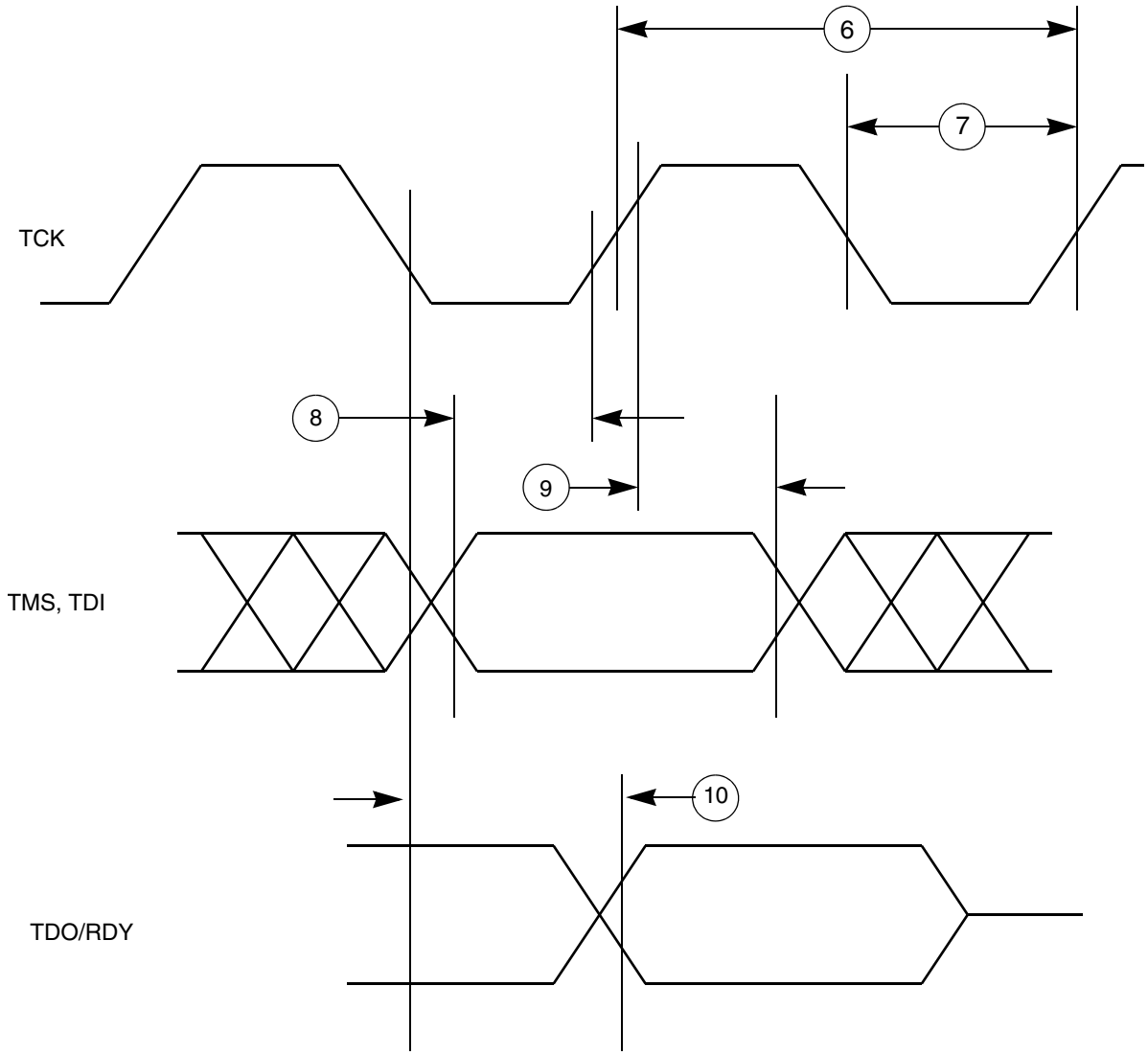


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	18.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

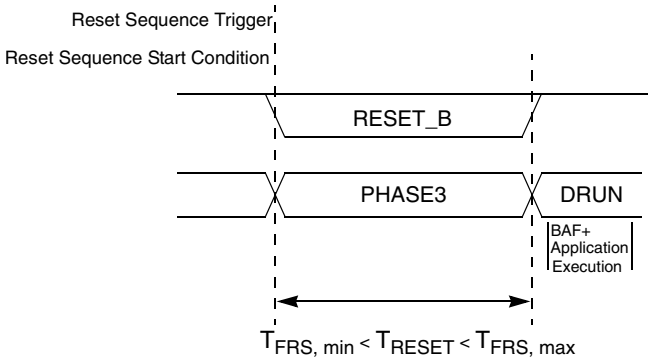


Figure 39. Functional reset sequence short

The reset sequences shown in Figure 38 and Figure 39 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 56. Revision History

Rev. No.	Date	Substantial Changes
1	14 March 2013	Initial Release
1.1	16 May 2013	Updated Pinouts section

2	22 May 2014	• Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet
		• Revised the feature list.
		• Revised Introduction section to remove classification information.
		• Updated optional information in the ordering information figure.
		• Revised Absolute maximum rating section:
		  • Removed category column from table
		  • Added footnote at Ta
		• Revised Recommended operating conditions section
		  • Added notes
		  • Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V)
		  • Updated table: Recommended operating conditions (VDD_HV_x = 5 V)
		• Revised Voltage regulator electrical characteristics
		  • Updated text describing bipolar transistors
		  • Updated figure: Voltage regulator capacitance connection
		  • Updated table: Voltage regulator electrical specifications
		  • Removed Brownout information
		• Revised Voltage monitor electrical characteristics table

		• Revised Supply current characteristics section
		  • Updated table: Current consumption characteristics
		  • Updated table: Low Power Unit (LPU) Current consumption characteristics
		  • STANDBY Current consumption characteristics

Table continues on the next page...

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In table: Functional Pad AC Specifications @ 3.3 V Range
		  • Updated values for symbol 'pad_sr_hv (output)'
		• In table: DC electrical specifications @ 3.3V Range
		  • Updtaed values for VDD_HV_x, Vih, Vhys
		  • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys
		• In table: Functional Pad AC Specifications @ 5 V Range
		  • Updated values for symbol 'pad_sr_hv (output)'
		• In table DC electrical specifications @ 5 V Range
		  • Added Vih (pad_i_hv), Vil (pad_i_hv), Vhys (pad_i_hv), Vih_hys, Vil_hys

		• In section: PORST electrical specifications
		  • In table: PORST electrical specifications
		  • Updated 'Min' value for $W_{NFPORST}$
		  • Corrected 'Unit' for V_{IH} and V_{IL}
		
		• In section: Peripheral operating requirements and behaviours
		  • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit)
		
		• In section: Analogue Comparator (CMP) electrical specifications
		  • In table: Comparator and 6-bit DAC electrical specifications
		  • Updated 'Max' value of I_{DDLS}
		  • Updated 'Min' and 'Max' for V_{AIO} and DNL
		  • Updated 'Descripton' 'Min' 'Max' od V_H
		  • Updated row for tDHS
		  • Added row for tDLS
		  • Removed row for VCMPOh and VCMPOl
		
		• In section: Clocks and PLL interfaces modules
		  • Revised table: Main oscillator electrical characteristics
		  • In table: 16 MHz RC Oscillator electrical specifications
		  • Updated 'Max' of Tstartup
		  • In table: 128 KHz Internal RC oscillator electrical specifications
		  • Removed Uncaliberated 'Condition' for Fosc
		  • Updated 'Min' and 'Max' of Caliberated Fosc
		  • Updated 'Temperature dependence' and 'Supply dependence'
		  • In table: PLL electrical specifications
		  • Removed Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (VDD_LV), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption
		  • Removed 'Typ' value of Duty Cycle at pllclkout
		  • Removed 'Min' from calibration mode of Lock Time
		  • In table: Jitter calculation
		  • Added 1 Sigma Random Jitter value for Long term jitter

		• In section Flash read wait state and address pipeline control settings • Revised table: Flash Read Wait State and Address Pipeline Control • Removed section: On-chip peripherals • Added section: 'Reset sequence'
Rev4	Feb 10 2017	• Added VDD_HV_BALLAST footnote in Voltage regulator electrical characteristics • Added Note to clarify In-Rush current and pin capacitance in Voltage regulator electrical characteristics • Updated SIUL2_MSCRn[SRC 1:0]=11@25pF max value; SIUL2_MSCRn[SRC 1:0]=11@50pF min value; SIUL2_MSCRn[SRC 1:0]=10@25pF min and max values in AC specifications @ 3.3 V Range

Table continues on the next page...