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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I ² C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	129
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5748gsk1mku6r

1 Block diagram

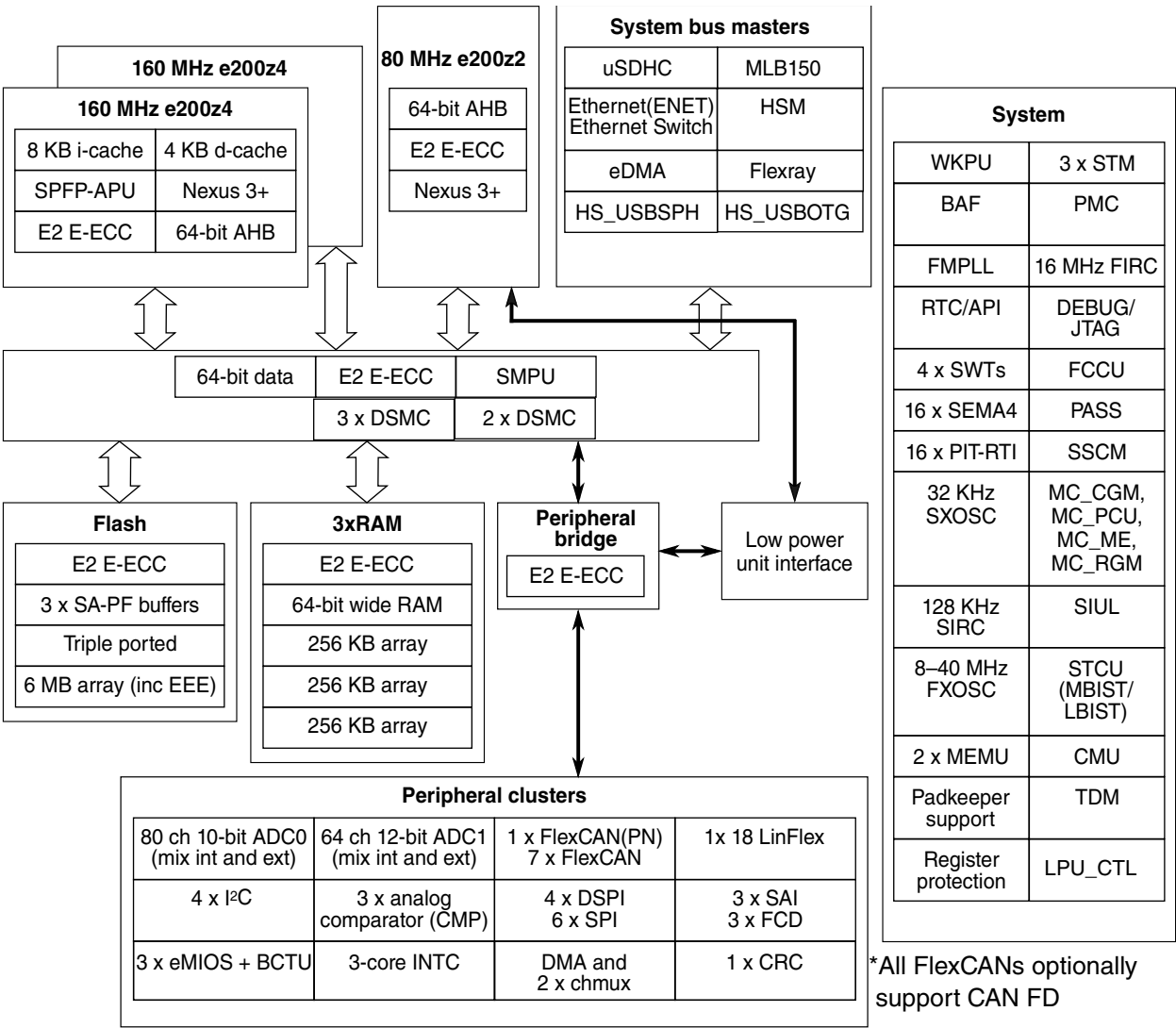


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison¹

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
CPUs	e200z4	e200z4	e200z4	e200z4	e200z4
	e200z2	e200z2	e200z4	e200z4	e200z4
			e200z2	e200z2	e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4
			e200z4	e200z4	e200z4
Maximum Operating Frequency ²	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)	160MHz (z4)
	80MHz (z2)	80MHz (z2)	160MHz (z4)	160MHz (z4)	160MHz (z4)
			80MHz (z2)	80MHz (z2)	80MHz (z2)
Flash memory	4 MB	6 MB	3 MB	4 MB	6 MB
EEPROM support	32 KB to 128 KB emulated		32 KB to 192 KB emulated		
RAM	512 KB	768 KB			
ECC	End to End				
SMPU	24 entry		32 entry		
DMA	32 channels				
10-bit ADC	48 Standard channels 32 External channels				
12-bit ADC	16 Precision channels 16 Standard channels 32 External channels				
AnalogComparator	3				
BCTU	1				
SWT	2		4 ³		
STM	2		3		
PIT-RTI	16 channels PIT 1 channels RTI				
RTC/API	Yes				
Total Timer I/O ⁴	96 channels 16-bits				
LINFlexD	1 M/S, 15 M		1 M/S, 17 M		
FlexCAN	8 with optional CAN FD support				
DSPI/SPI	4 x DSPI				
	6 x SPI				

Table continues on the next page...

Table 3. MPC5748G Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW	MPC5747C MPC5748C	MPC5746G MPC5747G MPC5748G
0x00F90000	0x00F93FFF	16 KB data Flash	2	available	available
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	available	available
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	available	available
0x00FA8000	0x00FABFFF	16 KB data Flash	3	available	available
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	available	available
0x00FB0000	0x00FB7FFF	32 KB data Flash	2	not available	available
0x00FB8000	0x00FBFFFF	32 KB data flash	3	not available	available

Table 4. MPC5748G Family Comparison - RAM Memory Map

Start Address	End Address	Allocated size [KB]	MPC5747C	MPC5748C MPC5746G MPC5747G MPC5748G
0x40000000	0x40001FFF	8	available	available
0x40002000	0x4000FFFF	56	available	available
0x40010000	0x4001FFFF	64	available	available
0x40020000	0x4003FFFF	128	available	available
0x40040000	0x4007FFFF	256	available	available
0x40080000	0x400BFFFF	256	not available	available

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5748G .

3.2 Ordering Information

Example Code	P	PC	57	4	8	G	S	K0	M	MJ	6	R
Qualification Status	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Power Architecture	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Automotive Platform	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Core Version	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Flash Size (core dependent)	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Product	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Optional fields	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Fab and mask indicator	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Temperature spec.	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
Package Code	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
CPU Frequency	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____	_____
R = Tape & Reel (blank if Tray)												

Qualification Status P = Engineering samples S = Automotive qualified	Product Version C = Body Control Feature Set G = Gateway Feature Set	Package Code KU = 176 LQFP EP MJ = 256 MAPBGA MN = 324 MAPBGA
PC = Power Architecture Automotive Platform 57 = Power Architecture in 55nm	Optional fields Blank = Feature not available S = HSM (Security Module) F = CAN FD B = Both HSM and CAN FD T = HSM and 2nd Ethernet G = CAN FD and 2nd Ethernet H = HSM, CAN FD, and 2nd Ethernet	CPU Frequency 2 = Each z4 operates up to 120 MHz 6 = Each z4 operates up to 160 MHz
Core Version 4 = e200z4 Core Version (highest core version in the case of multiple cores)	Fab and mask version indicator K=TSMC Fab #=Version of maskset 0=0N65H 1=1N81M 0A=0N78S	Shipping Method R = Tape and reel Blank = Tray
Flash Memory Size 6 = 3 MB 7 = 4 MB 8 = 6 MB		Temperature spec. C = -40.C to +85.C Ta V = -40.C to +105.C Ta M = -40.C to +125.C Ta

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in [Table 5](#) for specific conditions

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FL A should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions (V_{DD_HV_x} = 3.3 V)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
V _{DD_HV_A} V _{DD_HV_B} V _{DD_HV_C}	HV IO supply voltage	—	3.15	3.6	V
V _{DD_HV_FL A} ³	HV flash supply voltage	—	3.15	3.6	V
V _{DD_HV_ADC1_REF}	HV ADC1 high reference voltage	—	3.0	5.5	V
V _{DD_HV_ADC0} V _{DD_HV_ADC1}	HV ADC supply voltage	—	max(V _{DD_HV_A} , V _{DD_HV_B} , V _{DD_HV_C}) - 0.05	3.6	V
V _{SS_HV_ADC0} V _{SS_HV_ADC1}	HV ADC supply ground	—	-0.1	0.1	V
V _{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
V _{IN1_CMP_REF} ^{5, 6}	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I _{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

Table 6. Recommended operating conditions ($V_{DD_HV_x} = 3.3\text{ V}$) (continued)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. $V_{DD_HV_FLA}$ must be connected to $V_{DD_HV_A}$ when $V_{DD_HV_A} = 3.3\text{ V}$
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
5. $V_{IN1_CMP_REF} \leq V_{DD_HV_A}$
6. This supply is shorted $V_{DD_HV_A}$ on lower packages.

NOTE

If $V_{DD_HV_A}$ is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. $V_{DD_HV_FLA}$ should not be supplied externally and should only have decoupling capacitor.

Table 7. Recommended operating conditions ($V_{DD_HV_x} = 5\text{ V}$)

Symbol	Parameter	Conditions ¹	Min ²	Max	Unit
$V_{DD_HV_A}$ $V_{DD_HV_B}$ $V_{DD_HV_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD_HV_FLA}$ ³	HV flash supply voltage	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	HV ADC supply voltage	—	$\max(V_{DD_H_V_A}, V_{DD_H_V_B}, V_{DD_H_V_C}) - 0.05$	5.5	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV} ⁴	Core supply voltage	—	1.2	1.32	V
$V_{IN1_CMP_REF}$ ⁵	Analog Comparator DAC reference voltage	—	3.15	5.5	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A	Ambient temperature under bias	$f_{CPU} \leq 160\text{ MHz}$	-40	125	°C
T_J	Junction temperature under bias	—	-40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When V_{DD_HV} is in 5 V range, $V_{DD_HV_FLA}$ cannot be supplied externally. This pin is decoupled with C_{flash_reg} .
4. V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. This supply is shorted $V_{DD_HV_A}$ on lower packages.

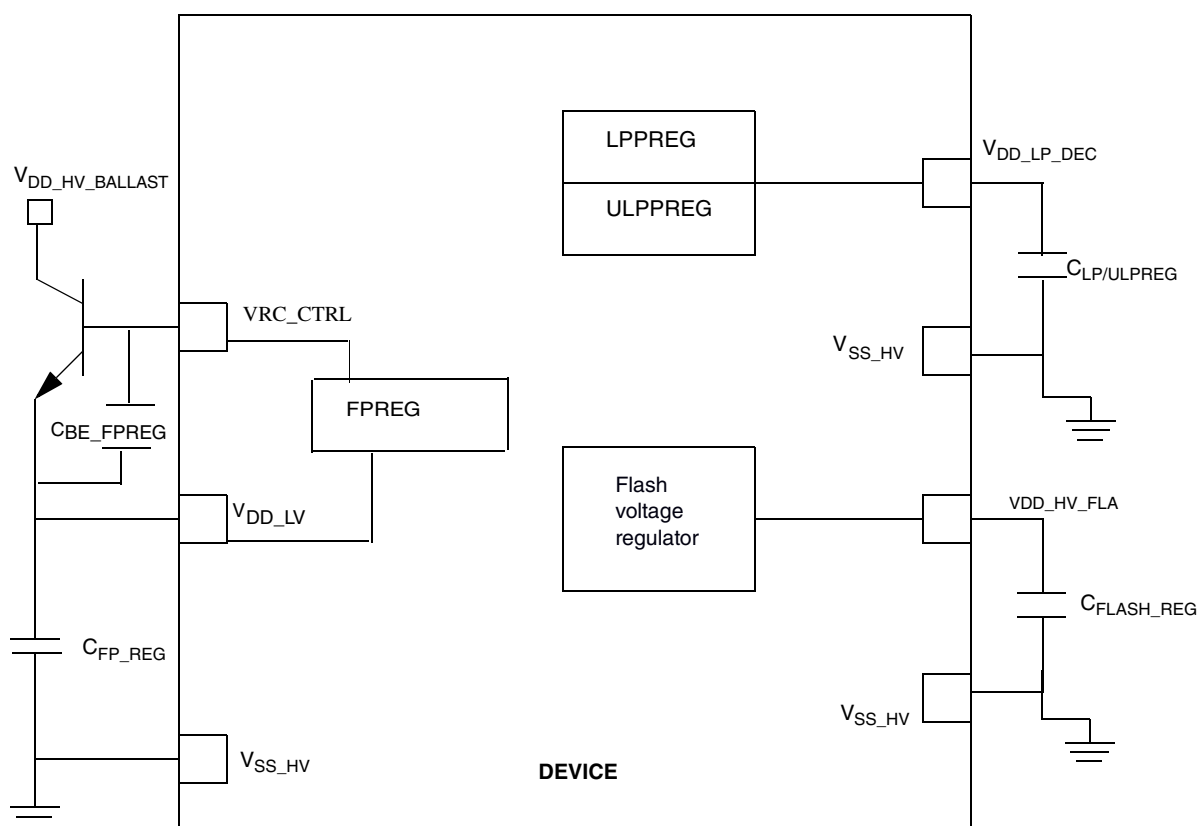


Figure 2. Voltage regulator capacitance connection

Table 8. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{fp_reg}^1$	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2 ²	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	μF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
$C_{be_fpreg}^3$	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		
$C_{flash_reg}^4$	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	μF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm

Table continues on the next page...

Table 20. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
R_{AD}^6	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{\text{precision channels}}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection		+/-5		LSB
$TUE_{\text{standard/extended channels}}$	Total unadjusted error for standard/extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection ⁷		+/-8		LSB
t_{recovery}	STOP mode to Run mode recovery time				< 1	μs

- Active ADC input, $V_{inA} < [\min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]$. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions ($VDD_HV_x = 3.3\text{ V}$)' for required relation between IO_supply_A,B,C and ADC_Supply .
- The internally generated clock (known as AD_clk or $ADCK$) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
- During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample} . After the end of the sample time t_{sample} , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
- This parameter does not include the sample time t_{sample} , but only the time for determining the digital result and the time to load the result register with the conversion result.
- Apart from t_{sample} and t_{conv} , few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
- See Figure 2.
- Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (V_{INA} , see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 21. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ ¹	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK^2 frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time ³	80 MHz @ 100 ohm source impedance	275	—	—	ns

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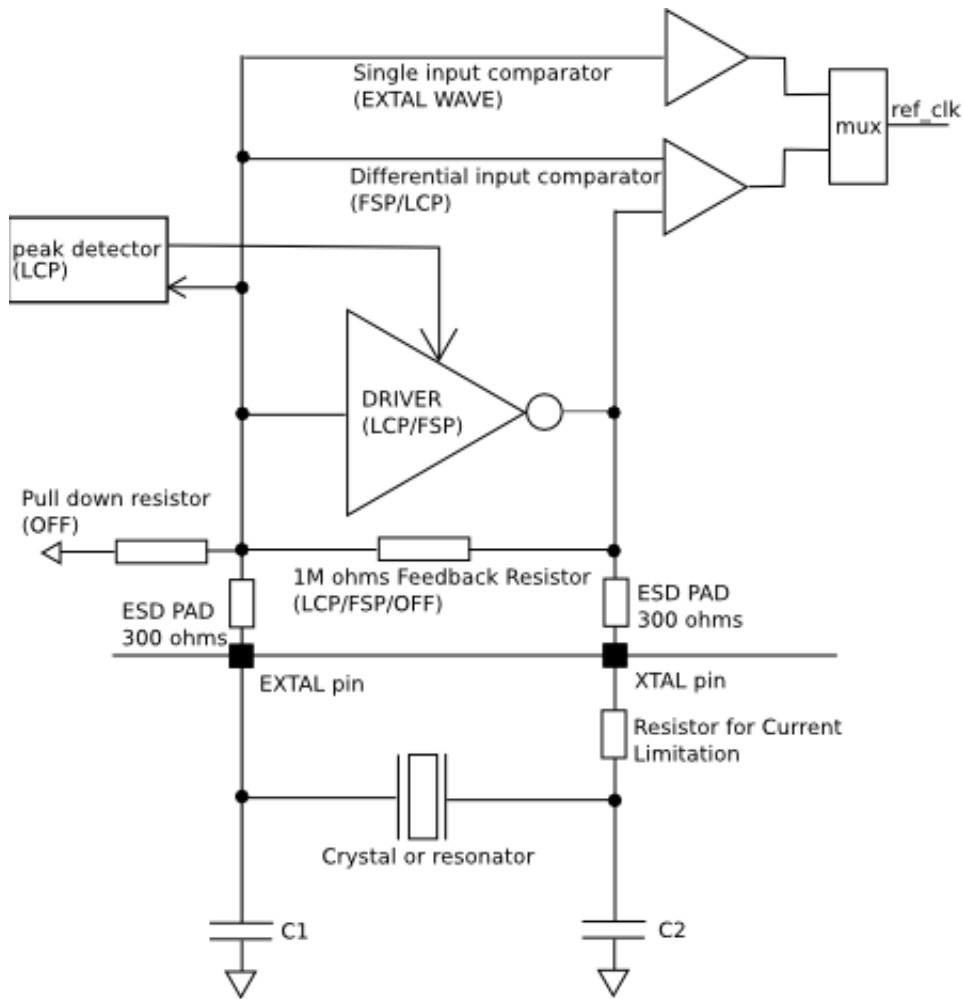


Figure 7. Oscillator connections scheme

Table 23. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		

Table continues on the next page...

Table 23. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V _{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V _{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

6.2.2 32 kHz Oscillator electrical specifications

Table 24. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t _{cst}	Crystal Start-up Time ^{1, 2}				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 25. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F _{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
T _{startup}	Startup time	—		—	1.5	us
T _{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T _{LTJIT}	Long term jitter		—	—	0.2	%

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

Memory interfaces

2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See [Percentage of sample exceeding specified value of jitter table](#)

Table 29. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30×10^{-3}
5	5.63×10^{-5}
6	2.00×10^{-7}
7	2.82×10^{-10}

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

[Table 30](#) shows the estimated Program/Erase times.

Table 30. Flash memory program and erase specifications

Symbol	Characteristic ¹	Typ ²	Factory Programming ^{3, 4}		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life ⁵	Lifetime Max ⁶		
			20°C ≤T _A ≤30°C	-40°C ≤T _J ≤150°C	-40°C ≤T _J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t _{dwp_{pgm}}	Doubleword (64 bits) program time	43	100	150	55	500		μs
t _{pp_{pgm}}	Page (256 bits) program time	73	200	300	108	500		μs
t _{qpp_{pgm}}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		μs
t _{16k_{ers}}	16 KB Block erase time	168	290	320	250	1,000		ms
t _{16k_{pgm}}	16 KB Block program time	34	45	50	40	1,000		ms

Table continues on the next page...

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 34. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

6.4 Communication interfaces

6.4.1 DSPI timing

Table 35. DSPI electrical specifications

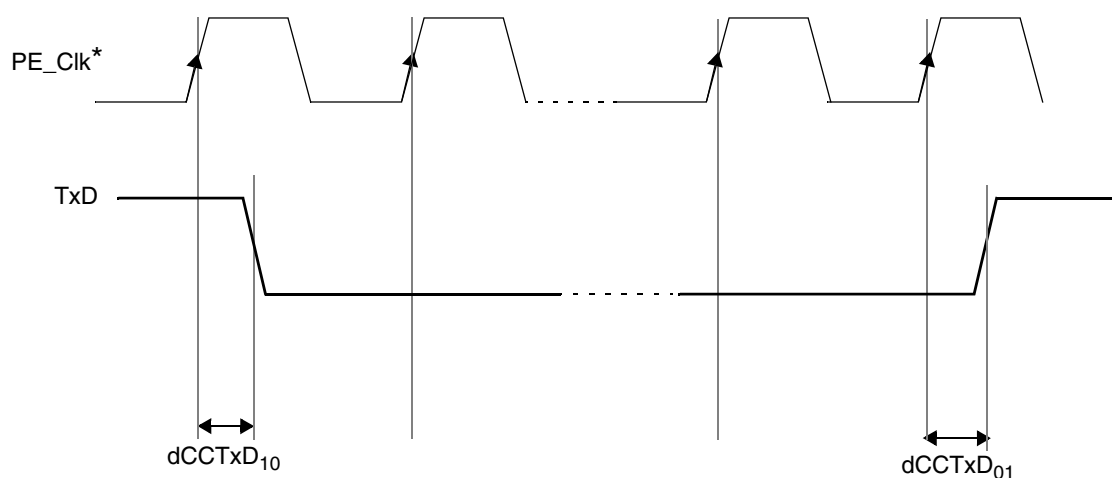
No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2 - 10$	$t_{SCK}/2 + 10$	—	—	ns
5	t_A	Slave access time	\overline{SS} active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	\overline{SS} inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to PCSS time	—	13	—	—	—	ns
8	t_{PASC}	PCSS to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8 ¹	—	

Table continues on the next page...

Table 39. TxD output characteristics (continued)

Name	Description ¹	Min	Max	Unit
dCCTxD ₀₁	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
dCCTxD ₁₀	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx} = 3.3\text{ V} \pm 5\%, \pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$, TxD pin load maximum 25 pF.
2. For $3.3\text{ V} \pm 10\%$ operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40. RxD input characteristic

Name	Description ¹	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
dCCRxD ₀₁	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
dCCRxD ₁₀	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $VDD_HV_IOx = 3.3\text{ V} \pm 5\%$, $\pm 10\%$, $T_J = -40\text{ }^{\circ}\text{C} / 150\text{ }^{\circ}\text{C}$.

6.4.3 uSDHC specifications

Table 41. uSDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
Card input clock					
SD1	fpp	Clock frequency (Identification mode)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (SD\SDIO high speed)	0	40	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f _{OD}	Clock frequency (MMC full speed)	0	40	MHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	6.5	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

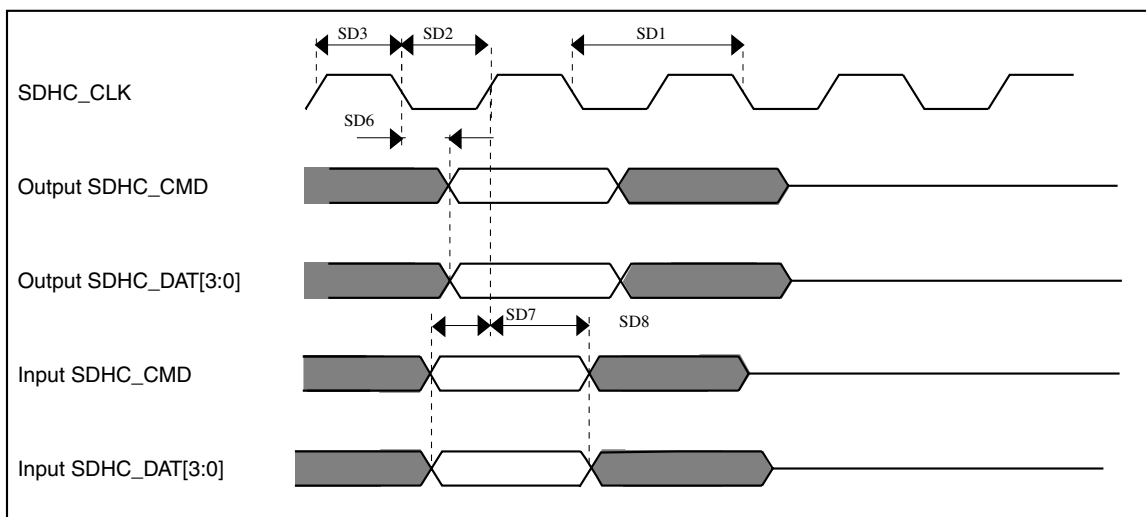


Figure 21. uSDHC timing

6.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

NOTE

ENET0 supports the following xMII interfaces: MII, MII_Lite and RMII. ENET1 supports the following xMII interfaces: MII_Lite.

NOTE

It is only possible to use ENET0 and ENET1 simultaneously when both are configured for MII_Lite.

NOTE

In certain pinout configurations ENET1 MII-Lite signals can be across multiple VDD_HV_A/B/C domains. If these configuration are used, VDD_HV IO domains need to be at the same voltage (for example: 3.3V)

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

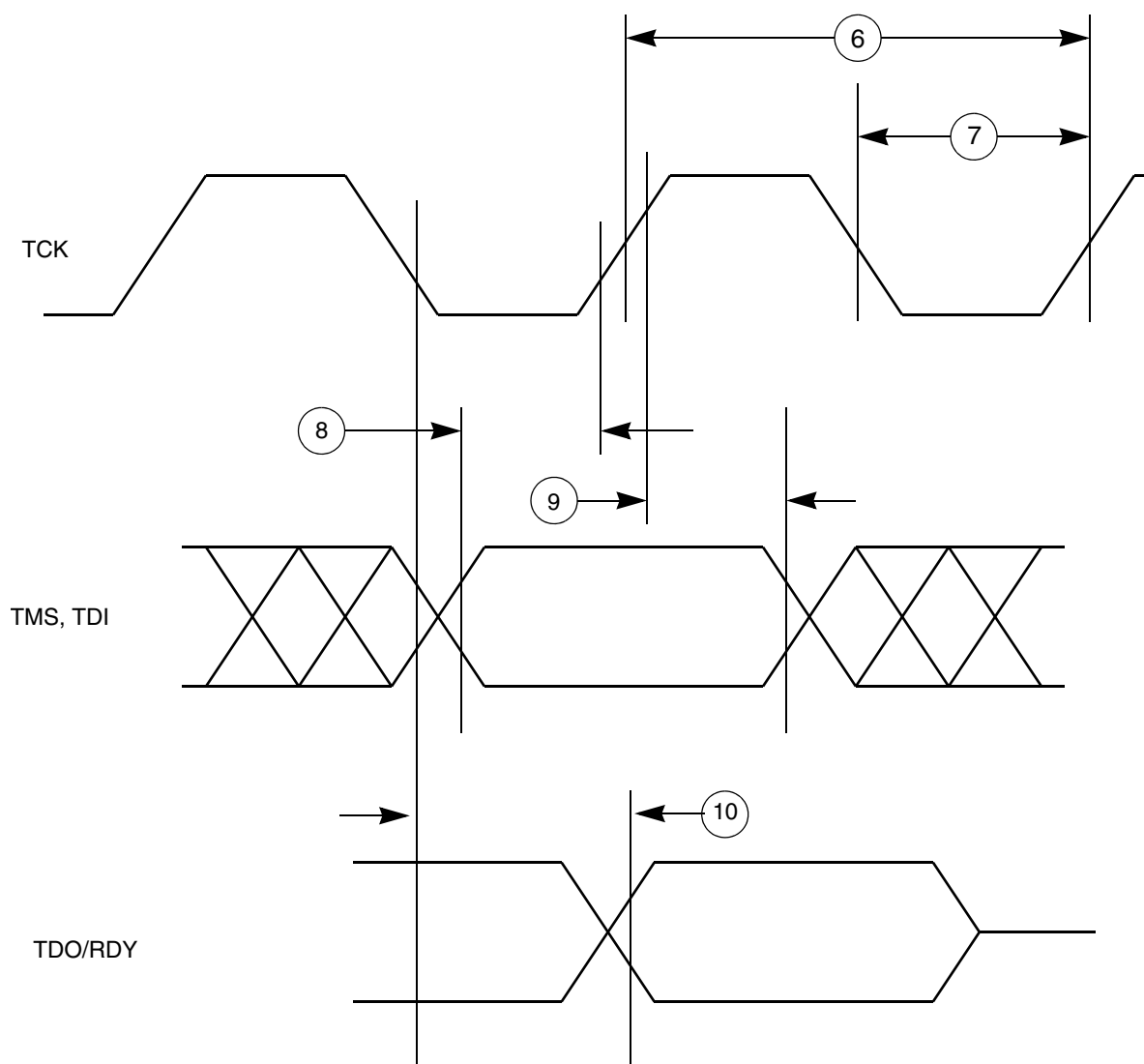


Figure 33. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 52. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI D}$	NMI pulse width that is passed	400	—	—	ns

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	0.2	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,23
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	18.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

[Table 54](#) specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in [Reset sequence description](#).

Table 54. RESET sequences

No.	Symbol	Parameter	T _{Reset}			Unit
			Min	Typ ¹	Max	
1	T _{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T _{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T _{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T _{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T _{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

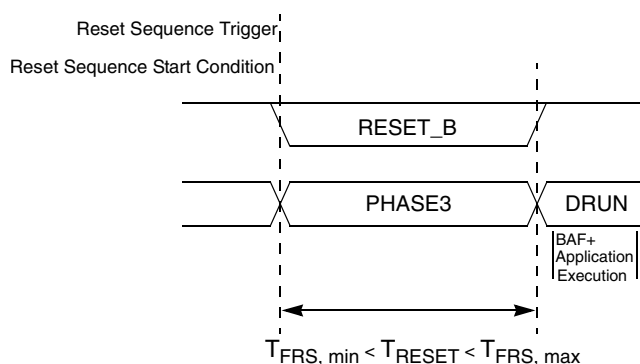


Figure 39. Functional reset sequence short

The reset sequences shown in [Figure 38](#) and [Figure 39](#) are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

The following table provides a revision history for this document.

Table 56. Revision History

Rev. No.	Date	Substantial Changes
1	14 March 2013	Initial Release
1.1	16 May 2013	Updated Pinouts section
2	22 May 2014	<ul style="list-style-type: none"> Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet Revised the feature list. Revised Introduction section to remove classification information. Updated optional information in the ordering information figure. Revised Absolute maximum rating section: <ul style="list-style-type: none"> Removed category column from table Added footnote at Ta Revised Recommended operating conditions section <ul style="list-style-type: none"> Added notes Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V) Updated table: Recommended operating conditions (VDD_HV_x = 5 V) Revised Voltage regulator electrical characteristics <ul style="list-style-type: none"> Updated text describing bipolar transistors Updated figure: Voltage regulator capacitance connection Updated table: Voltage regulator electrical specifications Removed Brownout information Revised Voltage monitor electrical characteristics table
		<ul style="list-style-type: none"> Revised Supply current characteristics section <ul style="list-style-type: none"> Updated table: Current consumption characteristics Updated table: Low Power Unit (LPU) Current consumption characteristics STANDBY Current consumption characteristics

Table continues on the next page...

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