Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z2, e200z4, e200z4
Core Size	32-Bit Tri-Core
Speed	80MHz/160MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SAI, SPI, USB, USB OTG
Peripherals	DMA, LVD, POR, WDT
Number of I/O	178
Program Memory Size	6MB (6M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 80x10b, 64x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LBGA
Supplier Device Package	256-MAPPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5748gtk1mmj6

1 Block diagram

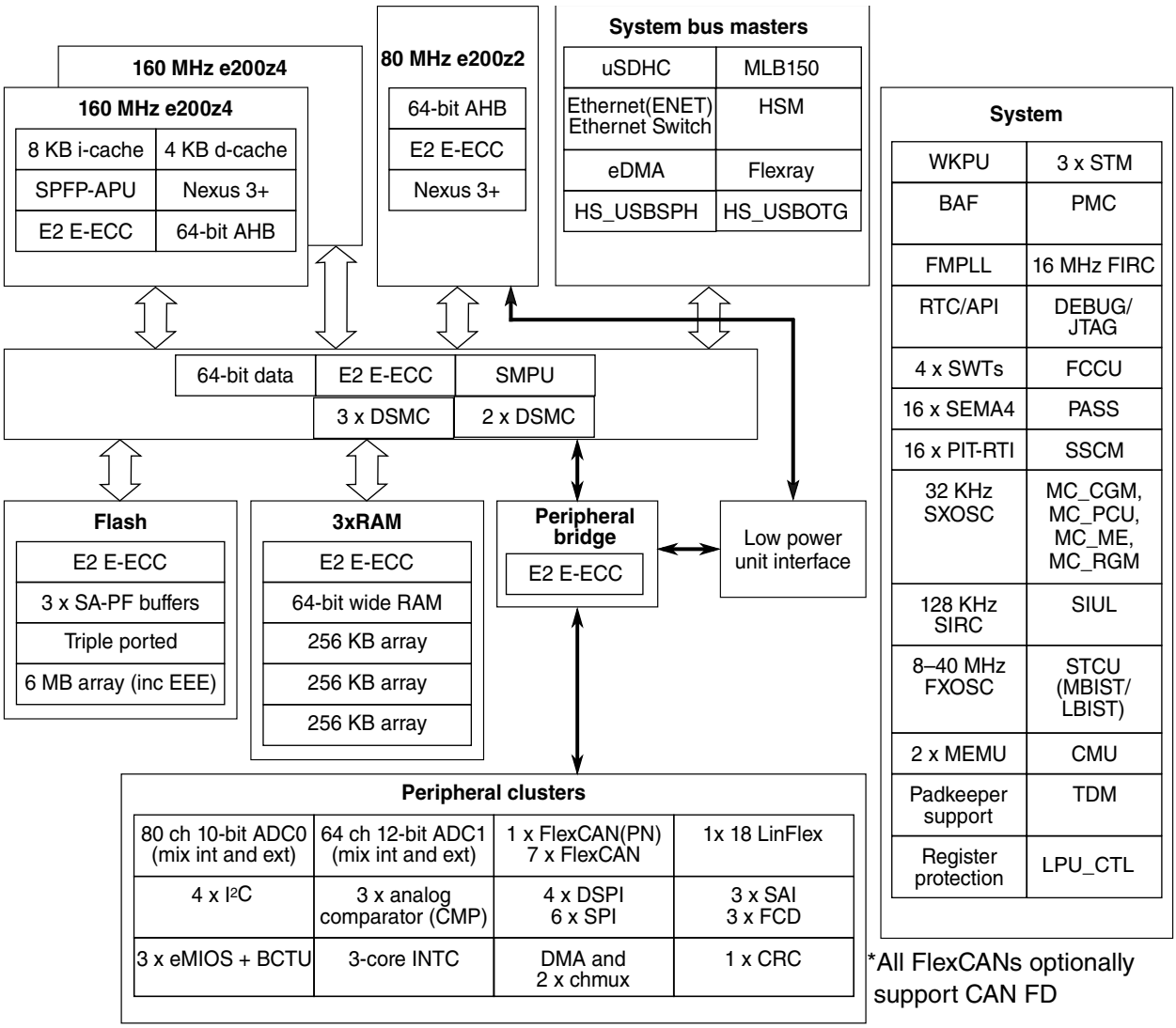


Figure 1. MPC5748G block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5748G family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

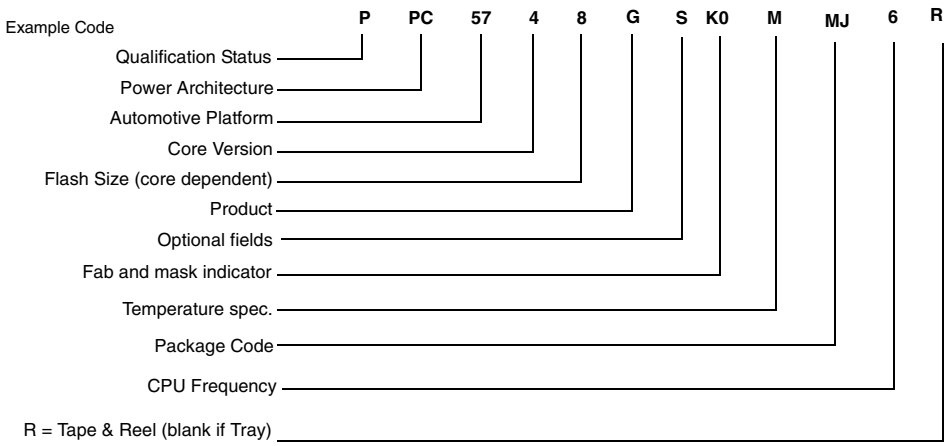
All optional features (Flash memory, RAM, Peripherals) start with lowest peripheral number (for example: STM_0) or memory address and end at the highest available peripheral number or memory address (for example: MPC574xC have 2 STM, ending with STM_1).

Table 1. MPC5748G Family Comparison[1]

Feature	MPC5747C	MPC5748C	MPC5746G	MPC5747G	MPC5748G
CPUs	e200z4 e200z2	e200z4 e200z2	e200z4 e200z4 e200z2	e200z4 e200z4 e200z2	e200z4 e200z4 e200z2
FPU	e200z4	e200z4	e200z4 e200z4	e200z4 e200z4	e200z4 e200z4
Maximum Operating Frequency[2]	160MHz (z4) 80MHz (z2)	160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)	160MHz (z4) 160MHz (z4) 80MHz (z2)
Flash memory	4 MB	6 MB	3 MB	4 MB	6 MB
EEPROM support	32 KB to 128 KB emulated		32 KB to 192 KB emulated		
RAM	512 KB	768 KB			
ECC	End to End				
SMPU	24 entry		32 entry		
DMA	32 channels				
10-bit ADC	48 Standard channels 32 External channels				
12-bit ADC	16 Precision channels 16 Standard channels 32 External channels				
AnalogComparator	3				
BCTU	1				
SWT	2		4[3]		
STM	2		3		
PIT-RTI	16 channels PIT 1 channels RTI				
RTC/API	Yes				
Total Timer I/O[4]	96 channels 16-bits				
LINFlexD	1 M/S, 15 M		1 M/S, 17 M		
FlexCAN	8 with optional CAN FD support				
DSPI/SPI	4 x DSPI 6 x SPI				

Table continues on the next page...

3.2 Ordering Information



Qualification Status
P = Engineering samples
S = Automotive qualified

PC = Power Architecture

Automotive Platform
57 = Power Architecture in 55nm

Core Version
4 = e200z4 Core Version (highest core version in the case of multiple cores)

Flash Memory Size
6 = 3 MB
7 = 4 MB
8 = 6 MB

Product Version
C = Body Control Feature Set
G = Gateway Feature Set

Optional fields
Blank = Feature not available
S = HSM (Security Module)
F = CAN FD
B = Both HSM and CAN FD
T = HSM and 2nd Ethernet
G = CAN FD and 2nd Ethernet
H = HSM, CAN FD, and 2nd Eternet

Fab and mask version indicator
K=TSMC Fab
#=Version of maskset
0=0N65H
1=1N81M
0A=0N78S

Package Code
KU = 176 LQFP EP
MJ = 256 MAPBGA
MN = 324 MAPBGA

CPU Frequency
2 = Each z4 operates up to 120 MHz
6 = Each z4 operates up to 160 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Temperature spec.
C = -40.C to +85.C Ta
V = -40.C to +105.C Ta
M = -40.C to +125.C Ta

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 5 for specific conditions

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 5. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[3, 4]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[5]	Decoupling pin for low power regulators[6]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[7]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 µF capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA. SeeThermal attributes

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 6. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	3.6	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[5, 6]	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
  - Control of external NPN ballast transistor
  - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 10. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{DD_FULL} 2, 3	RUN Full Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	219	292	mA
		T_a = 105°C	—	230	328	mA
		T_a = 125 °C	—	249	400	mA
I_{DD_GWY} 5, 6	RUN Gateway Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	183	260	mA
		T_a = 105°C	—	196	294	mA
		T_a = 125°C[4]	—	215	348	mA
$I_{DD\_BODY\_1}$ 7, 8	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	149	223	mA
		T_a = 105 °C	—	158	270	mA
		T_a = 125°C [4]	—	175	310	mA
IDD_BODY_2[9, 10]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	105	174	mA

Table continues on the next page...

Table 17. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 11)	38	132	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 11)	48	220	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn[SRC 1:0]= 10)	19	66	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn[SRC 1:0]= 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

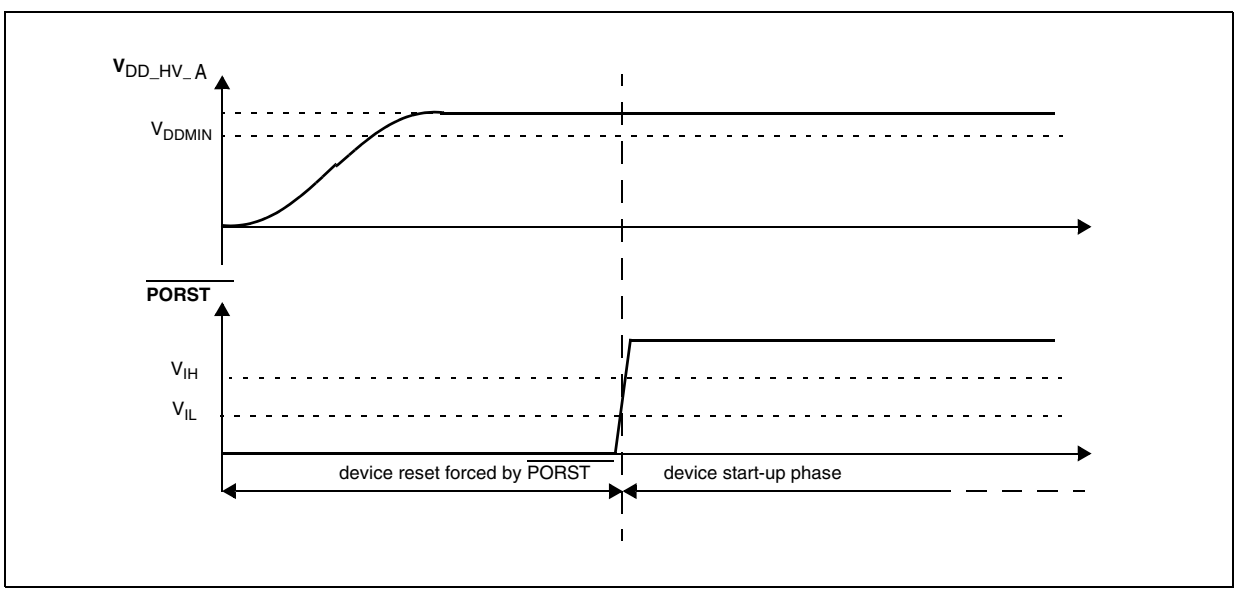


Figure 3. Start-up reset requirements

5.6 PORST electrical specifications

Table 19. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{PORST}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{PORST}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD\_HV\_A}$	—	V
V_{IL}	Input low level	—	0.35 x $V_{DD\_HV\_A}$	—	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

Table 36. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 37. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

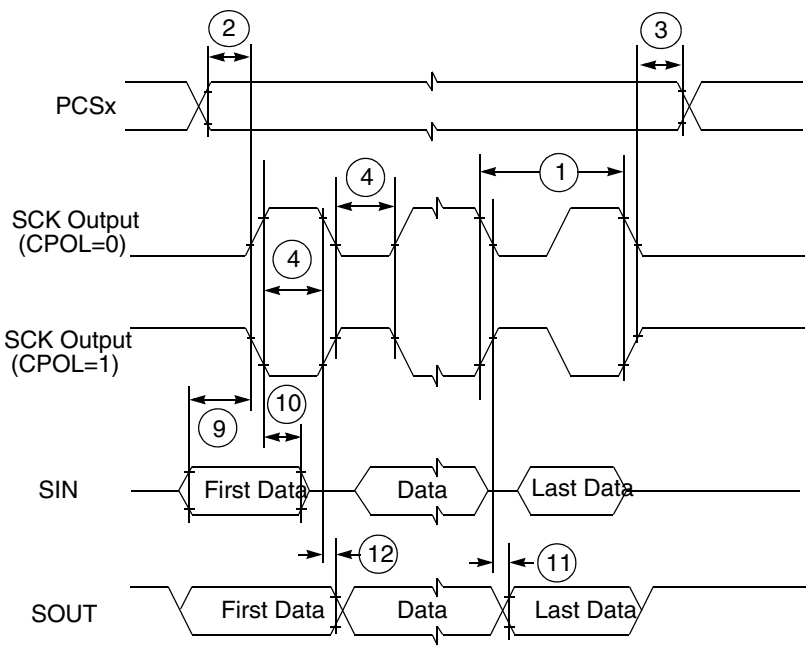


Figure 8. DSPI classic SPI timing — master, CPHA = 0

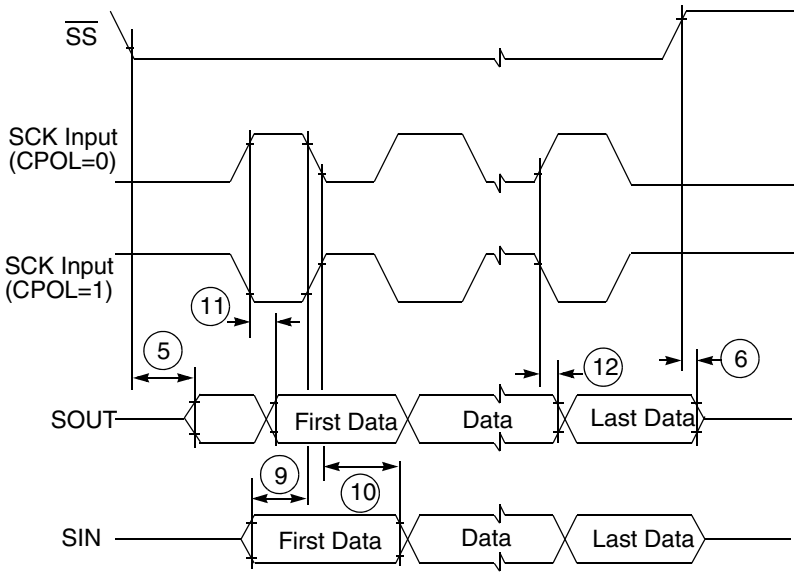


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

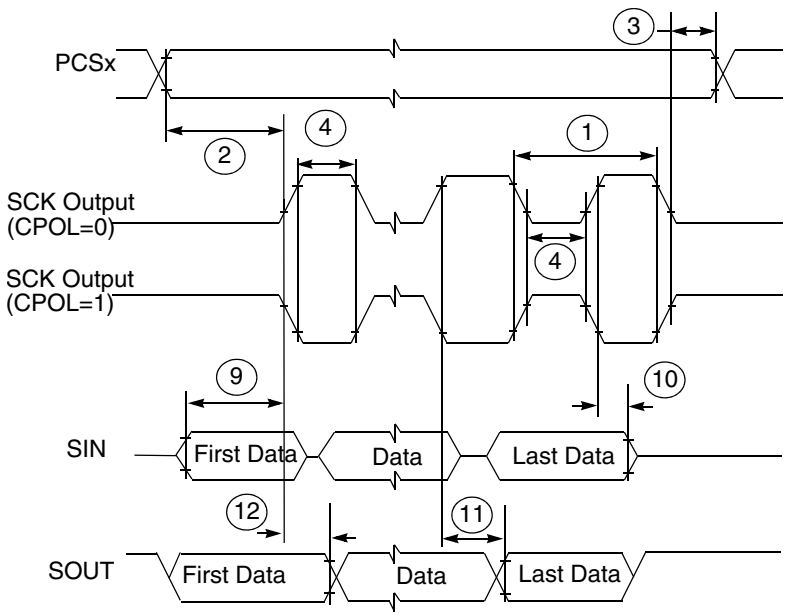


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

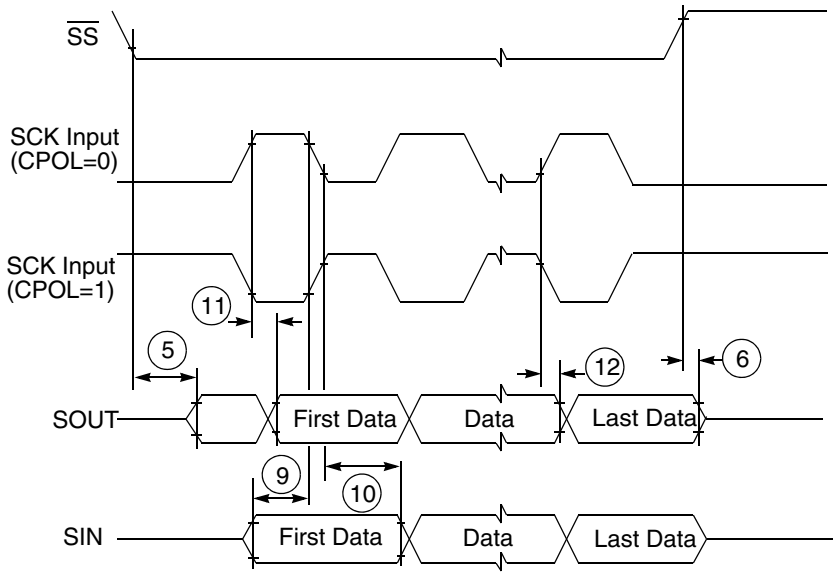


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

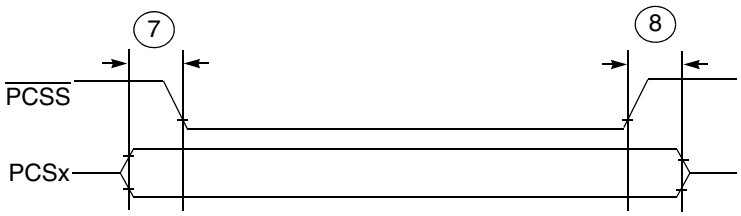


Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

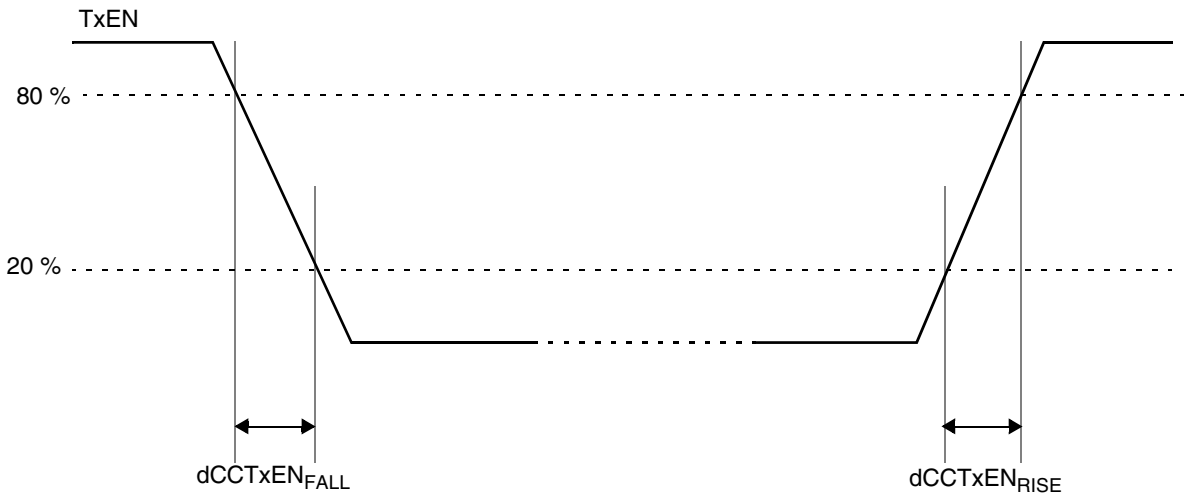


Figure 17. TxEN signal

Table 38. TxEN output characteristics[1]

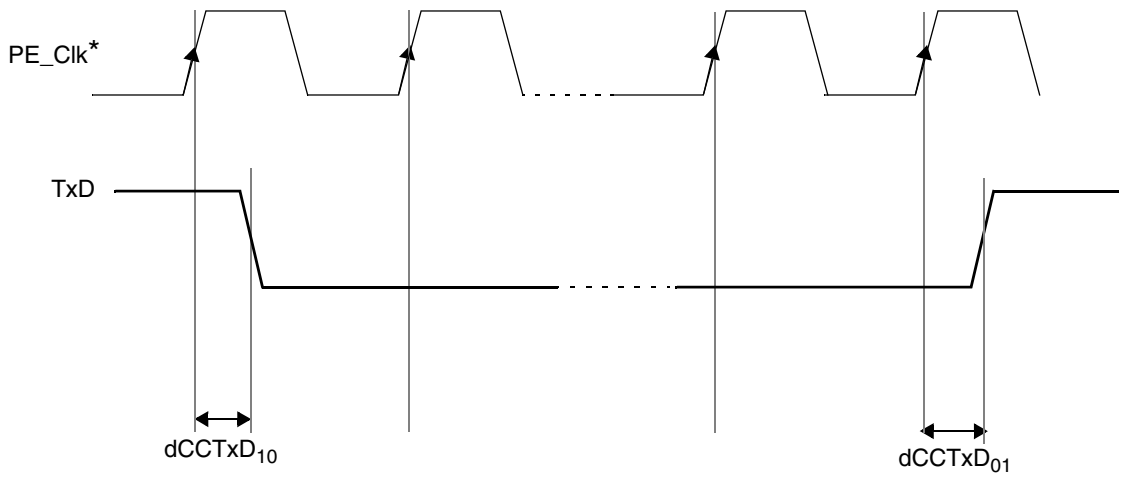
Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

Table 39. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 40. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 45. MLB 3-Pin 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	$t_{mck}r$		3	ns	$V_{IL\ to\ V_{IH}}$
MLBCLK fall time	$t_{mck}f$		3	ns	$V_{IH\ to\ V_{IL}}$
MLBCLK low time[1]	$t_{mck}l$	30 14	—	ns	256xFs 512xFs
MLBCLK high time	$t_{mck}h$	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	$t_{mck}l$	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	4	—	ns	2

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 46. MLB 3-Pin 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056 -	- 51.2	MHz MHz	1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz
MLBCLK rise time	f_{mckr}		1	ns	$V_{IL\ to}\ V_{IH}$
MLBCLK fall time	f_{mckf}		1	ns	$V_{IH\ to}\ V_{IL}$
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	2
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	3

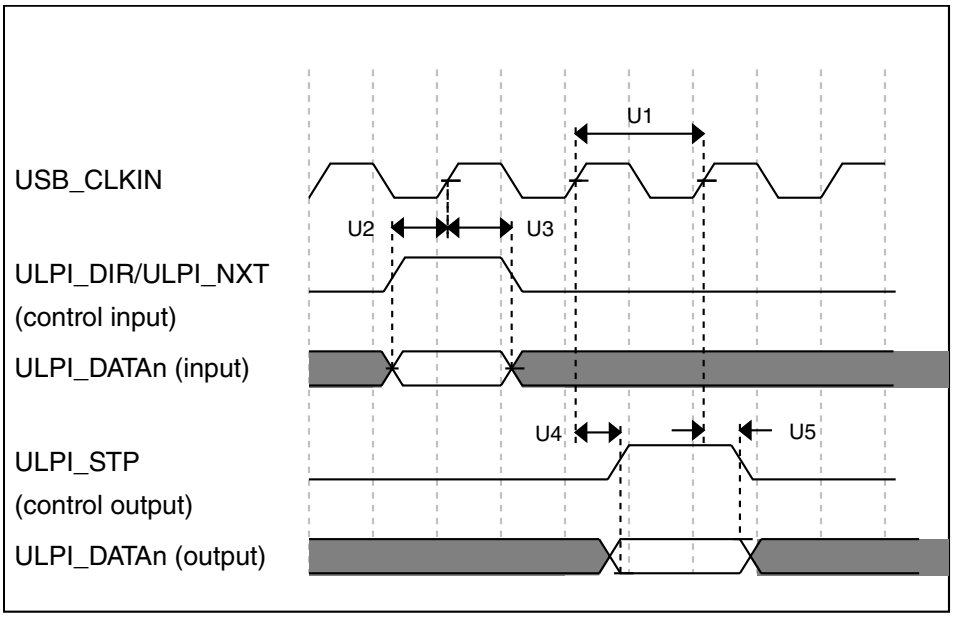


Figure 25. ULPI timing diagram

6.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 48. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

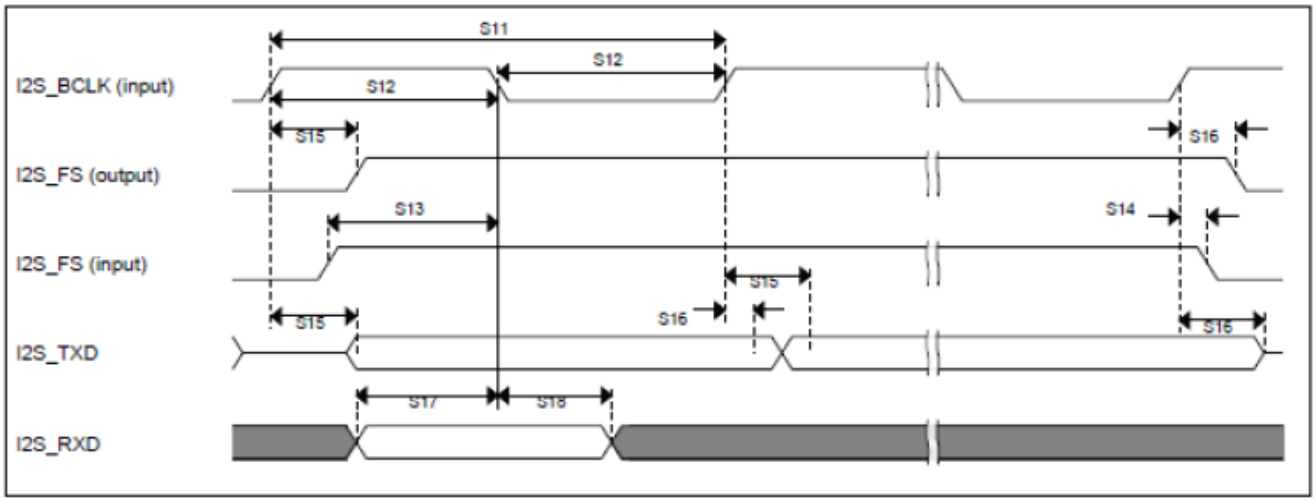


Figure 27. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 50. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time [2]	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20[3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1 Reset sequence duration

Table 54 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 54. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ [1]	Max	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	5.730	7.796		ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	0.111	0.182		ms
3	T_{ERLB}	External Reset Sequence Long, Unsecure Boot	5.729	7.793		ms
4	T_{FRL}	Functional Reset Sequence Long, Unsecure Boot	0.110	0.179		ms
5	T_{FRS}	Functional Reset Sequence Short, Unsecure Boot	0.007	0.009		ms

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

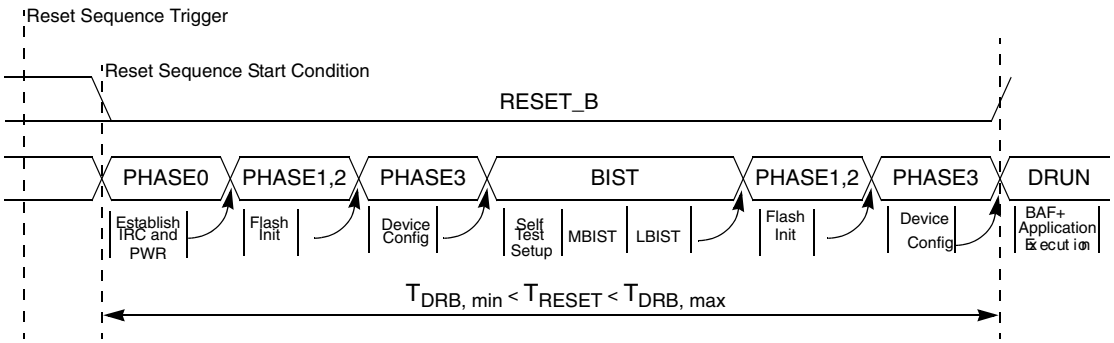


Figure 35. Destructive reset sequence, BIST enabled

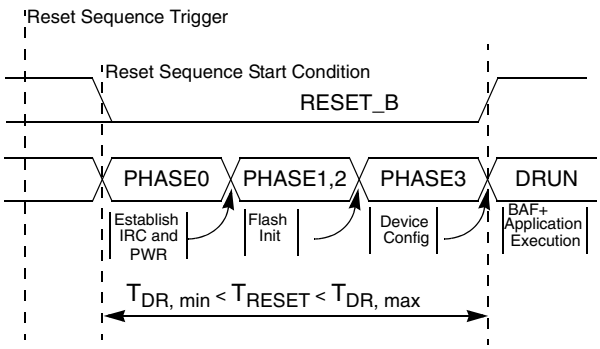


Figure 36. Destructive reset sequence, BIST disabled

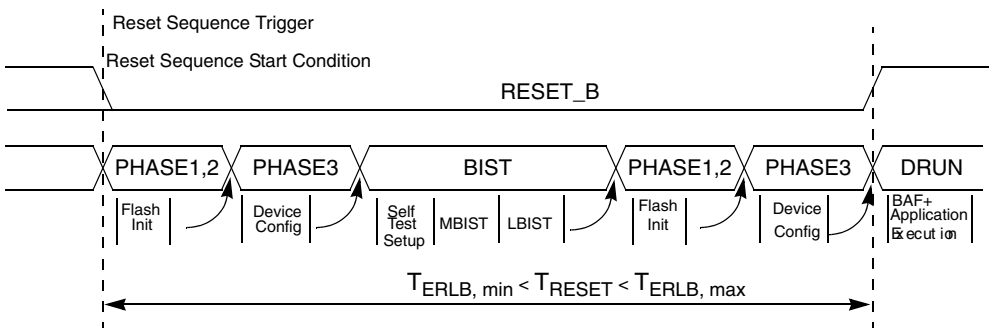


Figure 37. External reset sequence long, BIST enabled

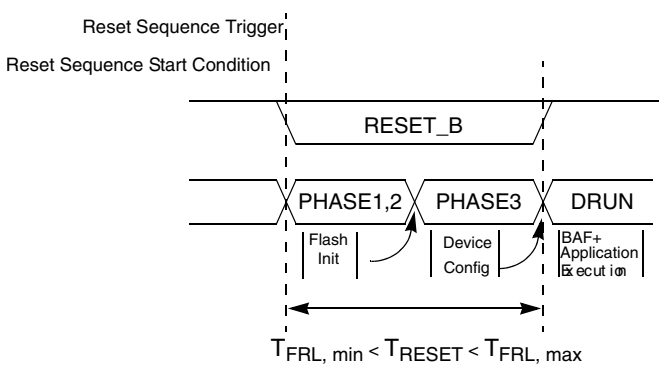


Figure 38. Functional reset sequence long

Table 56. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated VIH min and VIL max values in Main oscillator electrical characteristics • Replaced ipp_sre[1:0] by SIUL2_MSCRn[SRC 1:0] in AC specifications @ 3.3 V Range, DC electrical specifications @ 3.3V Range • Functional reset sequence short, unsecure boot corrected Reset sequence duration • Added NVM memory map and RAM memory map Family comparison • Added BAF execution duration section BAF execution duration • Supply names (VDD_LV, VSS_LV replace dvss, avss, dvdd, avdd) corrected in Jitter calculation table PLL electrical specifications • Updated Ordering information: Fab and Mask version indicator • Updated tpsus typical and max values Flash memory AC timing specifications • Added Notes on IBIS models use in AC specifications @3.3 V Range AC specifications @ 3.3 V Range • Updated Vol value in DC electrical specifications @ 3.3V Range DC electrical specifications @ 3.3V Range • Added Notes on IBIS models in Functional Pad AC Specifications @ 5 V Range AC specifications @ 5 V Range • Updated Vol values in DC electrical specifications @5V Range DC electrical specifications @ 5 V Range • Updated IDD Current values Supply current characteristics • Updated STANDBY current consumption with FIRC ON Supply current characteristics • Thermal numbers update for 256MAPBGA Thermal attributes • POR_HV Trim values removed Voltage monitor electrical characteristics • ADC analog pad leakage for 105 C added ADC electrical specifications • IDD STANDBY0, 1, 2 and 3 added Supply current characteristics
Rev5	July 31 2017	• Updated Standby2 value to 125 C in Standby current consumption characteristics • Corrected typo in Note from "case" to "cause" Voltage regulator electrical characteristics • Updated propagation delay from 14 to 21 in ACMP electrical specifications