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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	33MHz
Connectivity	I²C, IrDA, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	106
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2166vt33v

Appendix

2.1.2 Differences from H8/300 CPU

In comparison to the H8/300 CPU, the H8S/2000 CPU has the following enhancements.

- More general registers and control registers
  - Eight 16-bit extended registers and one 8-bit control register have been added.
- Extended address space
  - Normal mode* supports the same 64 kbytes address space as the H8/300 CPU.
  - Advanced mode supports a maximum 16 Mbytes address space.

Note: * Not available in this LSI.

- Enhanced addressing
  - The addressing modes have been enhanced to make effective use of the 16 Mbytes address space.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - Signed multiply and divide instructions have been added.
  - Two-bit shift and two-bit rotate instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions are executed twice as fast.

2.1.3 Differences from H8/300H CPU

In comparison to the H8/300H CPU, the H8S/2000 CPU has the following enhancements.

- Additional control register
  - One 8-bit control register has been added.
- Enhanced instructions
  - Addressing modes of bit-manipulation instructions have been enhanced.
  - Two-bit shift and two-bit rotate instructions have been added.
  - Instructions for saving and restoring multiple registers have been added.
  - A test and set instruction has been added.
- Higher speed
  - Basic instructions are executed twice as fast.

Table 2.7 Bit Manipulation Instructions (1)

Instruction	Size*	Function
BSET	B	1 → (<bit-No.> of <EAd>) Sets a specified bit in a general register or memory operand to 1. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BCLR	B	0 → (<bit-No.> of <EAd>) Clears a specified bit in a general register or memory operand to 0. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BNOT	B	~ (<bit-No.> of <EAd>) → (<bit-No.> of <EAd>) Inverts a specified bit in a general register or memory operand. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BTST	B	~ (<bit-No.> of <EAd>) → Z Tests a specified bit in a general register or memory operand and sets or clears the Z flag accordingly. The bit number is specified by 3-bit immediate data or the lower three bits of a general register.
BAND	B	C ∧ (<bit-No.> of <EAd>) → C Logically ANDs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIAND	B	C ∧ (<bit-No.> of <EAd>) → C Logically ANDs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.
BOR	B	C ∨ (<bit-No.> of <EAd>) → C Logically ORs the carry flag with a specified bit in a general register or memory operand and stores the result in the carry flag.
BIOR	B	C ∨ (~ <bit-No.> of <EAd>) → C Logically ORs the carry flag with the inverse of a specified bit in a general register or memory operand and stores the result in the carry flag. The bit number is specified by 3-bit immediate data.

[Legend]

*: Size refers to the operand size.

B: Byte

5.7.2 Instructions that Disable Interrupts

The instructions that disable interrupts are LDC, ANDC, ORC, and XORC. After any of these instructions are executed, all interrupts including NMI are disabled and the next instruction is always executed. When the I bit or UI bit is set by one of these instructions, the new value becomes valid two states after execution of the instruction ends.

5.7.3 Interrupts during Execution of EEPMOV Instruction

Interrupt operation differs between the EEPMOV.B instruction and the EEPMOV.W instruction.

With the EEPMOV.B instruction, an interrupt request (including NMI) issued during the transfer is not accepted until the move is completed.

With the EEPMOV.W instruction, if an interrupt request is issued during the transfer, interrupt exception handling starts at a break in the transfer cycle. The PC value saved on the stack in this case is the address of the next instruction. Therefore, if an interrupt is generated during execution of an EEPMOV.W instruction, the following coding should be used.

```
L1:   EEPMOV.W
      MOV.W     R4,R4
      BNE       L1
```

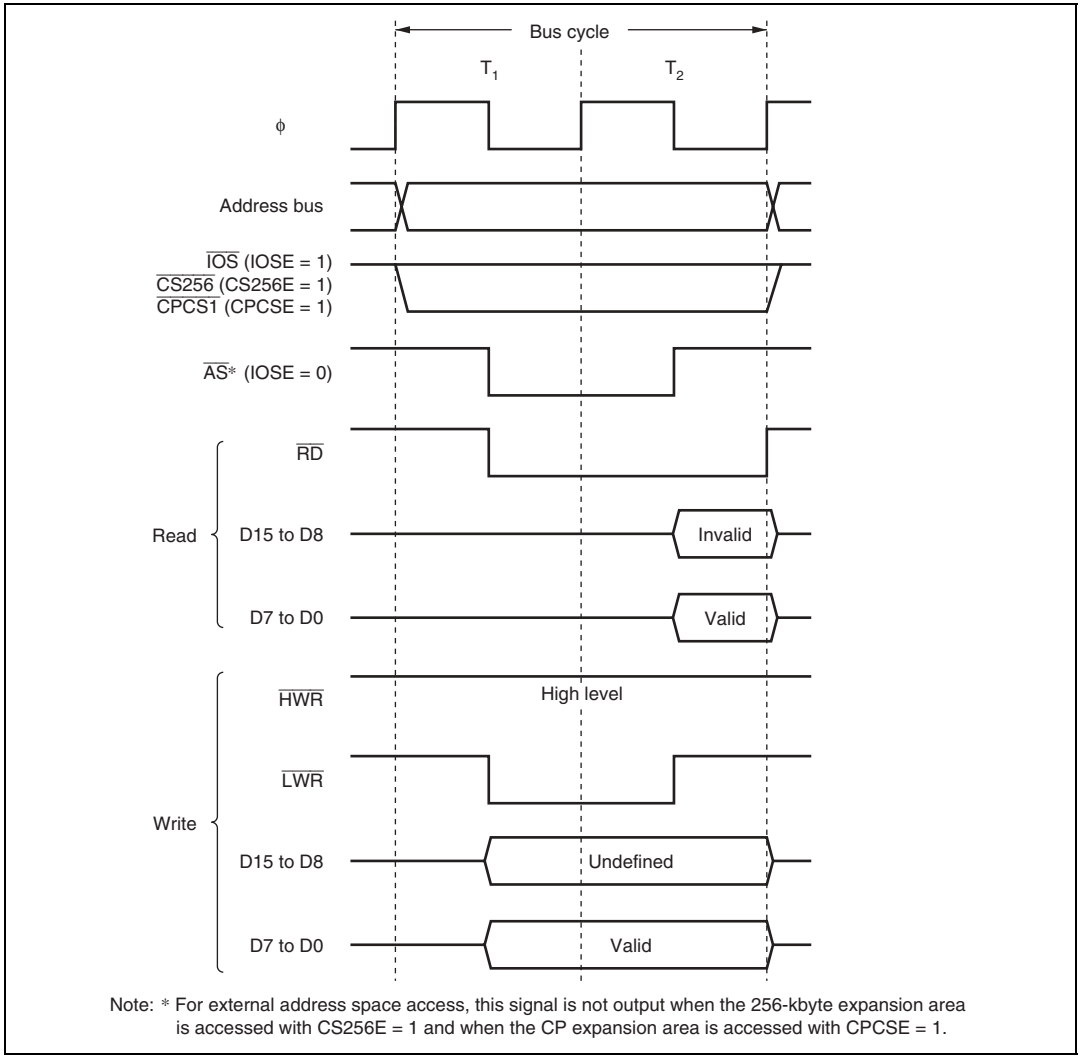
5.7.4 IRQ Status Registers (ISR16, ISR)

Since IRQnF may be set to 1 according to the pin status after a reset, the ISR16 and the ISR should be read after a reset, and then write 0 in IRQnF (n = 15 to 0).

6.3.4 Wait State Control Register 2 (WSCR2)

WSCR2 is used to specify the wait mode and number of wait states in access to the 256-kbyte extended area and CP extended area.

Bit	Bit Name	Initial Value	R/W	Description
7	WMS10	0	R/W	256-kbyte Extended Area Wait Mode Select 0 Selects the wait mode for access to the 256-kbyte extended area when the CS256E bit in SYSCR and the AST256 bit in WSCR are set to 1. 0: Program wait mode 1: Wait disabled mode
6	WC11	1	R/W	256-kbyte Extended Area Wait Count 1 and 0 Selects the number of program wait states to be inserted into the data cycle for access to the 256-kbyte extended area when the CS256E bit in SYSCR and the AST256 bit in WSCR are set to 1. 00: Program wait state is not inserted 01: 1 program wait state is inserted 10: 2 program wait states are inserted 11: 3 program wait states are inserted
5	WC10	1	R/W	
4	WMS21	0	R/W	CP Extended Area Wait Mode Select 1 and 0 Selects the wait mode for access to the CP extended area when the CPCSE and ASTCP bits in BCR2 are set to 1. 00: Program wait mode 01: Wait disabled mode 10: Pin wait mode 11: Pin auto-wait mode
3	WMS20	0	R/W	



Note: * For external address space access, this signal is not output when the 256-kbyte expansion area is accessed with CS256E = 1 and when the CP expansion area is accessed with CPCSE = 1.

Figure 6.8 Bus Timing for 16-Bit, 2-State Access Space (Odd Byte Access)

7.6.5 Interrupt Sources

An interrupt request is issued to the CPU when the DTC has completed the specified number of data transfers, or a data transfer for which the DISEL bit was set to 1. In the case of interrupt activation, the interrupt set as the activation source is generated. These interrupts to the CPU are subject to CPU mask level and priority level control by the interrupt controller.

In the case of software activation, a software-activated data transfer end interrupt (SWDTEND) is generated.

When the DISEL bit is 1 and one data transfer has been completed, or the specified number of transfers have been completed, after data transfer ends, the SWDTE bit is held at 1 and an SWDTEND interrupt is generated. The interrupt handling routine will then clear the SWDTE bit to 0.

When the DTC is activated by software, an SWDTEND interrupt is not generated during a data transfer wait or during data transfer even if the SWDTE bit is set to 1.

7.6.6 Operation Timing

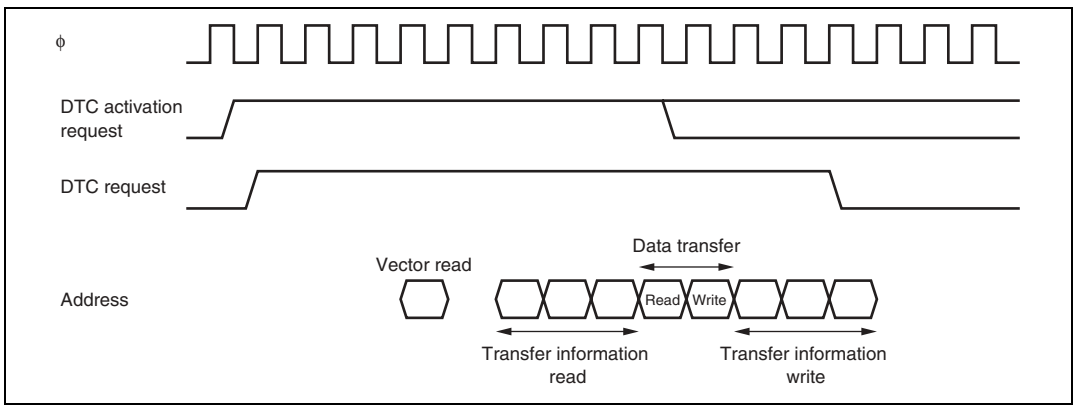


Figure 7.9 DTC Operation Timing (Example in Normal Mode or Repeat Mode)

8.2.4 Pin Functions

The relationship between register setting values and pin functions are as follows in each operating mode.

Extended Mode (EXPE = 1):

The function of port 2 pins is switched as shown below according to the combination of the CS256E and IOSE bits in SYSCR, the ADFULLE and CPCSE bits in BCR2 of BSC, and the P2nDDR bit.

Addresses 13 and 11 in the following table are expressed by the following logical expressions:

Address 13 = 1:$\overline{\text{ADFULLE}} \cdot \overline{\text{CS256E}} \cdot (\text{CPCSE} \mid \text{IOSE})$

Address 11 = 1:$\overline{\text{ADFULLE}} \cdot \overline{\text{CS256E}} \cdot \overline{\text{CPCSE}} \cdot \text{IOSE}$

P2nDDR	0		1		
ADMXE	0	1	0		1
Address 13	—	—	0	1	—
Pin function	P27 to P25 input pins	AD15 to AD13 input/output pins	A15 to A13 output pins	P27 to P25 output pins	AD15 to AD13 input/output pins

[Legend]
n = 7 to 5

P24DDR	0		1		
ADMXE	0	1	0		1
Address 11	—	—	0	1	—
Pin function	P24 input pin	AD12 input/output pin	A12 output pin	P24 output pin	AD12 input/output pin

P23DDR	0		1		
ADMXE	0	1	0		1
Address 11	—	—	0	1	—
Pin function	P23 input pin	AD11 input/output pin	A11 output pin	P23 output pin	AD11 input/output pin

8.11 Port B

Port B is an 8-bit multi-function input/output port that can also be used event counter input pin. Port B has the following registers.

- Port B data direction register (PBDDR)
- Port B output data register (PBODR)
- Port B input data register (PBPIN)

8.11.1 Port B Data Direction Register (PBDDR)

PBDDR is used to specify the input/output attribute of each pin of port B.

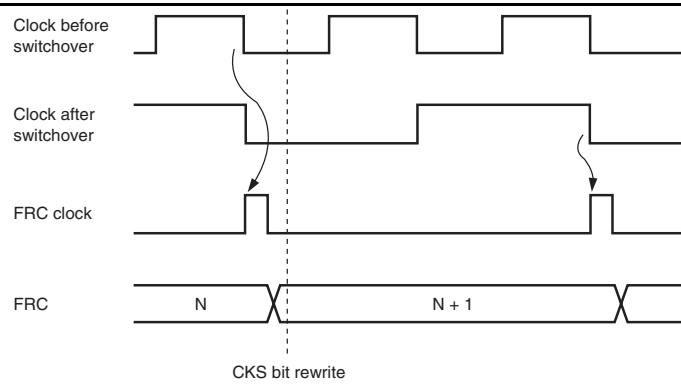
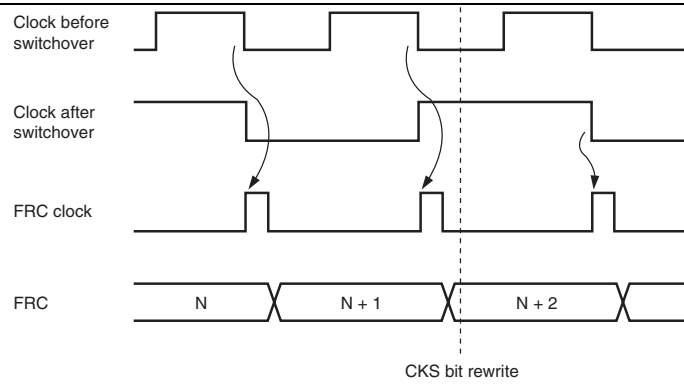
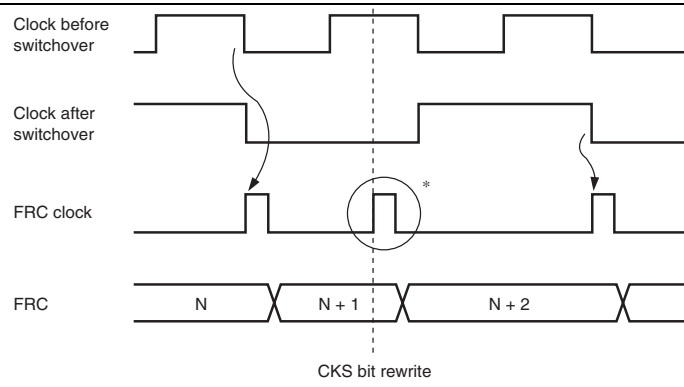
Bit	Bit Name	Initial Value	R/W	Description
7	PB7DDR	0	W	The corresponding port B pins are output ports when the PBDDR bits are set to 1, and input ports when cleared to 0.
6	PB6DDR	0	W	
5	PB5DDR	0	W	
4	PB4DDR	0	W	
3	PB3DDR	0	W	
2	PB2DDR	0	W	
1	PB1DDR	0	W	
0	PB0DDR	0	W	

8.11.2 Port B Output Data Register (PBODR)

PBODR stores output data for the port B pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7ODR	0	R/W	The PBODR register stores the output data for the pins that are used a general output port.
6	PB6ODR	0	R/W	
5	PB5ODR	0	R/W	
4	PB4ODR	0	R/W	
3	PB3ODR	0	R/W	
2	PB2ODR	0	R/W	
1	PB1ODR	0	R/W	
0	PB0ODR	0	R/W	

Table 11.3 Switching of Internal Clock and FRC Operation

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	FRC Operation
1	Switching from low to low	
2	Switching from low to high	
3	Switching from high to low	

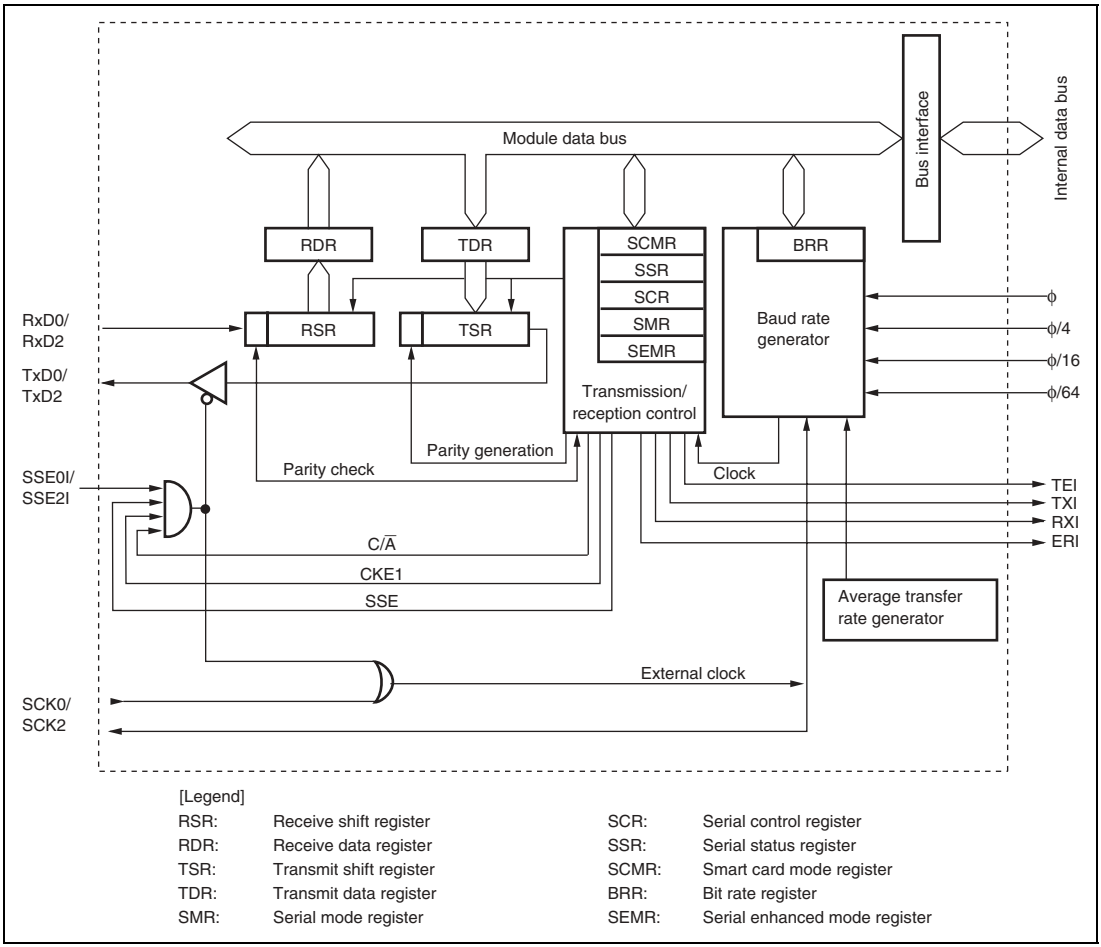


Figure 14.2 Block Diagram of SCI_0 and SCI_2

Bit	Bit Name	Initial Value	R/W	Description
1	CKE1	0	R/W	Clock Enable 1 and 0
0	CKE0	0	R/W	These bits select the clock source and SCK pin function. Asynchronous mode: 00: Internal clock (SCK pin functions as I/O port.) 01: Internal clock (Outputs a clock of the same frequency as the bit rate from the SCK pin.) 1*: External clock (Inputs a clock with a frequency 16 times the bit rate from the SCK pin.) Clock synchronous mode: 0*: Internal clock (SCK pin functions as clock output.) 1*: External clock (SCK pin functions as clock input.)

[Legend]

*: Don’t care

Table 14.13 IrCKS2 to IrCKS0 Bit Settings

Operating Frequency	Bit Rate (bps) (Upper Row) / Bit Interval × 3/16 (µs) (Lower Row)					
	2400	9600	19200	38400	57600	115200
ϕ (MHz)	78.13	19.53	9.77	4.88	3.26	1.63
5	011	011	011	011	011	011
6	100	100	100	100	100	100
6.144	100	100	100	100	100	100
7.3728	100	100	100	100	100	100
8	100	100	100	100	100	100
9.8304	100	100	100	100	100	100
10	100	100	100	100	100	100
12	101	101	101	101	101	101
12.288	101	101	101	101	101	101
14	101	101	101	101	101	101
14.7456	101	101	101	101	101	101
16	101	101	101	101	101	101
16.9344	101	101	101	101	101	101
17.2032	101	101	101	101	101	101
18	101	101	101	101	101	101
19.6608	101	101	101	101	101	101
20	101	101	101	101	101	101
25	110	110	110	110	110	110
33	110	110	110	110	110	110

14.11.3 CRC Operation Circuit Operation

The CRC operation circuit generates a CRC code for LSB-first/MSB-first communications. An example in which a CRC code for hexadecimal data H'F0 is generated using the $X^{16} + X^{12} + X^5 + 1$ polynomial with the G1 and G0 bits in CRCCR set to B'11 is shown below.

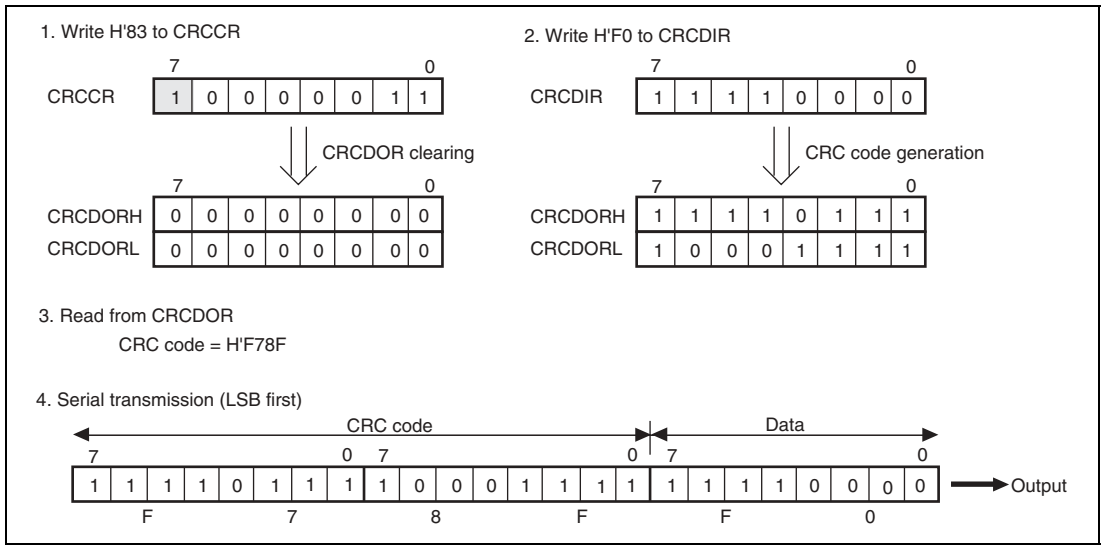


Figure 14.46 LSB-First Data Transmission

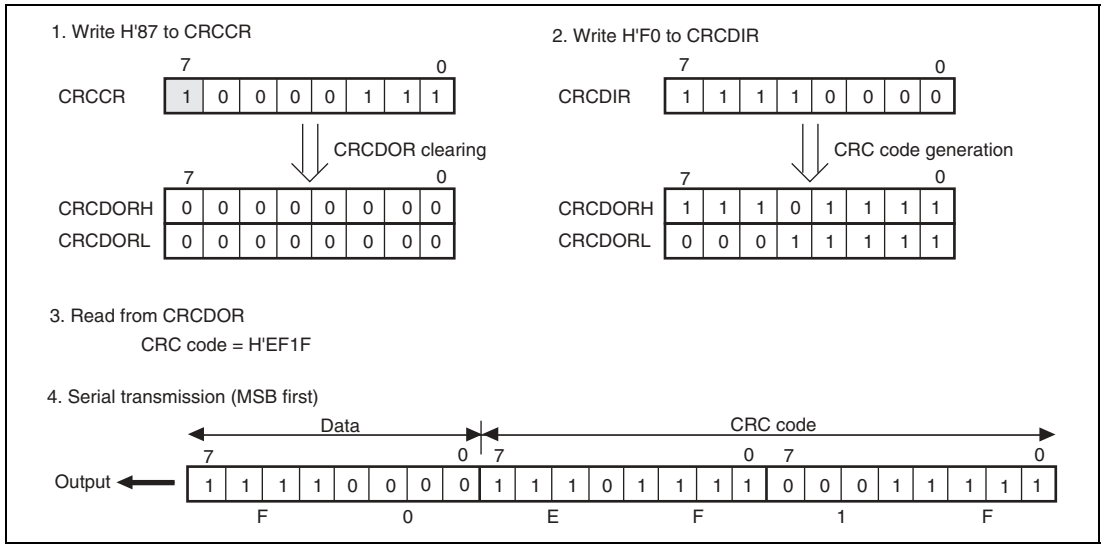


Figure 14.47 MSB-First Data Transmission

- I^2C bus format: addressing format with acknowledge bit
- Clocked synchronous serial format: non-addressing format without acknowledge bit, for master mode only

15.3.4 I^2C Bus Mode Register (ICMR)

ICMR sets the communication format and transfer rate. It can only be accessed when the ICE bit in ICCR is set to 1.

Bit	Bit Name	Initial Value	R/W	Description
7	MLS	0	R/W	MSB-First/LSB-First Select 0: MSB-first 1: LSB-first Set this bit to 0 when the I^2C bus format is used.
6	WAIT	0	R/W	Wait Insertion Bit This bit is valid only in master mode with the I^2C bus format. 0: Data and the acknowledge bit are transferred consecutively with no wait inserted. 1: After the fall of the clock for the final data bit (8th clock), the IRIC flag is set to 1 in ICCR, and a wait state begins (with SCL at the low level). When the IRIC flag is cleared to 0 in ICCR, the wait ends and the acknowledge bit is transferred. For details, refer to section 15.4.7, IRC Setting Timing and SCL Control.
5 4 3	CKS2 CKS1 CKS0	All 0	R/W	Transfer Clock Select These bits are used only in master mode. These bits select the required transfer rate, together with the IICX5 (channel 5), IICX4 (channel 4), and IICX3 (channel 3) bits in IICX3, and the IICX2 (channel 2), IICX1 (channel 1), and IICX0 (channel 0) bits in STCR. Refer to table 15.3.

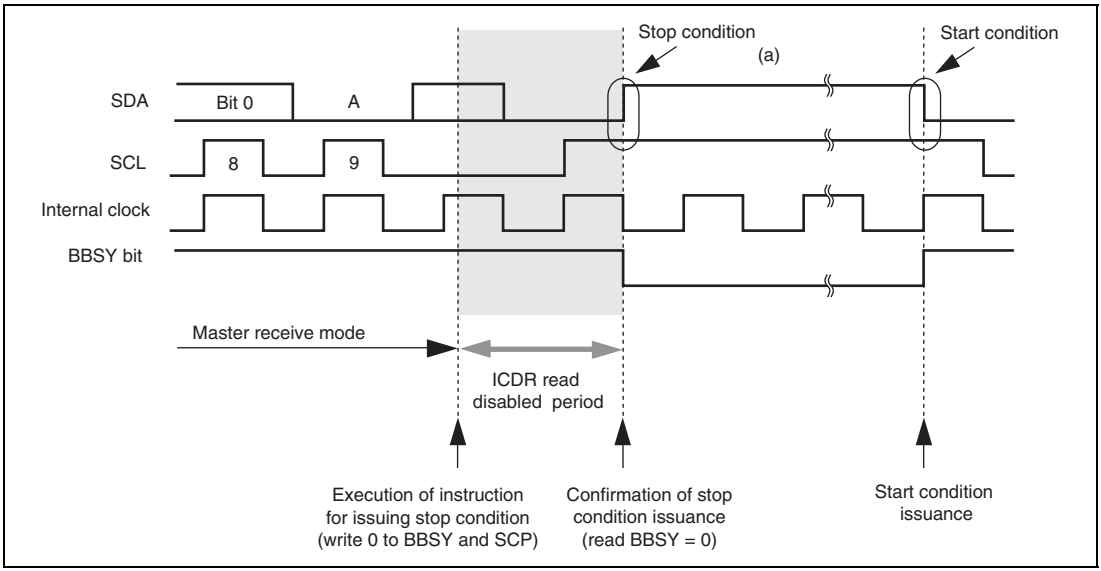


Figure 15.29 Notes on Reading Master Receive Data

Note: This restriction on usage can be canceled by setting the FNC1 and FNC0 bits to B′11 in ICXR.

8. Notes on start condition issuance for retransmission

   Figure 15.30 shows the timing of start condition issuance for retransmission, and the timing for subsequently writing data to ICDR, together with the corresponding flowchart. Write the transmit data to ICDR after the start condition for retransmission is issued and then the start condition is actually generated.

Bit	Bit Name	Initial Value	R/W		Description
			Slave	Host	
5	IRQBSY	0	R	—	SERIRQ Busy Indicates that the LPC interface's SERIRQ signal is engaged in transfer processing. 0: SERIRQ transfer frame wait state [Clearing conditions] • LPC hardware reset or LPC software reset • LPC hardware shutdown or LPC software shutdown • End of SERIRQ transfer frame 1: SERIRQ transfer processing in progress [Setting condition] • Start of SERIRQ transfer frame
4	LRSTB	0	R/W	—	LPC Software Reset Bit Resets the LPC interface. For the scope of initialization by an LPC reset, see section 16.4.6, LPC Interface Shutdown Function (LPCPD). 0: Normal state [Clearing conditions] • Writing 0 • LPC hardware reset 1: LPC software reset state [Setting condition] • Writing 1 after reading LRSTB = 0

18.7.3 Setting Range of Analog Power Supply and Other Pins

If conditions shown below are not met, the reliability of this LSI may be adversely affected.

- Analog input voltage range
  The voltage applied to analog input pin ANn during A/D conversion should be in the range AVSS ≤ ANn ≤ AVref (n = 0 to 7).
- Relation between AVCC, AVSS and VCC, VSS
  For the relationship between AVCC, AVSS and VCC, VSS, set AVSS = VSS, and AVCC = VCC is not always necessary. If the A/D converter is not used, the AVCC and AVSS pins must on no account be left open.
- AVref pin reference voltage specification range
  The reference voltage of the AVref pin should be in the range AVref ≤ AVCC.

18.7.4 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values. Also, digital circuitry must be isolated from the analog input signals (AN0 to AN7), and analog power supply (AVCC) by the analog ground (AVSS). Also, the analog ground (AVSS) should be connected at one point to a stable digital ground (VSS) on the board.

18.7.5 Notes on Noise Countermeasures

A protection circuit connected to prevent damage due to an abnormal voltage such as an excessive surge at the analog input pins (AN0 to AN7) should be connected between AVCC and AVSS as shown in figure 18.7. Also, the bypass capacitors connected to AVCC and AVref, and the filter capacitors connected to AN0 to AN7 must be connected to AVSS.

If a filter capacitor is connected, the input currents at the analog input pins (AN0 to AN7) are averaged, and so an error may arise. Also, when A/D conversion is performed frequently, as in scan mode, if the current charged and discharged by the capacitance of the sample-and-hold circuit in the A/D converter exceeds the current input via the input impedance (R_{in}), an error will arise in the analog input pin voltage. Careful consideration is therefore required when deciding the circuit constants.

20.1.3 Flash Memory MAT Configuration

This LSI's flash memory is configured by the 8-kbyte user boot MAT and 256-kbyte (H8S/2168), 384-kbyte (H8S/2167), or 512-kbytes (H8S/2166) user MAT.

The start address is allocated to the same address in the user MAT and user boot MAT. Therefore, when the program execution or data access is performed between two MATs, the MAT must be switched by using FMATS.

The user MAT or user boot MAT can be read in all modes. However, the user boot MAT can be programmed only in boot mode and programmer mode.

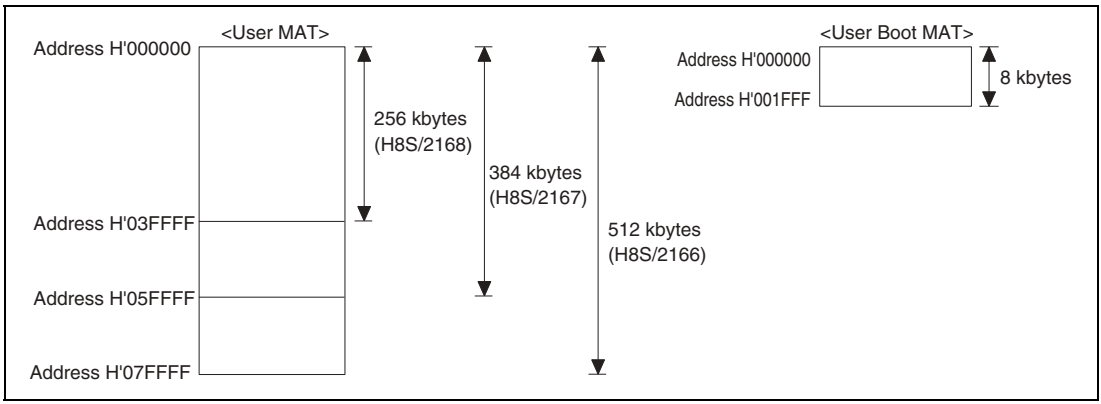


Figure 20.3 Flash Memory Configuration

The size of the user MAT is different from that of the user boot MAT. An address which exceeds the size of the 8-kbyte user boot MAT should not be accessed. If the attempt is made, data is read as undefined value.