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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	33MHz
Connectivity	I²C, IrDA, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	106
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2167vt33v

Table 2.5 Logic Operations Instructions

Instruction	Size*	Function
AND	B/W/L	Rd ∧ Rs → Rd, Rd ∧ #IMM → Rd Performs a logical AND operation on a general register and another general register or immediate data.
OR	B/W/L	Rd ∨ Rs → Rd, Rd ∨ #IMM → Rd Performs a logical OR operation on a general register and another general register or immediate data.
XOR	B/W/L	Rd ⊕ Rs → Rd, Rd ⊕ #IMM → Rd Performs a logical exclusive OR operation on a general register and another general register or immediate data.
NOT	B/W/L	~ Rd → Rd Takes the one's complement (logical complement) of data in a general register.

[Legend]

*: Size refers to the operand size.

B: Byte

W: Word

L: Longword

Table 2.6 Shift Instructions

Instruction	Size*	Function
SHAL	B/W/L	Rd (shift) → Rd
SHAR		Performs an arithmetic shift on data in a general register. 1-bit or 2 bit shift is possible.
SHLL	B/W/L	Rd (shift) → Rd
SHLR		Performs a logical shift on data in a general register. 1-bit or 2 bit shift is possible.
ROTL	B/W/L	Rd (rotate) → Rd
ROTR		Rotates data in a general register. 1-bit or 2 bit rotation is possible.
ROTXL	B/W/L	Rd (rotate) → Rd
ROTXR		Rotates data including the carry flag in a general register. 1-bit or 2 bit rotation is possible.

[Legend]

*: Size refers to the operand size.

B: Byte

W: Word

L: Longword

Bit	Bit Name	Initial Value	R/W	Description
3	ADFULLE	0	R/W	Address Output Full Enable Controls the address output in access to the IOS extended area, 256-kbyte extended area, or CP extended area. See section 8, I/O Ports. This is not supported while ADMXE = 1.
2	EXCKS	0	R/W	External Extension Clock Select Selects the operating clock used in external extended area access. 0: Medium-speed clock is selected as the operating clock 1: System clock (φ) is selected as the operating clock. The operating clock is switched in the bus cycle prior to external extended area access.
1	—	1	R/W	Reserved The initial value should not be changed.
0	CPCSE	0	R/W	CP Extended Area Enable Selects the extended area to be accessed. 0: External address space 1: CP extended area

8.1.2 Port 1 Data Register (P1DR)

P1DR stores output data for the port 1 pins.

Bit	Bit Name	Initial Value	R/W	Description
7	P17DR	0	R/W	P1DR stores output data for the port 1 pins that are used as the general output port. If a port 1 read is performed while the P1DDR bits are set to 1, the P1DR values are read. If a port 1 read is performed while the P1DDR bits are cleared to 0, the pin states are read.
6	P16DR	0	R/W	
5	P15DR	0	R/W	
4	P14DR	0	R/W	
3	P13DR	0	R/W	
2	P12DR	0	R/W	
1	P11DR	0	R/W	
0	P10DR	0	R/W	

8.1.3 Port 1 Pull-Up MOS Control Register (P1PCR)

P1PCR controls the port 1 built-in input pull-up MOSs.

Bit	Bit Name	Initial Value	R/W	Description
7	P17PCR	0	R/W	When the pins are in input state, the corresponding input pull-up MOS is turned on when a P1PCR bit is set to 1. In address-data multiplex extended bus mode is used, the initial value should not be changed.
6	P16PCR	0	R/W	
5	P15PCR	0	R/W	
4	P14PCR	0	R/W	
3	P13PCR	0	R/W	
2	P12PCR	0	R/W	
1	P11PCR	0	R/W	
0	P10PCR	0	R/W	

12.4 Operation

12.4.1 Pulse Output

Figure 12.3 shows an example for outputting an arbitrary duty pulse.

1. Clear the CCLR1 bit to 0 and set the CCLR0 bit to 1in TCR so that TCNT is cleared according to the compare match of TCORA.
2. Set the OS3 to OS0 bits in TCSR to B'0110 so that 1 is output according to the compare match of TCORA and 0 is output according to the compare match of TCORB.

According to the above settings, the waveforms with the TCORA cycle and TCORB pulse width can be output without the intervention of software.

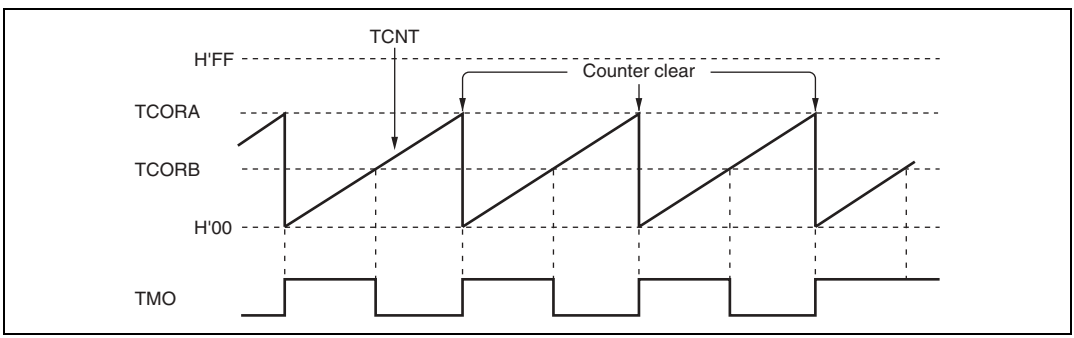


Figure 12.3 Pulse Output Example

12.9.4 Conflict between Compare-Matches A and B

If compare-matches A and B occur at the same time, the 8-bit timer operates in accordance with the priorities for the output states set for compare-match A and compare-match B, as shown in table 12.6.

Table 12.6 Timer Output Priorities

Output Setting	Priority
Toggle output	High
1 output	↑
0 output	
No change	Low

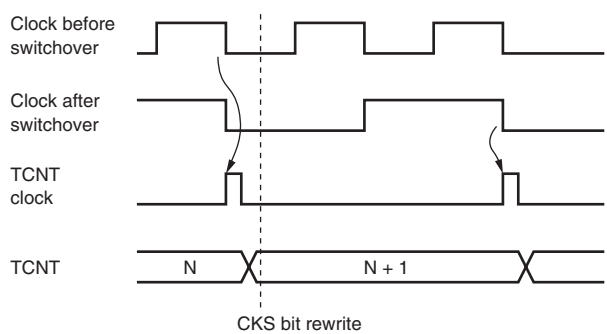
12.9.5 Switching of Internal Clocks and TCNT Operation

TCNT may increment erroneously when the internal clock is switched over. Table 12.7 shows the relationship between the timing at which the internal clock is switched (by writing to the CKS1 and CKS0 bits) and the TCNT operation.

When the TCNT clock is generated from an internal clock, the falling edge of the internal clock pulse is detected. If clock switching causes a change from high to low level, as shown in no. 3 in table 12.7, a TCNT clock pulse is generated on the assumption that the switchover is a falling edge, and TCNT is incremented.

Erroneous incrementation can also happen when switching between internal and external clocks.

Table 12.7 Switching of Internal Clocks and TCNT Operation

No.	Timing of Switchover by Means of CKS1 and CKS0 Bits	TCNT Clock Operation
1	Clock switching from low to low level*[1]	

Asynchronous Mode:

- Data length: 7 or 8 bits
- Stop bit length: 1 or 2 bits
- Parity: Even, odd, or none
- Receive error detection: Parity, overrun, and framing errors
- Break detection: Break can be detected by reading the RxD pin level directly in case of a framing error
- Average transfer rate generator (SCI_0 and SCI_2): 460.606 kbps or 115.152 kbps selectable at 10.667-MHz operation; 720 kbps, 460.784 kbps, 230.392 kbps, or 115.196 kbps selectable at 16- or 24-MHz operation; 230.392 kbps or 115.196 kbps selectable at 20-MHz operation; and 720 kbps selectable at 32-MHz operation

Clock Synchronous Mode:

- Data length: 8 bits
- Receive error detection: Overrun errors
- SCI channel selectable (SCI_0 and SCI_2): When SSE0I = 1, TxD0 = high-impedance state and SCK0 = fixed to high input; when SSE2I = 1, TxD2 = high-impedance state and SCK2 = fixed to high input

Smart Card Interface:

- An error signal can be automatically transmitted on detection of a parity error during reception
- Data can be automatically re-transmitted on detection of a error signal during transmission
- Both direct convention and inverse convention are supported

Figure 14.1 shows a block diagram of SCI_1, and figure 14.2 shows a block diagram of SCI_0 and SCI_2.

14.2 Input/Output Pins

Table 14.1 shows the input/output pins for each SCI channel.

Table 14.1 Pin Configuration

Channel	Symbol*	Input/Output	Function
0	SCK0	Input/Output	Channel 0 clock input/output
	RxD0	Input	Channel 0 receive data input
	TxD0	Output	Channel 0 transmit data output
	SSE0I	Input	Channel 0 stop input
1	SCK1	Input/Output	Channel 1 clock input/output
	RxD1/IrRxD	Input	Channel 1 receive data input (normal/IrDA)
	TxD1/IrTxD	Output	Channel 1 transmit data output (normal/IrDA)
2	SCK2	Input/Output	Channel 2 clock input/output
	RxD2	Input	Channel 2 receive data input
	TxD2	Output	Channel 2 transmit data output
	SSE2I	Input	Channel 2 stop input

Note: * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

- STR2

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
7 6 5 4	DBU27 DBU26 DBU25 DBU24	All 0	R/W	R	Defined by User The user can use these bits as necessary.
3	C/$\overline{D}$2	0	R	R	Command/Data When the host processor writes to an IDR2 register, bit 2 of the I/O address is written into this bit to indicate whether IDR2 contains data or a command. 0: Content of input data register (IDR2) is data 1: Content of input data register (IDR2) is a command
2	DBU22	0	R/W	R	Defined by User The user can use this bit as necessary.
1	IBF2	0	R	R	Input Data Register Full Indicates whether or not there is receive data in IDR2. This bit is an internal interrupt source to the slave processor (this LSI). 0: There is not receive data in IDR2 [Clearing condition] When the slave processor reads IDR2 1: There is receive data in IDR2 [Setting condition] When the host processor writes to IDR2 using I/O write cycle
0	OBF2	0	R/(W) *	R	Output Data Register Full Indicates whether or not there is transmit data in ODR2. 0: There is not transmit data in ODR2 [Clearing condition] When the host processor reads ODR2 using I/O read cycle, or the slave processor writes 0 to the OBF2 bit 1: There is transmit data in ODR2 [Setting condition] When the slave processor writes to ODR2

Note: * Only 0 can be written to clear the flag.

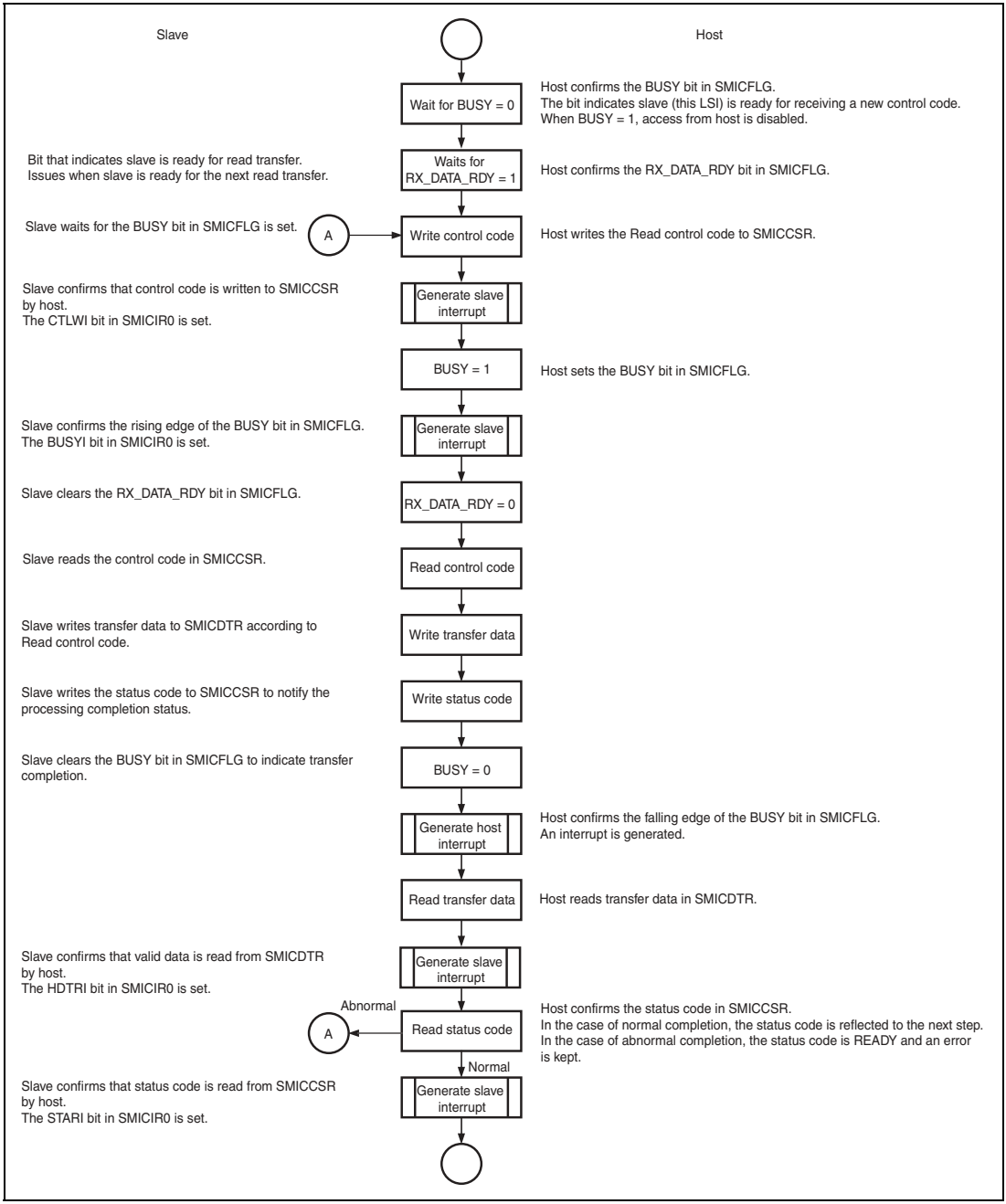


Figure 16.5 SMIC Read Transfer Flow

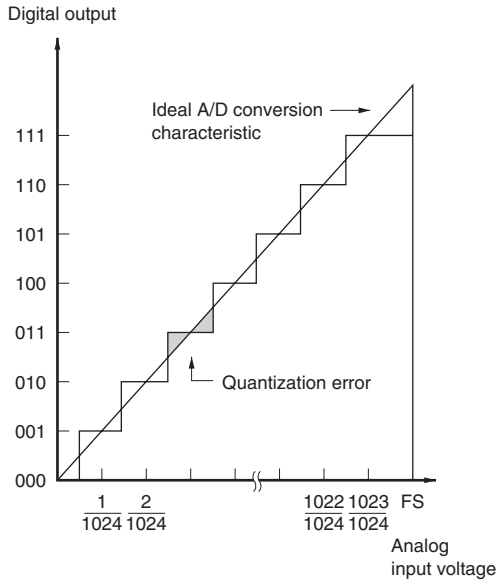


Figure 18.4 A/D Conversion Accuracy Definitions

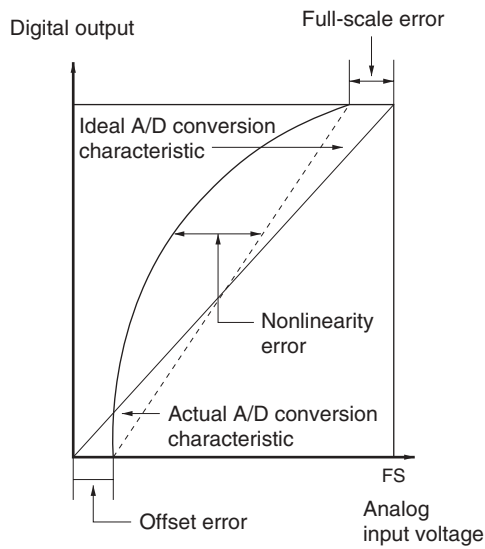


Figure 18.5 A/D Conversion Accuracy Definitions

20.1.2 Mode Comparison

The comparison table of programming and erasing related items about boot mode, user program mode, user boot mode, and programmer mode is shown in table 20.1.

Table 20.1 Comparison of Programming Modes

	Boot mode	User program mode	User boot mode	Programmer mode
Programming/ erasing environment	On-board	On-board	On-board	PROM programmer
Programming/ erasing enable MAT	User MAT User boot MAT	User MAT	User MAT	User MAT User boot MAT
All erasure	○ (Automatic)	○	○	○ (Automatic)
Block division erasure	○ *1	○	○	×
Program data transfer	From host via SCI	Via optional device	Via optional device	Via programmer
Reset initiation MAT	Embedded program storage MAT	User MAT	User boot MAT*2	—
Transition to user mode	Changing mode setting and reset	Changing FLSHE bit and FWE pin	Changing mode setting and reset	—

Notes: 1. All-erasure is performed. After that, the specified block can be erased.
2. Firstly, the reset vector is fetched from the embedded program storage MAT. After the flash memory related registers are checked, the reset vector is fetched from the user boot MAT.

- The user boot MAT can be programmed or erased only in boot mode and programmer mode.
- The user MAT and user boot MAT are erased in boot mode. Then, the user MAT and user boot MAT can be programmed by means of the command method. However, the contents of the MAT cannot be read until this state.
  Only user boot MAT is programmed and the user MAT is programmed in user boot mode or only user MAT is programmed because user boot mode is not used.
- The boot operation of the optional interface can be performed by the mode pin setting different from user program mode in user boot mode.

(4) Erasure Execution

When flash memory is erased, the erase-block number on the user MAT must be passed to the erasing program which is downloaded. This is set to the FEBS parameter (general register ER0).

One block is specified from the block number 0 to 15.

For details on the erasing processing procedure, see section 20.4.2, User Program Mode.

(a) Flash erase block select parameter (FEBS: general register ER0 of CPU)

This parameter specifies the erase-block number. The several block numbers cannot be specified.

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	—	—	Unused These bits should be cleared to H′0.
7	EB7	—	R/W	Erase Block Set the erase-block number in the range from 0 to 15. 0 corresponds to the EB0 block and 15 corresponds to the EB15 block. The number other than 0 to 11, 0 to 13, and 0 to 15 should not be set in the H8S/2168, H8S/2167, and H8S/2166, respectively.
6	EB6	—	R/W	
5	EB5	—	R/W	
4	EB4	—	R/W	
3	EB3	—	R/W	
2	EB2	—	R/W	
1	EB1	—	R/W	
0	EB0	—	R/W	

(f) Operating Clock Frequency Inquiry

The boot program will return the number of operating clock frequencies, and the maximum and minimum values.

Command

H'23

- Command, H'23, (1 byte): Inquiry regarding operating clock frequencies

Response

H'33	Size	Number of operating clock frequencies
Minimum value of operating clock frequency		Maximum value of operating clock frequency
...		
SUM		

- Response, H'33, (1 byte): Response to operating clock frequency inquiry
- Size (1 byte): The number of bytes that represents the minimum values, maximum values, and the number of frequencies.
- Number of operating clock frequencies (1 byte): The number of supported operating clock frequency types
  (e.g. when there are two operating clock frequency types, which are the main and peripheral clocks, the number of types will be H'02.)
- Minimum value of operating clock frequency (2 bytes): The minimum value of the multiplied or divided clock frequency.

  The minimum and maximum values represent the values in MHz, valid to the hundredths place of MHz, and multiplied by 100. (e.g. when the value is 20.00 MHz, it will be 2000, which is H'07D0.)
- Maximum value (2 bytes): Maximum value among the multiplied or divided clock frequencies.

  There are as many pairs of minimum and maximum values as there are operating clock frequencies.
- SUM (1 byte): Checksum

Pin No.	Pin Name	Input/Output	Bit No.
115	PB5	Input	69
		Enable	68
		Output	67
116	PB4	Input	66
		Enable	65
		Output	64
117	PB3	Input	63
		Enable	62
		Output	61
118	PB2	Input	60
		Enable	59
		Output	58
119	PB1	Input	57
		Enable	56
		Output	55
120	PB0	Input	54
		Enable	53
		Output	52
121	P30	Input	51
		Enable	50
		Output	49
122	P31	Input	48
		Enable	47
		Output	46
123	P32	Input	45
		Enable	44
		Output	43
124	P33	Input	42
		Enable	41
		Output	40
125	P34	Input	39
		Enable	38
		Output	37
126	P35	Input	36
		Enable	35
		Output	34
127	P36	Input	33
		Enable	32
		Output	31

Notes: 1. Boundary scan mode does not cover power-supply-related pins (VCC, VCL, VSS, AVCC, AVSS, and AVref).
2. Boundary scan mode does not cover clock-related pins (EXTAL, XTAL, and PFSEL).
3. Boundary scan mode does not cover reset- and standby-related pins ($\overline{\text{RES}}$, $\overline{\text{STBY}}$, and $\overline{\text{RESO}}$).
4. Boundary scan mode does not cover JTAG-related pins (ETCK, ETDI, ETDO, ETMS, and $\overline{\text{ETRST}}$).
5. Fix the $\overline{\text{MD2}}$ pin high.
6. Use the $\overline{\text{STBY}}$ pin in high state.

Function		High-Speed	Medium-Speed	Sleep	Module Stop	Watch	Sub-Active	Sub-Sleep	Software Standby	Hardware Standby
Peripheral modules	CRC	Function-ing	Function-ing	Function-ing	Function-ing/Halted (retained)	Halted (retained)	Halted (retained)	Halted (retained)	Halted (retained)	Halted (reset)
	D/A converter									
	SCI_0 to SCI_2				Function-ing/Halted (retained/ reset)	Halted (retained/ reset)	Halted (retained/ reset)	Halted (retained/ reset)	Halted (retained/ reset)	
	PWM				Function-ing/Halted (reset)	Halted (reset)	Halted (reset)	Halted (reset)	Halted (reset)	
	PWMX_0, PWMX_1									
	A/D converter									
	RAM			Function-ing (DTC)	Function-ing	Retained	Function-ing	Retained	Retained	Retained
	I/O			Function-ing				Function-ing		High impedance

Notes: Halted (retained) means that internal register values are retained. The internal state is operation suspended.

Halted (reset) means that internal register values and internal states are initialized.

In module stop mode, only modules for which a stop setting has been made are halted (reset or retained).

23.9 Subactive Mode

The CPU makes a transition to subactive mode when the SLEEP instruction is executed in high-speed mode with the SSBY bit in SBYCR set to 1, the DTON bit and LSON bit in LPWRCR set to 1, and the PSS bit in TCSR (WDT_1) set to 1. When an interrupt occurs in watch mode, and if the LSON bit in LPWRCR is 1, a direct transition is made to subactive mode. Similarly, if an interrupt occurs in subsleep mode, a transition is made to subactive mode.

In subactive mode, the CPU operates at a low speed based on the subclock and sequentially executes programs. Peripheral modules other than TMR_0, TMR_1, WDT_0, and WDT_1 are also stopped.

When operating the CPU in subactive mode, the SCK2 to SCK0 bits in SBYCR must be cleared to 0.

Subactive mode is exited by the SLEEP instruction, $\overline{\text{RES}}$ pin input, or $\overline{\text{STBY}}$ pin input.

When the SLEEP instruction is executed with the SSBY bit in SBYCR set to 1, the DTON bit in LPWRCR cleared to 0, and the PSS bit in TCSR (WDT_1) set to 1, the CPU exits subactive mode and a transition is made to watch mode. When the SLEEP instruction is executed with the SSBY bit in SBYCR cleared to 0, the LSON bit in LPWRCR set to 1, and the PSS bit in TCSR (WDT_1) set to 1, a transition is made to subsleep mode. When the SLEEP instruction is executed with the SSBY bit in SBYCR set to 1, the DTON bit and LSON bit in LPWRCR set to 10, and the PSS bit in TCSR (WDT_1) set to 1, a direct transition is made to high-speed mode.

For details of direct transitions, see section 23.11, Direct Transitions.

When the $\overline{\text{RES}}$ pin is driven low, system clock oscillation starts. Simultaneously with the start of system clock oscillation, the system clock is supplied to the entire LSI. Note that the $\overline{\text{RES}}$ pin must be held low until the clock oscillation is settled. If the $\overline{\text{RES}}$ pin is driven high after the clock oscillation settling time has passed, the CPU begins reset exception handling.

If the $\overline{\text{STBY}}$ pin is driven low, the LSI enters hardware standby mode.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
ICCR_5	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_5
ICSR_5	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	
ICDR_5	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SARX_5	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX	
ICMR_5	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0	
SAR_5	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
ICCR_3	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_3
ICSR_3	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	
ICDR_3	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SARX_3	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX	
ICMR_3	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0	
SAR_3	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
ICCR_2	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_2
ICSR_2	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	
ICDR_2	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SARX_2	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX	
ICMR_2	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0	
SAR_2	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
DADRA_1	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	PWMX_1
	DA5	DA4	DA3	DA2	DA1	DA0	CFS	—	
DACR_1	—	PWME	—	—	OEB	OEA	OS	CKS	
DADRB_1	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	
	DA5	DA4	DA3	DA2	DA1	DA0	CFS	REGS	
DACNT_1	UC7	UC6	UC5	UC4	UC3	UC2	UC1	UC0	
	UC8	UC9	UC10	UC11	UC12	UC13	—	REGS	
SEMR_0	SSE	—	—	ACS4	ABCS	ACS2	ACS1	ACS0	SCI_0
SEMR_2	SSE	—	—	ACS4	ABCS	ACS2	ACS1	ACS0	SCI_2
CRCCR	DORCLR	—	—	—	—	LMS	G1	G0	CRC
CRCDIR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
CRCDOR	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
ICXR_0	STOPIM	HNDS	ICDRF	ICDRE	ALIE	ALSL	FNC1	FNC0	IIC_0
ICXR_1	STOPIM	HNDS	ICDRF	ICDRE	ALIE	ALSL	FNC1	FNC0	IIC_1

25.6 Flash Memory Characteristics

Table 25.16 lists the flash memory characteristics.

Table 25.16 Flash Memory Characteristics

Condition: VCC = 3.0 V to 3.6 V, AVCC = 3.0 V to 3.6 V, Avref = 3.0 V to AVCC, VSS = AVSS = 0 V
Ta = 0°C to +75°C (operating temperature range for programming/erasing in regular specifications)
Ta = 0°C to +85°C (operating temperature range for programming/erasing in wide-range specifications)

- H8S/2168

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Programming time*1*2*4	t_P	—	3	30	ms/128 bytes	
Erase time*1*2*4	t_E	—	80	800	ms/4-kbyte block	
		—	500	5000	ms/32-kbyte block	
		—	1000	10000	ms/64-kbyte block	
Programming time (total)*1*2*4	Σt_P	—	5	15	s/256 kbytes	Ta = 25°C
Erase time (total)*1*2*4	Σt_E	—	5	15	s/256 kbytes	Ta = 25°C
Programming and Erase time (total)*1*2*4	Σt_{PE}	—	10	30	s/256 kbytes	Ta = 25°C
Reprogramming count*5	N_{WEC}	100*3	1000	—	Times	
Data retention time*4	t_{DRP}	10	—	—	Years	

Notes: 1. Programming and erase time depends on the data.
2. Programming and erase time do not include data transfer time.
3. This value indicates the minimum number of which the flash memory are reprogrammed with all characteristics guaranteed. (The guaranteed value ranges from 1 to the minimum number.)
4. This value indicates the characteristics while the flash memory is reprogrammed within the specified range (including the minimum number).
5. Reprogramming count in each erase block.