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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	H8S/2000
Core Size	16-Bit
Speed	33MHz
Connectivity	I²C, IrDA, LPC, SCI, SmartCard
Peripherals	POR, PWM, WDT
Number of I/O	106
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TQFP
Supplier Device Package	144-TQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2168vt33v

5.6.2 Interrupt Control Mode 1

In interrupt control mode 1, mask control is applied to three levels for IRQ and on-chip peripheral module interrupt requests by comparing the I and UI bits in CCR in the CPU, and the ICR setting.

1. An interrupt request with interrupt control level 0 is accepted when the I bit in CCR is cleared to 0. When the I bit is set to 1, the interrupt request is held pending.

   EVENTI, KIN, and WUE interrupts are enabled or disabled by the I bit.
2. An interrupt request with interrupt control level 1 is accepted when the I bit or UI bit in CCR is cleared to 0. When both I and UI bits are set to 1, the interrupt request is held pending.

For instance, the state when the interrupt enable bit corresponding to each interrupt is set to 1, and ICRA to ICRD are set to H'20, H'00, H'00, and H'00, respectively (IRQ2 and IRQ3 interrupts are set to interrupt control level 1, and other interrupts are set to interrupt control level 0) is shown below. Figure 5.6 shows a state transition diagram.

1. All interrupt requests are accepted when I = 0. (Priority order: NMI > IRQ2 > IRQ3 > IRQ0 > IRQ1 > address break …)
2. Only NMI, IRQ2, IRQ3, and address break interrupt requests are accepted when I = 1 and UI = 0.
3. Only NMI and address break interrupt requests are accepted when I = 1 and UI = 1.

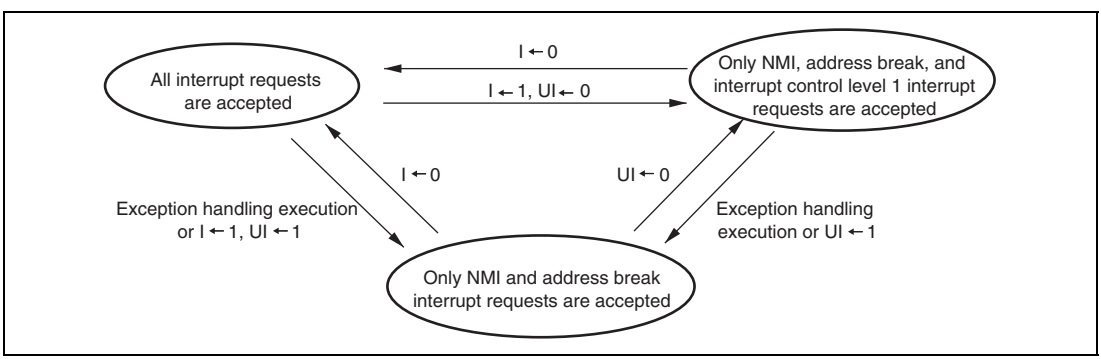

Figure 5.6 State Transition in Interrupt Control Mode 1

Figure 5.7 shows a flowchart of the interrupt acceptance operation.

8.15.3 Port F Input Data Register (PFPIN)

PFPIN indicates the pin states of port F.

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	—	—	Reserved. When this bit is read, an undefined value is returned.
2	PF2PIN	Undefined*	R	When PFPIN is read, the pin states are returned.
1	PF1PIN	Undefined*	R	This register is assigned to the same address as that of PFDDR. When this register is written to, data is written to PFDDR and the port F setting is then changed.
0	PF0PIN	Undefined*	R	

Note: The initial value of these pins is determined in accordance with the state of pins PF2 to PF0.

8.15.4 Pin Functions

Port F is a 3-bit input/output port that functions as a PWM output. The relationship between the register settings and pin functions is depicted below.

- PF2/ExPW2, PF1/ExPW1, PF0/ExPW0

  The pin function is switched as shown below according to the combination of the OEn bit in PWOERA of PWM, the PWMS bit in PTCNT0, and PFnDDR bit.

PFnDDR	0		1		—
PWMS	0	1	0	1	1
OEn	—	0	—	0	1
Pin Function	PFn input pin		PFn output pin		PWn output pin

[Legend]
n = 2 to 0

11.3.6 Timer Interrupt Enable Register (TIER)

TIER enables and disables interrupt requests.

Bit	Bit Name	Initial Value	R/W	Description
7	ICIAE	0	R/W	Input Capture Interrupt A Enable Selects whether to enable input capture interrupt A request (ICIA) when input capture flag A (ICFA) in TCSR is set to 1. 0: ICIA requested by ICFA is disabled 1: ICIA requested by ICFA is enabled
6	ICIBE	0	R/W	Input Capture Interrupt B Enable Selects whether to enable input capture interrupt B request (ICIB) when input capture flag B (ICFB) in TCSR is set to 1. 0: ICIB requested by ICFB is disabled 1: ICIB requested by ICFB is enabled
5	ICICE	0	R/W	Input Capture Interrupt C Enable Selects whether to enable input capture interrupt C request (ICIC) when input capture flag C (ICFC) in TCSR is set to 1. 0: ICIC requested by ICFC is disabled 1: ICIC requested by ICFC is enabled
4	ICIDE	0	R/W	Input Capture Interrupt D Enable Selects whether to enable input capture interrupt D request (ICID) when input capture flag D (ICFD) in TCSR is set to 1. 0: ICID requested by ICFD is disabled 1: ICID requested by ICFD is enabled
3	OCIAE	0	R/W	Output Compare Interrupt A Enable Selects whether to enable output compare interrupt A request (OCIA) when output compare flag A (OCFA) in TCSR is set to 1. 0: OCIA requested by OCFA is disabled 1: OCIA requested by OCFA is enabled

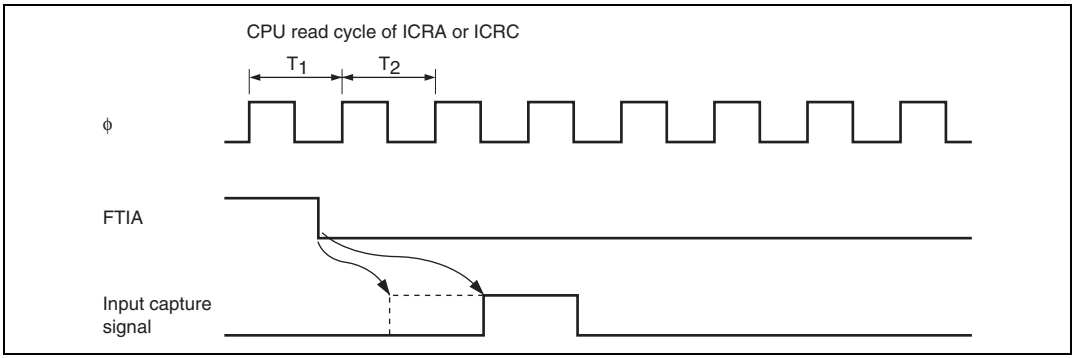

Figure 11.10 Buffered Input Capture Timing (BUFEA = 1)

11.5.6 Timing of Input Capture Flag (ICF) Setting

The input capture flag, ICFA to ICFD, is set to 1 by the input capture signal. The FRC value is simultaneously transferred to the corresponding input capture register (ICRA to ICRD). Figure 11.11 shows the timing of setting the ICFA to ICFD flag.

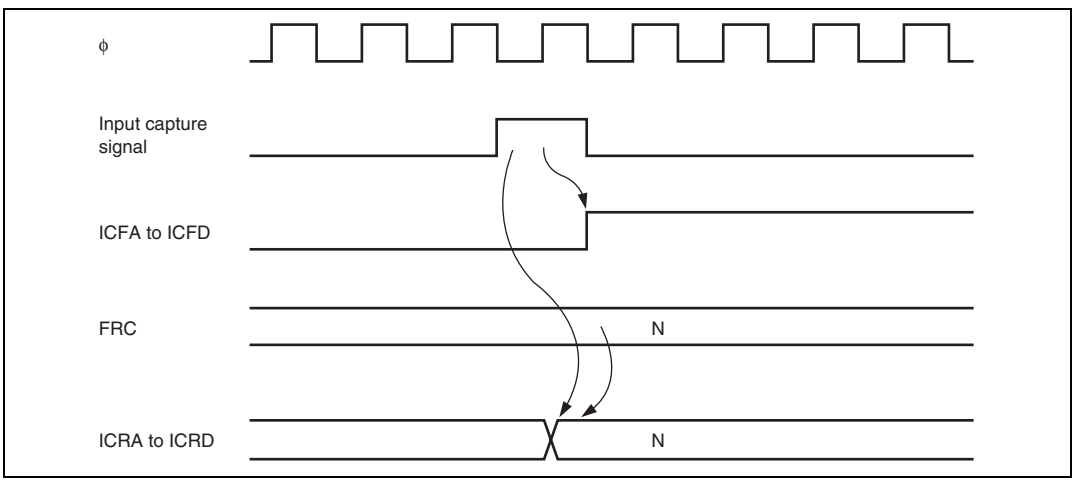

Figure 11.11 Timing of Input Capture Flag (ICFA to ICFD) Setting

13.4.3 $\overline{\text{RESO}}$ Signal Output Timing

When TCNT overflows in watchdog timer mode, the OVF bit in TCSR is set to 1. When the RST/$\overline{\text{NMI}}$ bit is 1 here, the internal reset signal is generated for the entire LSI. At the same time, the low level signal is output from the $\overline{\text{RESO}}$ pin. The timing is shown in figure 13.5.

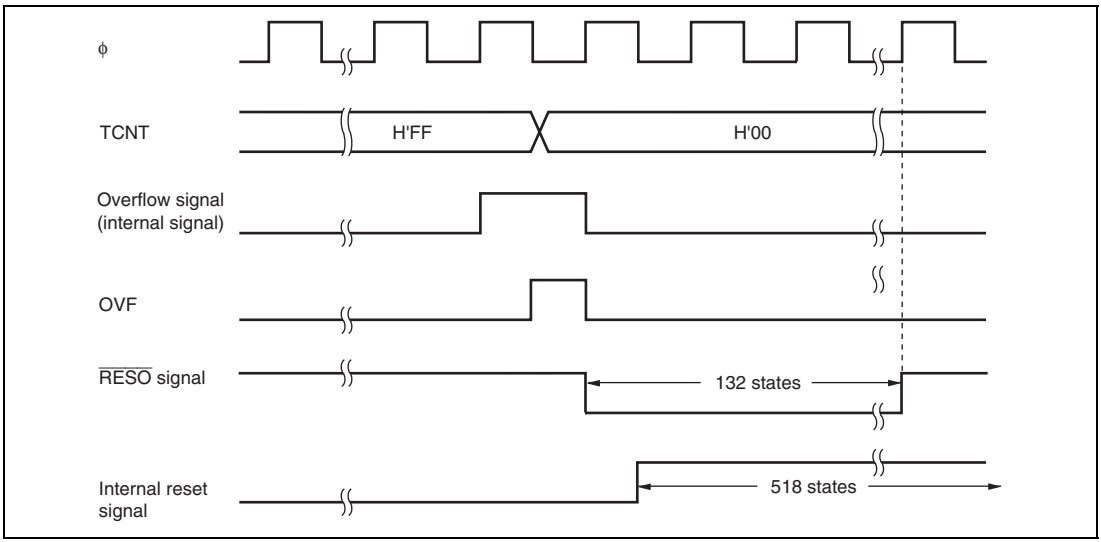

Figure 13.5 Output Timing of $\overline{\text{RESO}}$ signal

14.2 Input/Output Pins

Table 14.1 shows the input/output pins for each SCI channel.

Table 14.1 Pin Configuration

Channel	Symbol*	Input/Output	Function
0	SCK0	Input/Output	Channel 0 clock input/output
	RxD0	Input	Channel 0 receive data input
	TxD0	Output	Channel 0 transmit data output
	SSE0I	Input	Channel 0 stop input
1	SCK1	Input/Output	Channel 1 clock input/output
	RxD1/IrRxD	Input	Channel 1 receive data input (normal/IrDA)
	TxD1/IrTxD	Output	Channel 1 transmit data output (normal/IrDA)
2	SCK2	Input/Output	Channel 2 clock input/output
	RxD2	Input	Channel 2 receive data input
	TxD2	Output	Channel 2 transmit data output
	SSE2I	Input	Channel 2 stop input

Note: * Pin names SCK, RxD, and TxD are used in the text for all channels, omitting the channel designation.

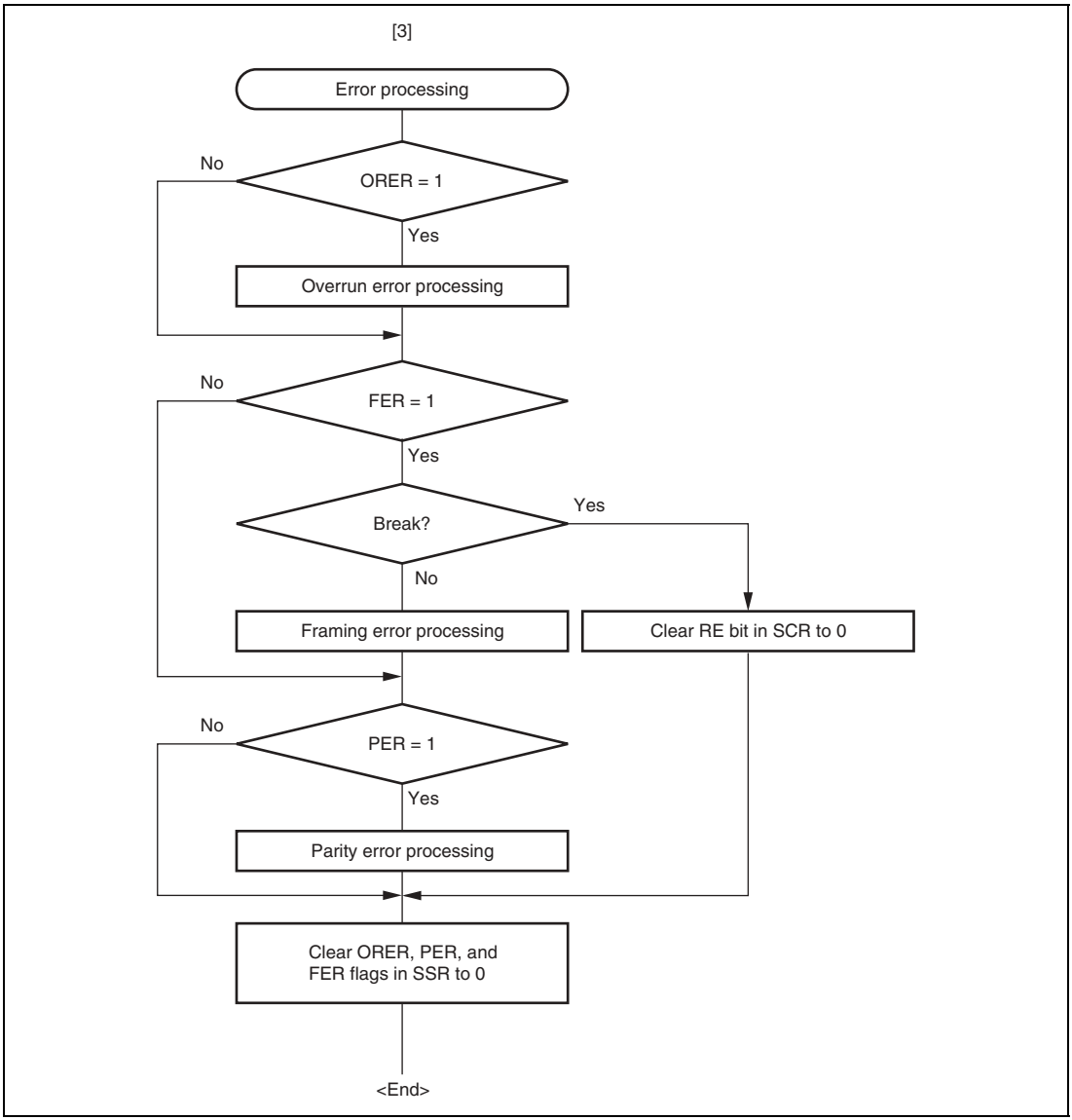

Figure 14.12 Sample Serial Reception Flowchart (2)

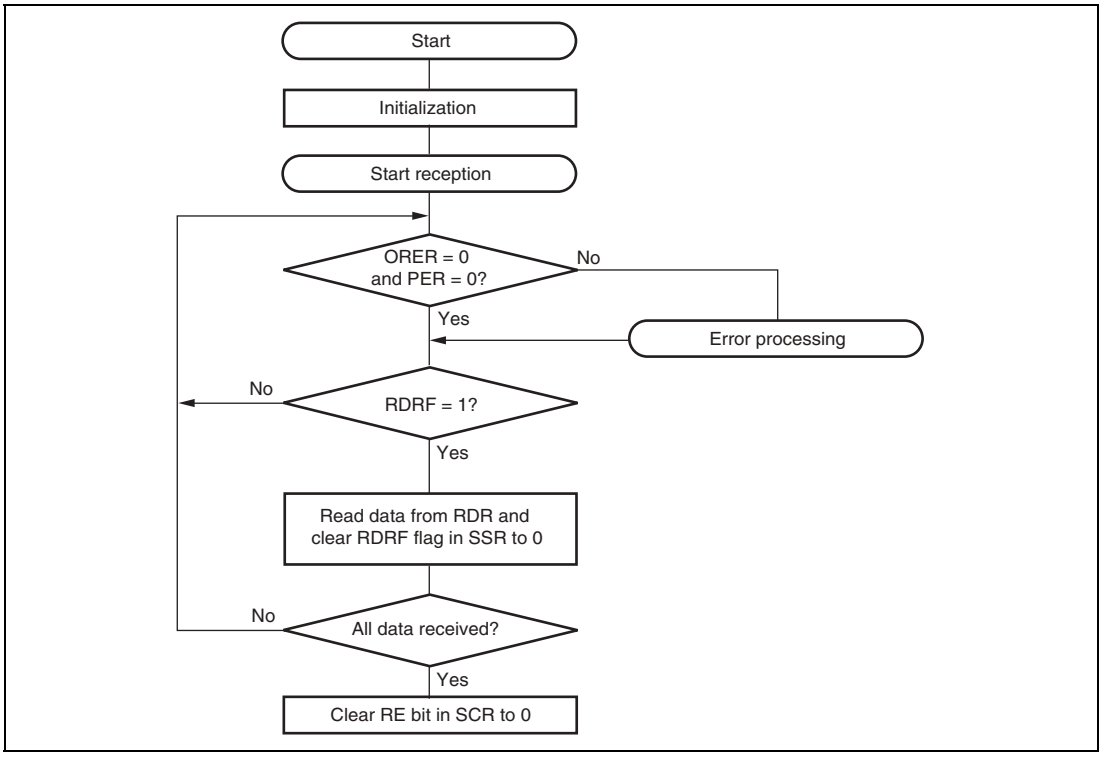

Figure 14.33 Sample Reception Flowchart

14.7.8 Clock Output Control

Clock output can be fixed using the CKE1 and CKE0 bits in SCR when the GM bit in SMR is set to 1. Specifically, the minimum width of a clock pulse can be specified.

Figure 14.34 shows an example of clock output fixing timing when the CKE0 bit is controlled with GM = 1 and CKE1 = 0.

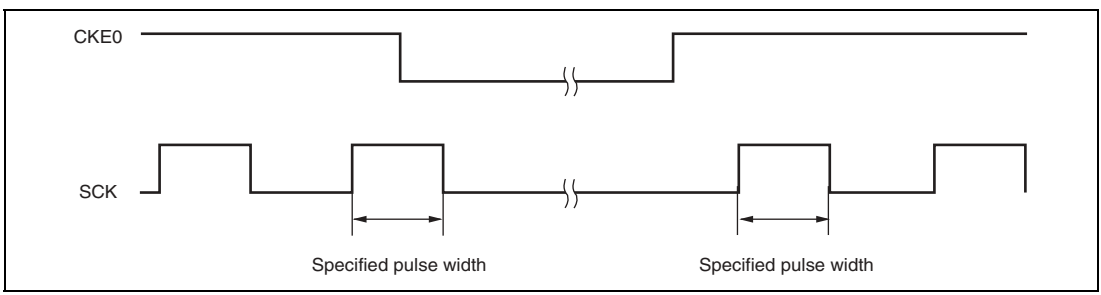

Figure 14.34 Clock Output Fixing Timing

Figure 15.1 shows a block diagram of the I²C bus interface. Figure 15.2 shows an example of I/O pin connections to external circuits. Since I²C bus interface I/O pins are different in structure from normal port pins, they have different specifications for permissible applied voltages. For details, see section 25, Electrical Characteristics.

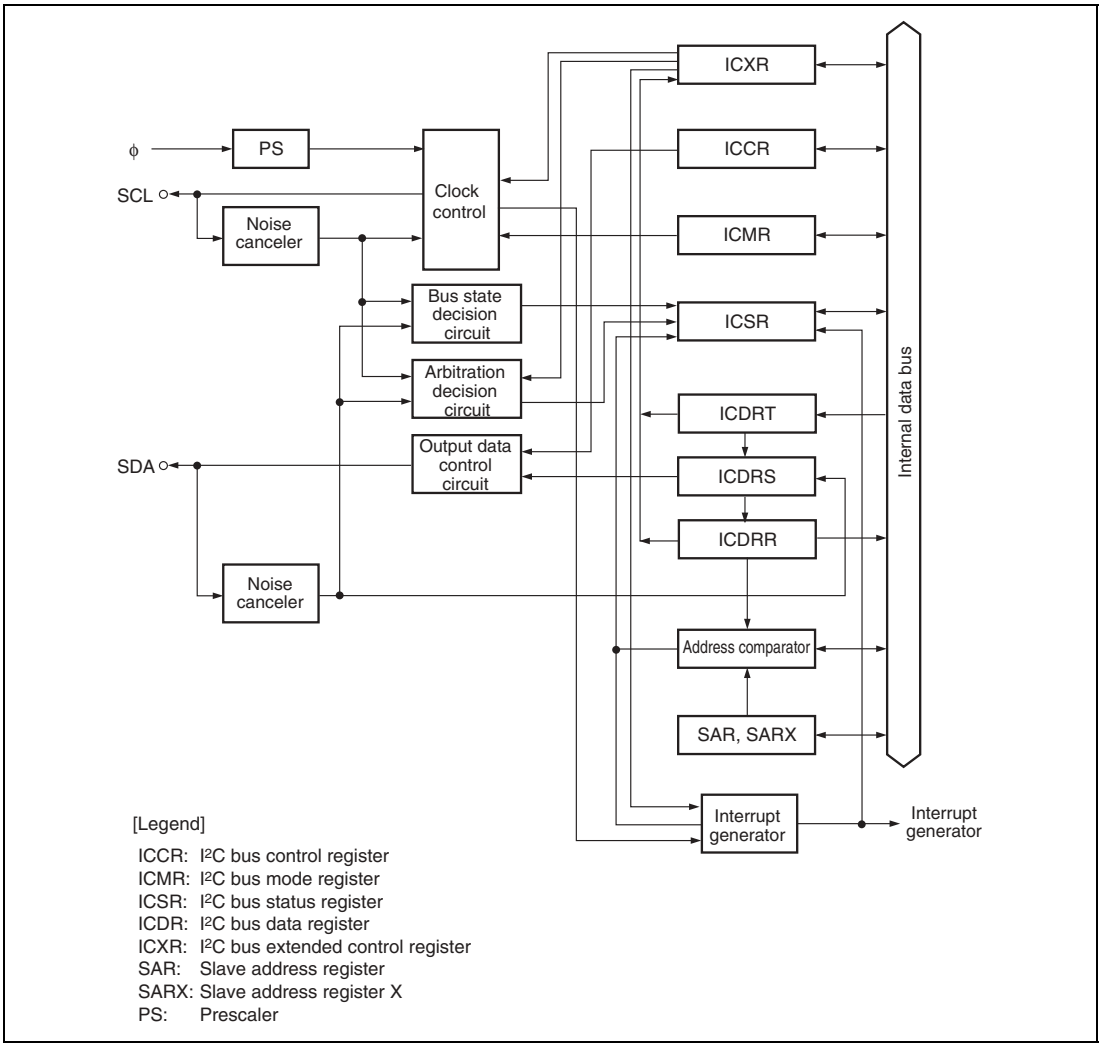

Figure 15.1 Block Diagram of I²C Bus Interface

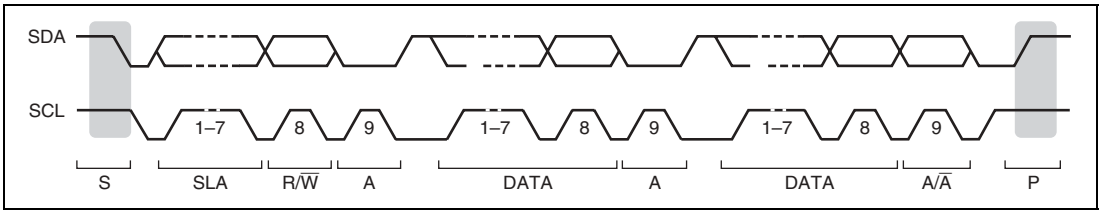

Figure 15.5 I²C Bus Timing

Table 15.8 I²C Bus Data Format Symbols

Symbol	Description
S	Start condition. The master device drives SDA from high to low while SCL is high
SLA	Slave address. The master device selects the slave device.
R/$\overline{W}$	Indicates the direction of data transfer: from the slave device to the master device when R/$\overline{W}$ is 1, or from the master device to the slave device when R/W is 0
A	Acknowledge. The receiving device drives SDA low to acknowledge a transfer. (The slave device returns acknowledge in master transmit mode, and the master device returns acknowledge in master receive mode.)
DATA	Transferred data. The bit length of transferred data is set with the BC2 to BC0 bits in ICMR. The MSB first or LSB first is switched with the MLS bit in ICMR.
P	Stop condition. The master device drives SDA from low to high while SCL is high

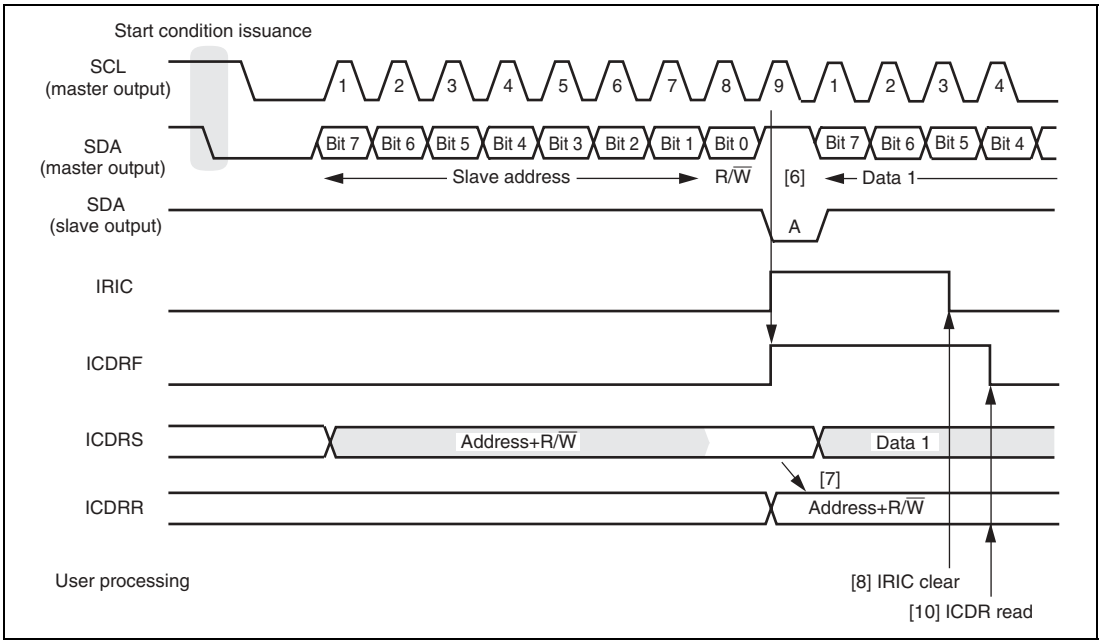

Figure 15.21 Slave Receive Mode Operation Timing Example (1)
(MLS = ACKB = 0, HNDS = 0)

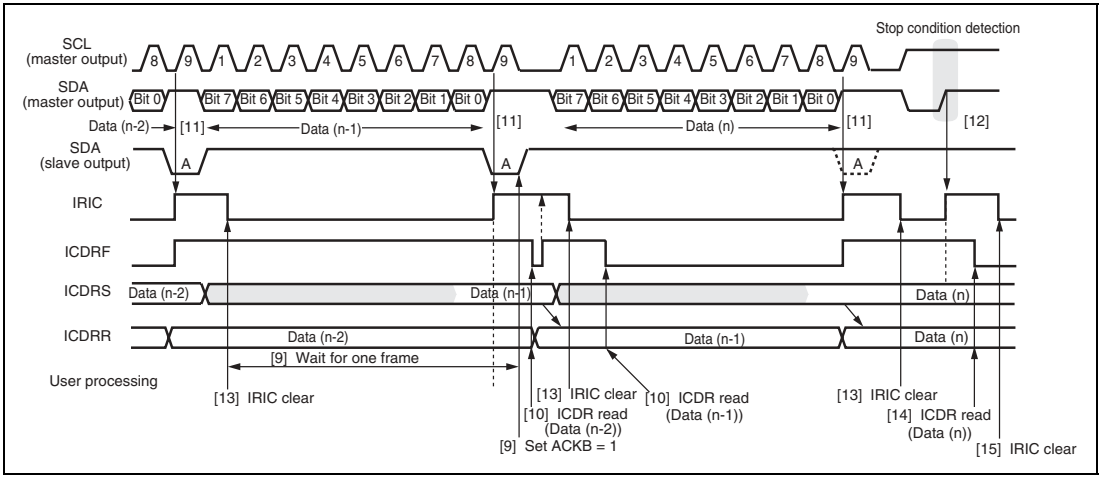

Figure 15.22 Slave Receive Mode Operation Timing Example (2)
(MLS = ACKB = 0, HNDS = 0)

Bit	Bit Name	Initial Value	R/W Slave	R/W Host	Description
2	HWRI	0	R/(W)*	—	BT Host Write Interrupt This status flag indicates that the host writes 1byte to BTDTR buffer. When the IBFIE3 bit and HWRIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: Host BTDTR write wait state [Clearing condition] After the slave reads HWRI = 1, writes 0 to this bit. 1: The host writes to BTDTR [Setting condition] The host writes one byte to BTDTR.
1	HBTWI	0	R/(W)*	—	BTDTR Host Write Start Interrupt This status flag indicates that the host writes the first byte of valid data to BTDTR buffer. When the IBFIE3 bit and HBTWIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: BTDTR host write start wait state [Clearing condition] After the slave reads HBTWI = 1 and writes 0 to this bit. 1: BTDTR host write start [Setting condition] The host starts writing valid data to BTDTR.
0	HBTRI	0	R/(W)*	—	BTDTR Host Read End Interrupt This status flag indicates that the host reads all valid data from BTDTR buffer. When the BFIE3 bit and HBTRIE bit are set to 1, IBFI3 interrupt is requested to the slave. 0: BTDTR host read end wait state [Clearing condition] After the slave reads HBTRI = 1 and writes 0 to this bit. 1: BTDTR host read end [Setting condition] When the host finished reading the valid data from BTDTR.

Note: * Only 0 can be written to clear the flag.

16.4.4 BT Mode Transfer Flow

Figure 16.6 shows the write transfer flow and figure 16.7 shows the read transfer flow in BT mode.

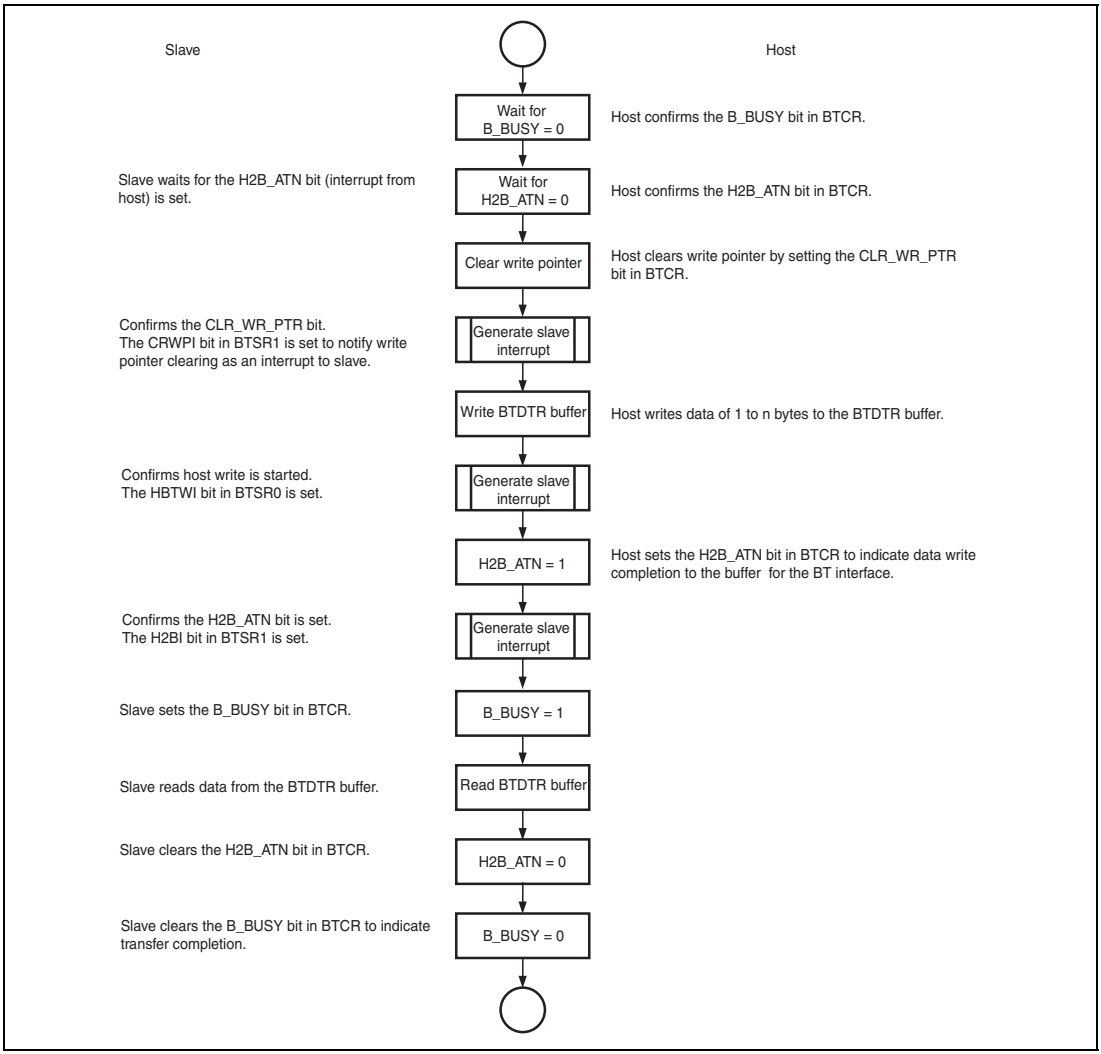

Figure 16.6 BT Write Transfer Flow

17.1 Features

- 8-bit resolution
- Two output channels
- Conversion time: Max. 10 µs (when load capacitance is 20 pF)
- Output voltage: 0 V to AVref
- D/A output retaining function in software standby mode

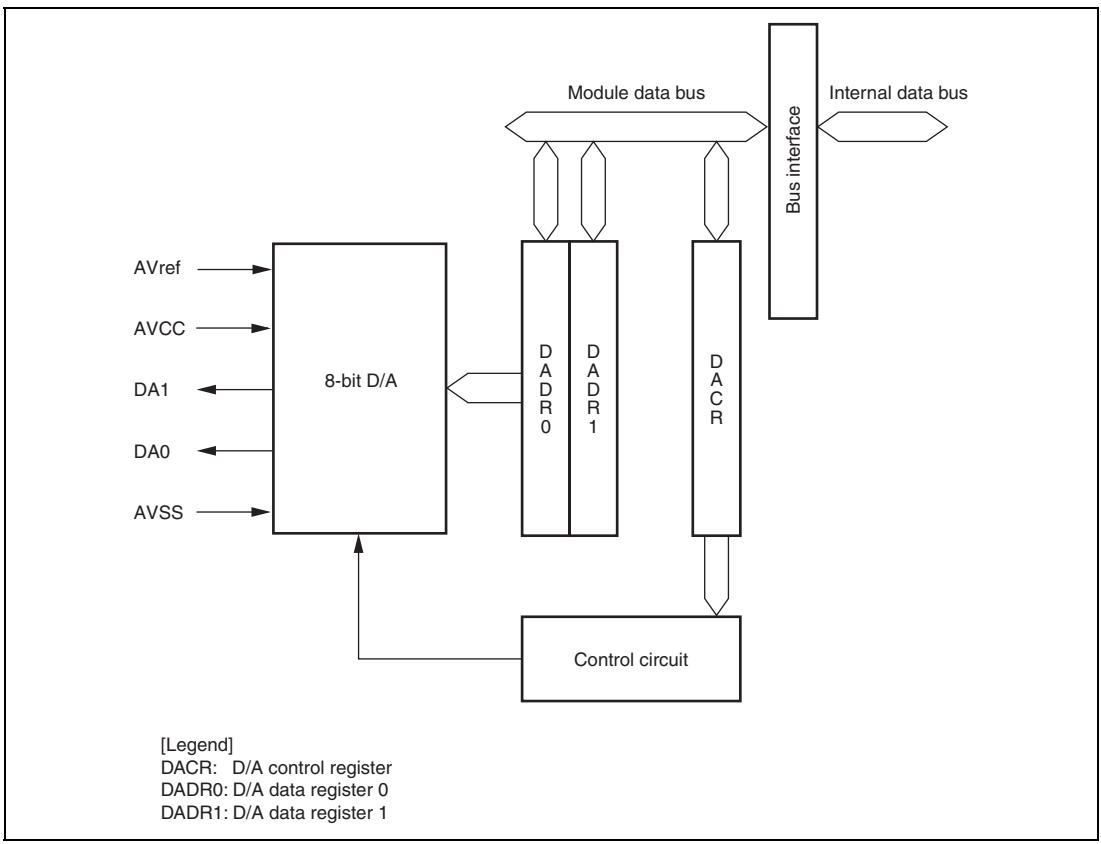

Figure 17.1 Block Diagram of D/A Converter

- Flash MAT Select Register (FMATS)

FMATS specifies whether user MAT or user boot MAT is selected.

Bit	Bit Name	Initial Value	R/W	Description
7	MS7	0/1*	R/W	MAT Select
6	MS6	0	R/W	These bits are in user-MAT selection state when the value other than H'AA is written and in user-boot-MAT selection state when H'AA is written.
5	MS5	0/1*	R/W	
4	MS4	0	R/W	
3	MS3	0/1*	R/W	The MAT is switched by writing the value in FMATS.
2	MS2	0	R/W	
1	MS1	0/1*	R/W	When the MAT is switched, follow section 20.6, Switching between User MAT and User Boot MAT. (The user boot MAT cannot be programmed in user program mode if user boot MAT is selected by FMATS. The user boot MAT must be programmed in boot mode or in programmer mode.)
0	MS0	0	R/W	H'AA: The user boot MAT is selected (in user-MAT selection state when the value of these bits are other than H'AA) Initial value when these bits are initiated in user boot mode. H'00: Initial value when these bits are initiated in a mode except for user boot mode (in user-MAT selection state) [Programmable condition] These bits are in the execution state in the on-chip RAM.

Note: * Set to 1 when in user boot mode, otherwise set to 0.

21.4 Operation

21.4.1 TAP Controller State Transitions

Figure 21.2 shows the internal states of the TAP controller. State transitions basically conform to the IEEE1149.1 standard.

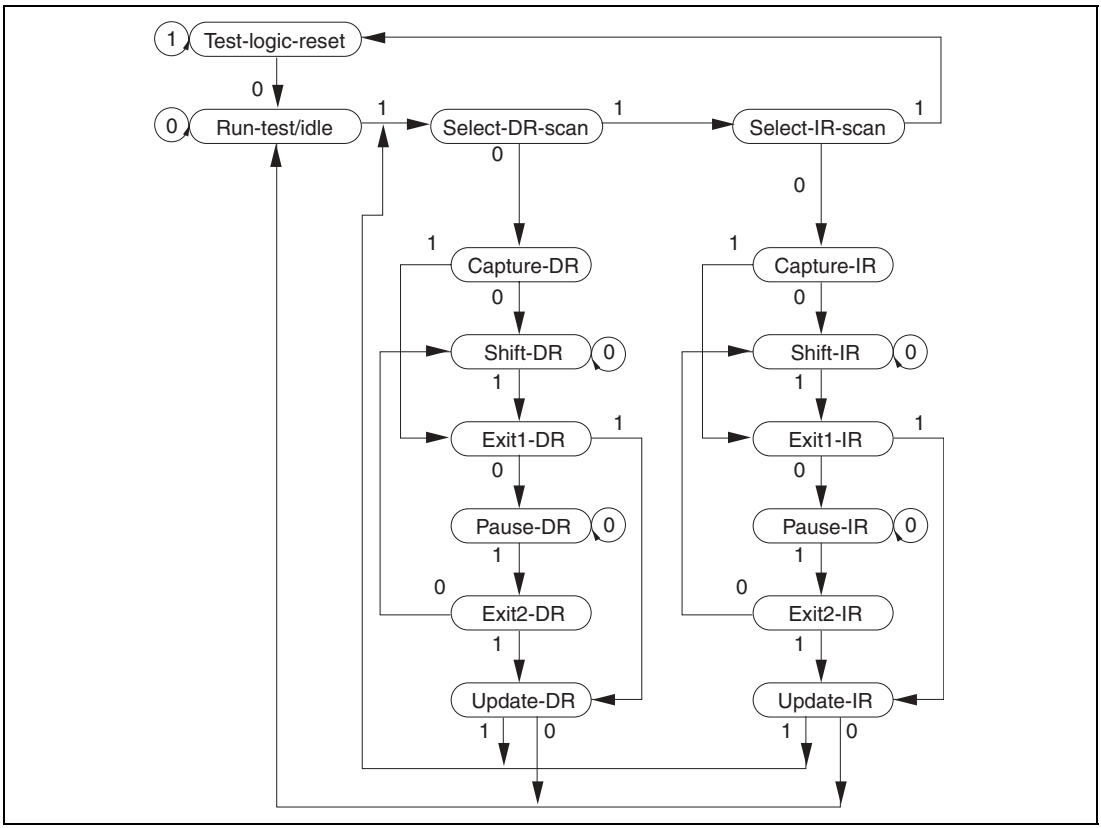

Figure 21.2 TAP Controller State Transitions

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
BCR2	—	—	ABWCP	ASTCP	ADFULLE	EXCKS	—	CPCSE	BSC
WSCR2	WMS10	WC11	WC10	WMS21	WMS20	WC22	WC21	WC20	
PCSR	PWCKX1B	PWCKX1A	PWCKX0B	PWCKX0A	PWCKX1C	PWCKB	PWCKA	PWCKX0C	PWM
SYSCR2	—	—	P6PUE	—	ADMXE	—	—	—	SYSTEM
SBYCR	SSBY	STS2	STS1	STS0	DTSPEED	SCK2	SCK1	SCK0	
LPWRCR	DTON	LSON	NESEL	EXCLE	—	PNCCS	PNCAH	—	
MSTPCRH	MSTP15	MSTP14	MSTP13	MSTP12	MSTP11	MSTP10	MSTP9	MSTP8	
MSTPCRL	MSTP7	MSTP6	MSTP5	MSTP4	MSTP3	MSTP2	MSTP1	MSTP0	
SMR_1*3	C/$\overline{A}$ (GM)	CHR (BLK)	PE (PE)	O/$\overline{E}$ (O/$\overline{E}$)	STOP (BCP1)	MP (BCP0)	CKS1 (CKS1)	CKS0 (CKS0)	SCI_1
ICCR_1	ICE	IEIC	MST	TRS	ACKE	BBSY	IRIC	SCP	IIC_1
BRR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	SCI_1
ICSR_1	ESTP	STOP	IRTR	AASX	AL	AAS	ADZ	ACKB	IIC_1
SCR_1	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	SCI_1
TDR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SSR_1*3	TDRE (TDRE)	RDRF (RDRF)	ORER (ORER)	FER (ERS)	PER (PER)	TEND (TEND)	MPB (MPB)	MPBT (MPBT)	
RDR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
SCMR_1	—	—	—	—	SDIR	SINV	—	SMIF	
ICDR_1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	IIC_1
SARX_1	SVAX6	SVAX5	SVAX4	SVAX3	SVAX2	SVAX1	SVAX0	FSX	
ICMR_1	MLS	WAIT	CKS2	CKS1	CKS0	BC2	BC1	BC0	
SAR_1	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
TIER	ICIAE	ICIBE	ICICE	ICIDE	OCIAE	OCIBE	OVIE	—	FRT
TCSR	ICFA	ICFB	ICFC	ICFD	OCFA	OCFB	OVF	CCLRA	
FRC	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRA	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
OCRB	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
TCR	IEDGA	IEDGB	IEDGC	IEDGD	BUFEA	BUFEB	CKS1	CKS0	
TOCR	ICRDMS	OCRAMS	ICRS	OCRS	OEA	OEB	OLVLA	OLVLB	

Register Abbreviation	Reset	High-Speed/ Medium-Speed	Watch	Sleep	Sub-Active	Sub-Sleep	Module Stop	Software Standby	Hardware Standby	Module
ICRA	Initialized	—	—	—	—	—	—	—	Initialized	INT
ICRB	Initialized	—	—	—	—	—	—	—	Initialized	
ICRC	Initialized	—	—	—	—	—	—	—	Initialized	
ISR	Initialized	—	—	—	—	—	—	—	Initialized	
ISCRH	Initialized	—	—	—	—	—	—	—	Initialized	
ISCRL	Initialized	—	—	—	—	—	—	—	Initialized	
DTCERA	Initialized	—	—	—	—	—	—	—	Initialized	DTC
DTCERB	Initialized	—	—	—	—	—	—	—	Initialized	
DTCERC	Initialized	—	—	—	—	—	—	—	Initialized	
DTCERD	Initialized	—	—	—	—	—	—	—	Initialized	
DTCERE	Initialized	—	—	—	—	—	—	—	Initialized	
DTVECR	Initialized	—	—	—	—	—	—	—	Initialized	
ABRKCR	Initialized	—	—	—	—	—	—	—	Initialized	INT
BARA	Initialized	—	—	—	—	—	—	—	Initialized	
BARB	Initialized	—	—	—	—	—	—	—	Initialized	
BARC	Initialized	—	—	—	—	—	—	—	Initialized	
IER16	Initialized	—	—	—	—	—	—	—	Initialized	
ISR16	Initialized	—	—	—	—	—	—	—	Initialized	
ISCR16H	Initialized	—	—	—	—	—	—	—	Initialized	
ISCR16L	Initialized	—	—	—	—	—	—	—	Initialized	
ISSR16	Initialized	—	—	—	—	—	—	—	Initialized	
ISSR	Initialized	—	—	—	—	—	—	—	Initialized	
PTCNT0	Initialized	—	—	—	—	—	—	—	Initialized	PORT
BCR2	Initialized	—	—	—	—	—	—	—	Initialized	BSC
WSCR2	Initialized	—	—	—	—	—	—	—	Initialized	
PCSR	Initialized	—	Initialized	—	Initialized	Initialized	Initialized	Initialized	Initialized	PWM
SYSCR2	Initialized	—	—	—	—	—	—	—	Initialized	SYSTEM
SBYCR	Initialized	—	—	—	—	—	—	—	Initialized	
LPWRCR	Initialized	—	—	—	—	—	—	—	Initialized	
MSTPCRH	Initialized	—	—	—	—	—	—	—	Initialized	
MSTPCRL	Initialized	—	—	—	—	—	—	—	Initialized	
SMR_1	Initialized	—	—	—	—	—	—	—	Initialized	SCI_1
ICCR_1	Initialized	—	—	—	—	—	—	—	Initialized	IIC_1

25.1 Absolute Maximum Ratings

Table 25.1 lists the absolute maximum ratings.

Table 25.1 Absolute Maximum Ratings

Item	Symbol	Value	Unit
Power supply voltage*	VCC	–0.3 to +4.3	V
Input voltage (except port 7, 8, C0 to C5, D6, and D7)	V_{in}	–0.3 to VCC +0.3	
Input voltage (port 7)	V_{in}	–0.3 to AVCC +0.3	
Input voltage (port 8, C0 to C5, D6, and D7)	V_{in}	–0.3 to +7.0	
Reference power supply voltage	AVref	–0.3 to AVCC +0.3	
Analog power supply voltage	AVCC	–0.3 to +4.3	
Analog input voltage	V_{AN}	–0.3 to AVCC +0.3	
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: –40 to +85	
Operating temperature (when flash memory is programmed or erased)	T_{opr}	0 to +75	
Storage temperature	T_{stg}	–55 to +125	

Caution: Permanent damage to this LSI may result if absolute maximum ratings are exceeded.

Note: * Voltage applied to the VCC pin.
Make sure power is not applied to the VCL pin.

25.3 AC Characteristics

Figure 25.3 shows the test conditions for the AC characteristics.

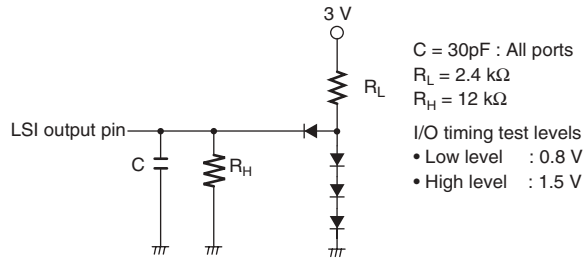

Figure 25.3 Output Load Circuit

25.3.1 Clock Timing

Table 25.4 shows the clock timing. The clock timing specified here covers clock output (ϕ) and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation stabilization times. For details of external clock input (EXTAL pin and EXCL pin) timing, see table 25.5 and 25.6.

Table 25.4 Clock Timing

Condition: VCC = 3.0 V to 3.6 V, VSS = 0 V, ϕ = 5 MHz to 33 MHz

Item	Symbol	Min.	Max.	Unit	Reference
Clock cycle time	t_{cyc}	30	200	ns	Figure 25.4
Clock high level pulse width	t_{CH}	10	—		
Clock low level pulse width	t_{CL}	10	—		
Clock rise time	t_{Cr}	—	5		
Clock fall time	t_{Cf}	—	5		
Reset oscillation stabilization (crystal)	t_{OSC1}	10	—	ms	Figure 25.5
Software standby oscillation stabilization time (crystal)	t_{OSC2}	8	—		Figure 25.6