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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	256-LFBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7309-cbz

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rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly.

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Table 3. Universal Asynchronous Receiver/Transmitters Pin Assignments

Digital Audio Interface (DAI)

The EP7309 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal® CS43L41/42/43 low-power audio DACs and the Crystal® CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Table 4. DAI Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

CODEC Interface

The EP7309 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the DAI and SSI2.

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Table 5. CODEC Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the DAI and CODEC interfaces through a multiplexer.

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Table 6. SSI2 Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

Table 11. Real-Time Clock Pin Assignments

PLL and Clocking

- Processor and Peripheral Clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Table 12. PLL and Clocking Pin Assignments

DC-to-DC converter interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Table 13. DC-to-DC Converter Interface Pin Assignments

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Pin Mnemonic	I/O	Pin Description
PA[7:0]	I/O	GPIO port A
PB[7:0]	I/O	GPIO port B
PD[0]/LEDFLSH (Note)	I/O	GPIO port D
PD[5:1]	I/O	GPIO port D
PD[7:6]/SDQM[1:0] (Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0] (Note)	I/O	GPIO port E
PE[2]/CLKSEL (Note)	I/O	GPIO port E

Table 14. General Purpose Input/Output Pin Assignments

Note: Pins are multiplexed. See Table 18 on page 10 for more information.

Hardware debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

Table 15. Hardware Debug Interface Pin Assignments

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Pin Mnemonic	I/O	Pin Description
PD[0]/LEDFLSH (Note)	O	LED flasher driver

Table 16. LED Flasher Pin Assignments

Note: Pins are multiplexed. See Table 18 on page 10 for more information.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	
COUT	Output capacitance	8	-	10.0	pF	

Timings

Timing Diagram Conventions

This data sheet contains timing diagrams. The following key explains the components used in these diagrams. Any variations are clearly labelled when they occur. Therefore, no additional meaning should be attached unless specifically stated.

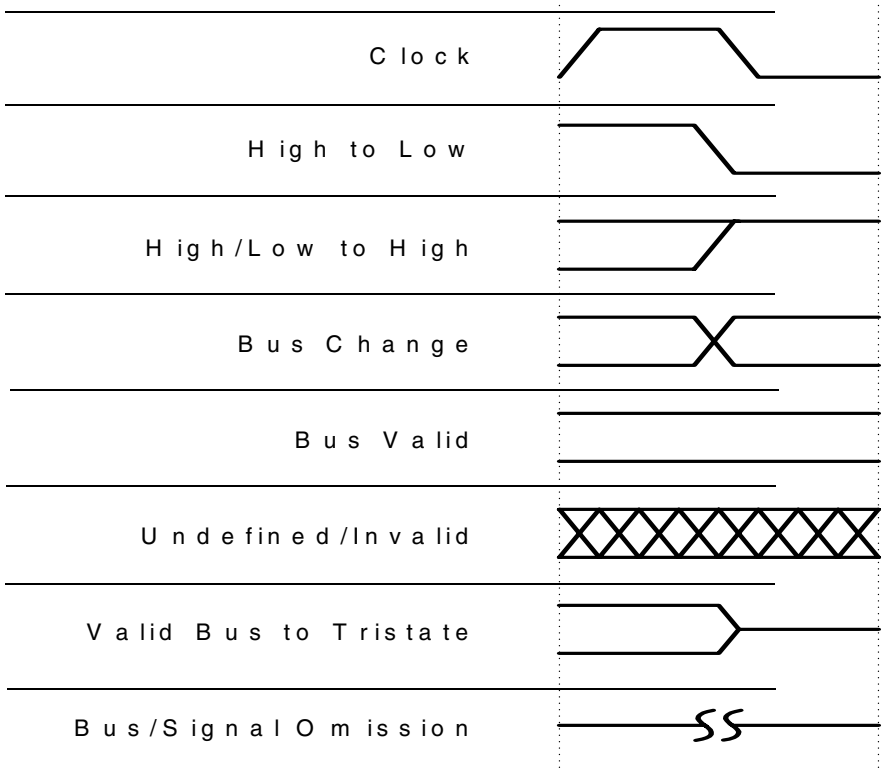


Figure 2. Legend for Timing Diagrams

Timing Conditions

Unless specified otherwise, the following conditions are true for all timing measurements. All characteristics are specified at V_{DDIO} = 3.1 - 3.5 V and V_{SS} = 0 V over an operating temperature of -40°C to +85°C. Pin loadings is 50 pF. The timing values are referenced to 1/2 V_{DD}.

Static Memory Single Read Cycle

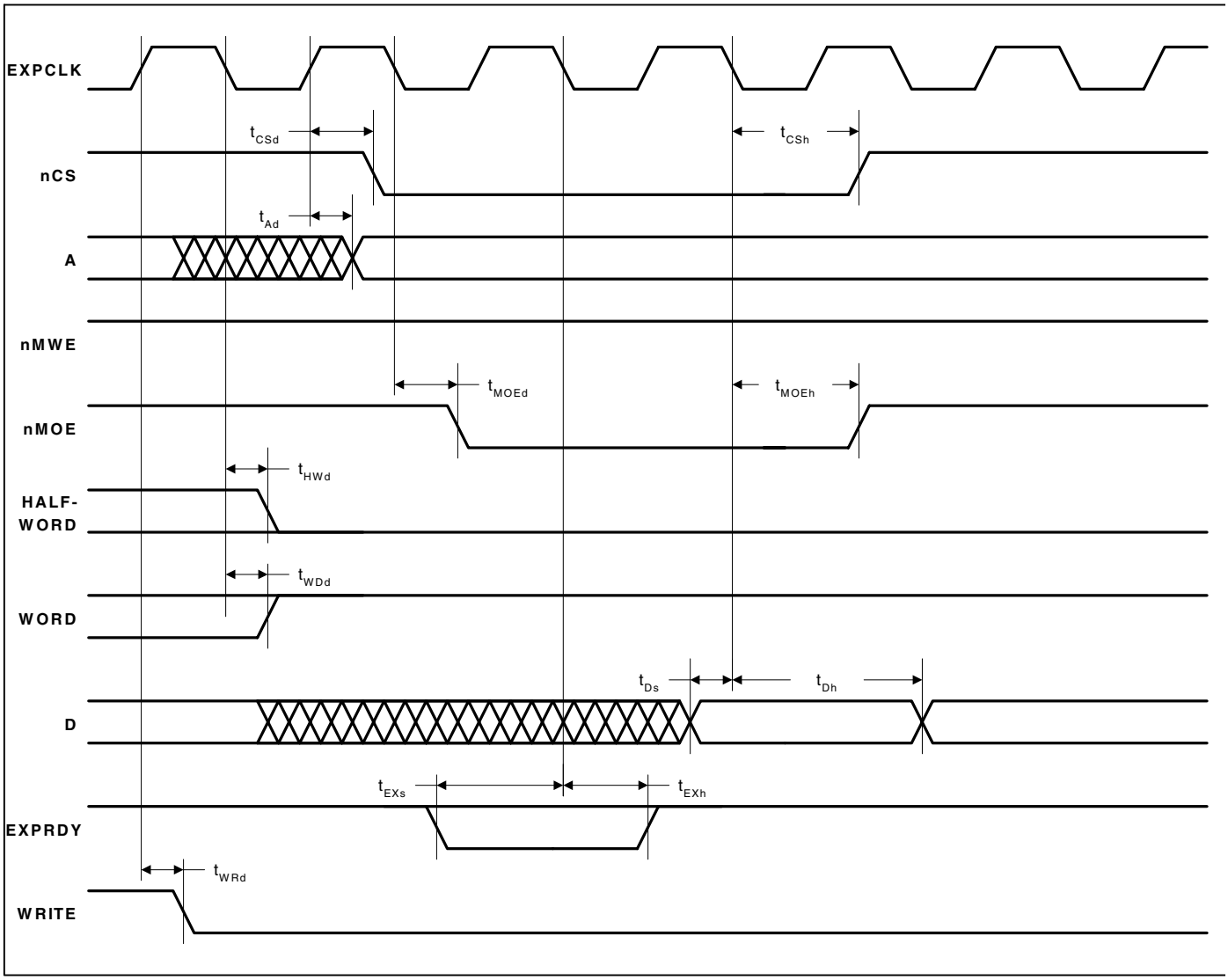


Figure 3. Static Memory Single Read Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
2. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Read Cycle

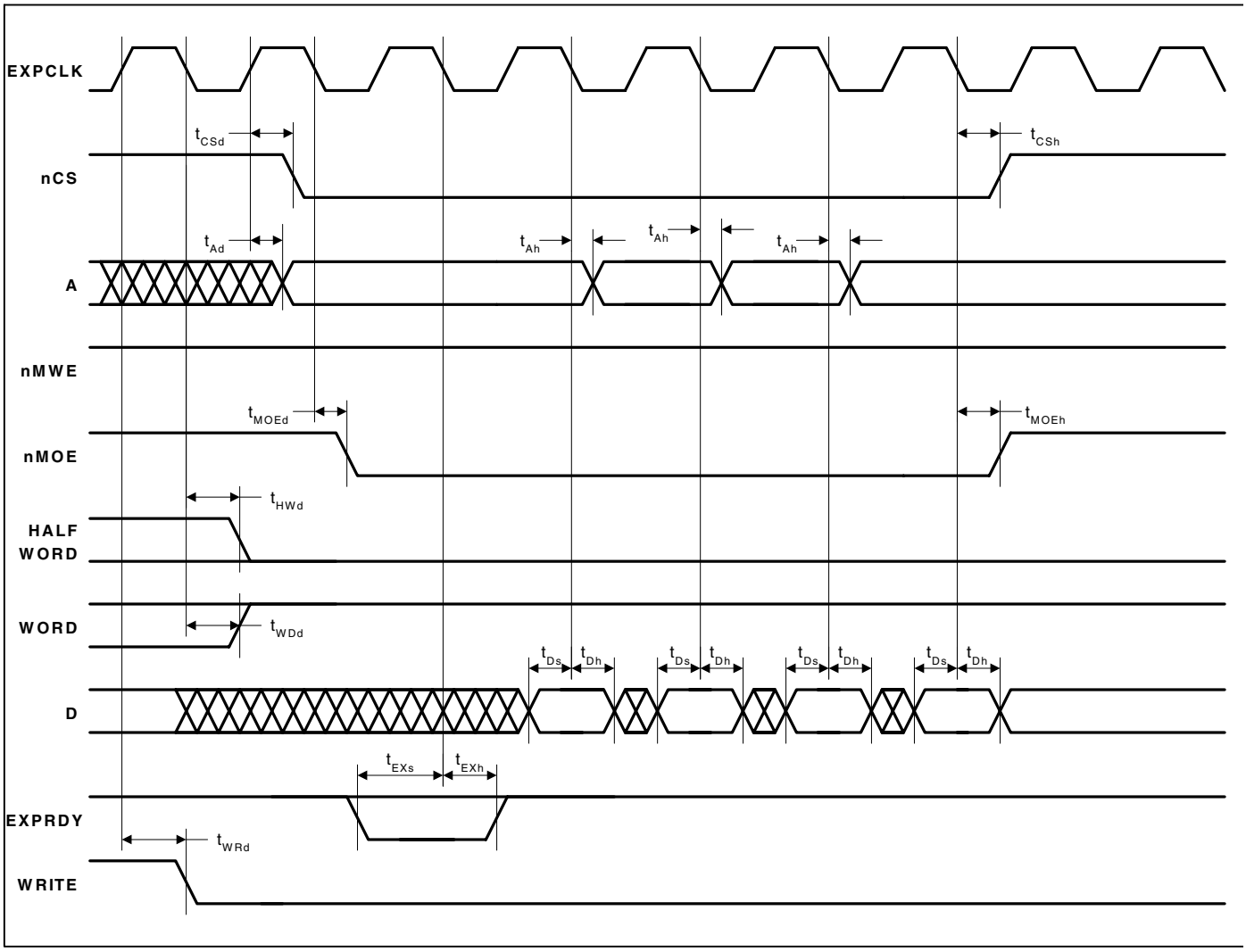


Figure 5. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

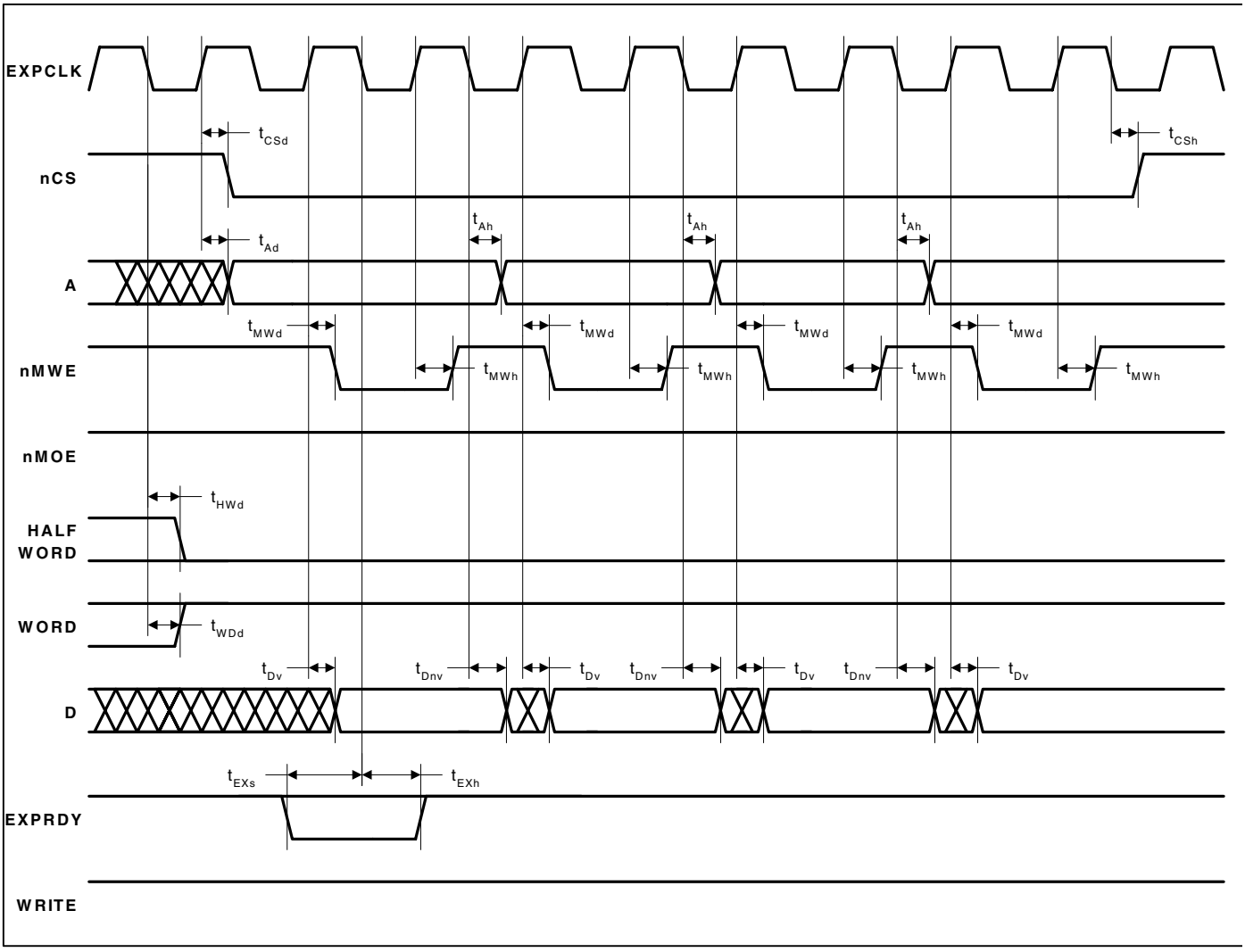


Figure 6. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI1 Interface

Parameter	Symbol	Min	Max	Unit
ADCCLK falling edge to nADCCSS deassert delay time	t_{Cd}	9	10	ms
ADCIN data setup to ADCCLK rising edge time	t_{INs}	-	15	ns
ADCIN data hold from ADCCLK rising edge time	t_{INh}	-	14	ns
ADCCLK falling edge to data valid delay time	t_{Ovd}	– 7	13	ns
ADCCLK falling edge to data invalid delay time	t_{Od}	– 2	3	ns

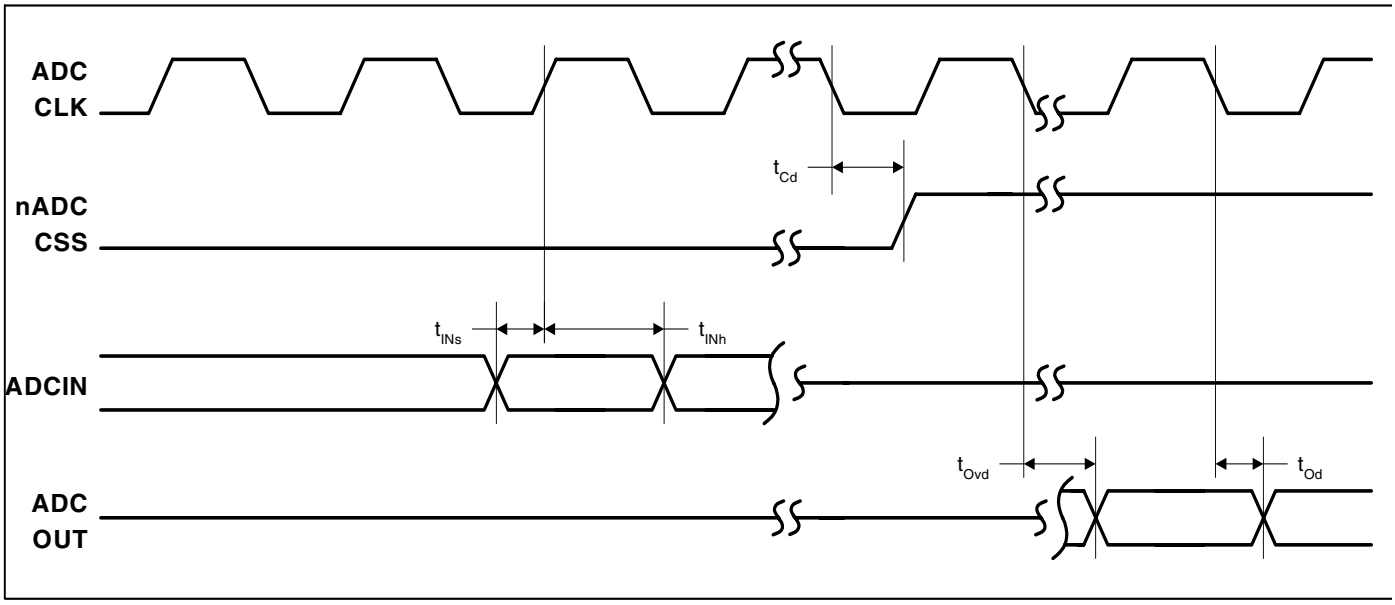


Figure 7. SSI1 Interface Timing Measurement

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
73	VSSIO	Pad Gnd		
74	VDDIO	Pad Pwr		
75	DRIVE[1]	I/O	2	High / Low
76	DRIVE[0]	I/O	2	High / Low
77	ADCCLK	O	1	Low
78	ADCOUT	O	1	Low
79	SMPCLK	O	1	Low
80	FB[1]	I		
81	VSSIO	Pad Gnd		
82	FB[0]	I		
83	COL[7]	O	1	High
84	COL[6]	O	1	High
85	COL[5]	O	1	High
86	COL[4]	O	1	High
87	COL[3]	O	1	High
88	COL[2]	O	1	High
89	VDDIO	Pad Pwr		
90	TCLK	I		
91	COL[1]	O	1	High
92	COL[0]	O	1	High
93	BUZ	O	1	Low
94	D[31]	I/O	1	Low
95	D[30]	I/O	1	Low
96	D[29]	I/O	1	Low
97	D[28]	I/O	1	Low
98	VSSIO	Pad Gnd		
99	A[27]	O	2	Low
100	D[27]	I/O	1	Low
101	A[26]	O	2	Low
102	D[26]	I/O	1	Low
103	A[25]	O	2	Low
104	D[25]	I/O	1	Low
105	HALFWORD	O	1	Low
106	A[24]	O	1	Low
107	VDDIO	Pad Pwr		—
108	VSSIO	Pad Gnd		—
109	D[24]	I/O	1	Low

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
110	A[23]	O	1	Low
111	D[23]	I/O	1	Low
112	A[22]	O	1	Low
113	D[22]	I/O	1	Low
114	A[21]	O	1	Low
115	D[21]	I/O	1	Low
116	VSSIO	Pad Gnd		
117	A[20]	O	1	Low
118	D[20]	I/O	1	Low
119	A[19]	O	1	Low
120	D[19]	I/O	1	Low
121	A[18]	O	1	Low
122	D[18]	I/O	1	Low
123	VDDIO	Pad Pwr		
124	VSSIO	Pad Gnd		
125	nTRST	I		
126	A[17]	O	1	Low
127	D[17]	I/O	1	Low
128	A[16]	O	1	Low
129	D[16]	I/O	1	Low
130	A[15]	O	1	Low
131	D[15]	I/O	1	Low
132	A[14]	O	1	Low
133	D[14]	I/O	1	Low
134	A[13]	O	1	Low
135	D[13]	I/O	1	Low
136	A[12]	O	1	Low
137	D[12]	I/O	1	Low
138	A[11]	O	1	Low
139	VDDIO	Pad Pwr		
140	VSSIO	Pad Gnd		
141	D[11]	I/O	1	Low
142	A[10]	O	1	Low
143	D[10]	I/O	1	Low
144	A[9]	O	1	Low
145	D[9]	I/O	1	Low
146	A[8]	O	1	Low
147	D[8]	I/O	1	Low

204-Ball TFBGA Package Characteristics

204-Ball TFBGA Package Specifications

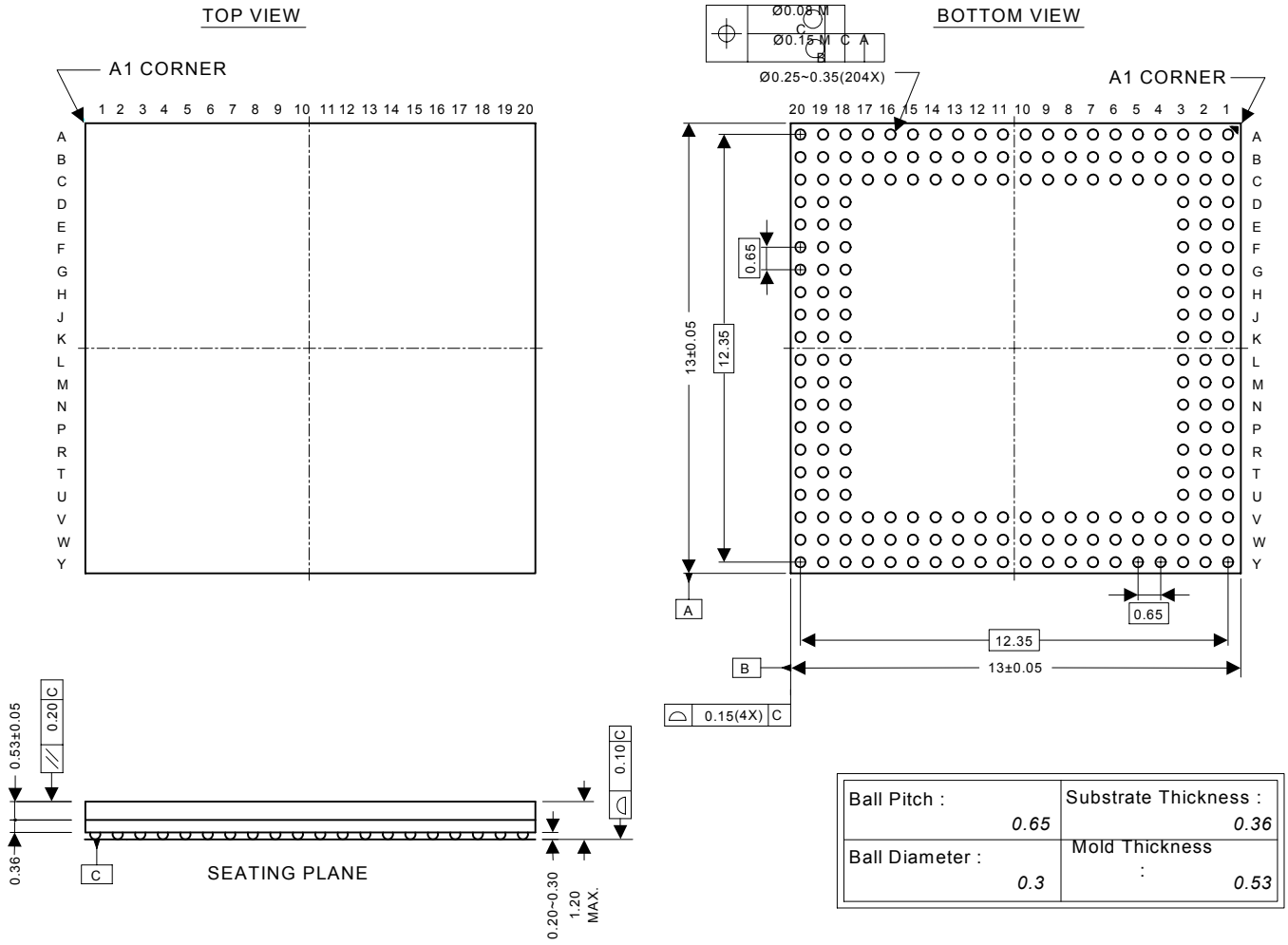


Figure 13. 204-Ball TFBGA Package

204-Ball TFBGA Pinout (Top View)

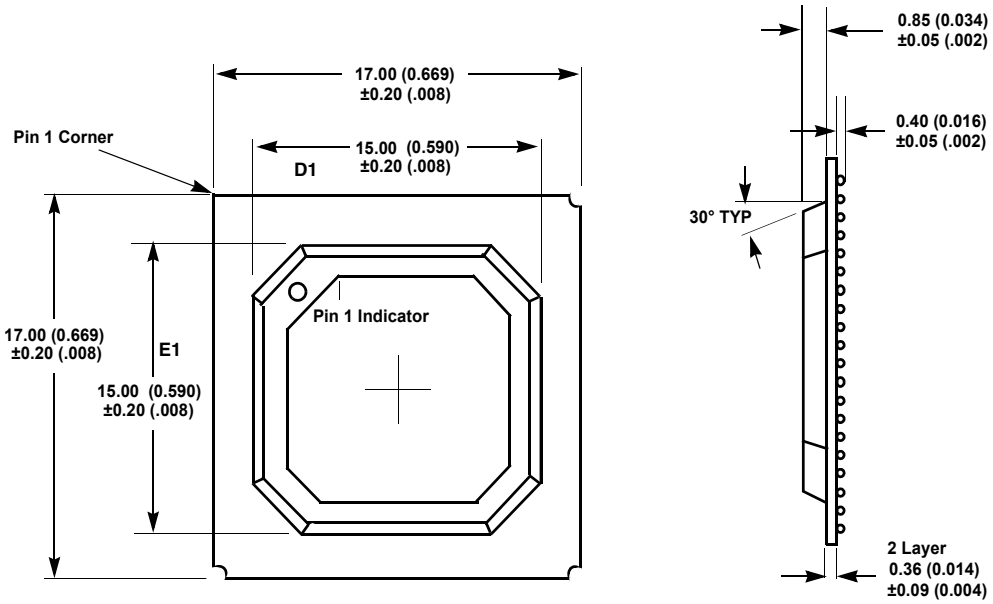
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VDDR	EXPCLK	nCS3	nCS1	nMWE	N/C	N/C	DD2	FRM	CL1	GNDD	D1	A2	D4	A5	nPWRFL	MOSCOUT	GNDR	GNDR	GNDR	A
B	WORD	VDDR	nCS5	nCS2	nMOE	N/C	N/C	DD1	M	CL2	D0	A1	D3	A4	D6	WAKEUP	MOSCIN	GNDR	GNDR	nURESET	B
C	RUN/ CLKEN	EXPRDY	VDDR	nCS4	nCS0	N/C	N/C	DD0	DD3	VDDD	A0	D2	A3	D5	A6	GNDO	VDDO	GNDR	BATOK	nPOR	C
D	PB7	RXD2	VDDR															GNDR	nBATCHG	A7	D
E	PB4	TXD2	WRITE															nMEDCHG /nBROM	nEXTPWR	D9	E
F	PB3	PB6	TDI															D7	A8	D10	F
G	PB1	PB2	PB5															D8	A9	D11	G
H	PA7	TDO	PB0															A10	D12	A12	H
J	PA4	PA5	PA6															A11	D13	A13	J
K	PA1	PA2	VDDR															D14	A14	D15	K
L	TXD1	LEDDRV	PA3															VDDR	D16	A16	L
M	RXD1	CTS	PA0															A15	A17	nTRST	M
N	DSR	nTEST1	PHDIN															D17	D19	A18	N
P	EINT3	nEINT2	DCD															D18	A20	D20	P
R	nEXTFIQ	PE2/ CLKSEL	nTEST0															A19	D22	A21	R
T	PE1/ BOOT SEL1	PE0/ BOOT SEL0	nEINT1															D21	D23	A22	T
U	GNDC	RTCOUT	RTCIN															HALF WORD	D24	A23	U
V	VDDC	GNDR	GNDR	PD7	PD4	PD2	SSICLK	SSIRXDA	nADCCS	VDDR	ADCCLK	COL7	COL4	TCLK	BUZ	D29	A26	VDDR	VDDR	A24	V
W	GNDR	GNDR	GNDR	PD6	TMS	PD1	SSITXFR	SSIRXFR	GNDD1	DRIVE1	ADCOUT	FB0	COL5	COL2	COL0	D30	A27	D26	VDDR	D25	W
Y	GNDR	GNDR	GNDR	PD5	PD3	PD0/ LED FLSH	SSITXDA	ADCIN	VDD1	DRIVE0	SMPLCK	FB1	COL6	COL3	COL1	D31	D28	D27	A25	VDDR	Y

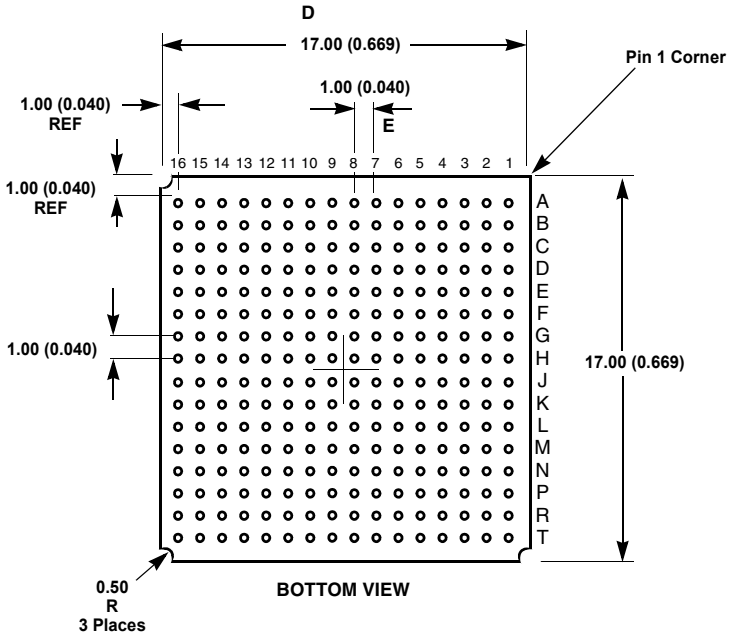
Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A

256-Ball PBGA Package Characteristics

256-Ball PBGA Package Specifications





JEDEC #: MO-151
Ball Diameter: 0.50 mm ± 0.10 mm
17 ¥ 17 ¥ 1.61 mm body

Figure 14. 256-Ball PBGA Package

Note: 1) For pin locations see Table 21.
2) Dimensions are in millimeters (inches), and controlling dimension is millimeter
3) Before beginning any new EP7309 design, contact Cirrus Logic for the latest package information.

256-Ball PBGA Pinout (Top View))

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VDDIO	nCS[4]	nCS[1]	N/C	N/C	DD[1]	M	VDDIO	D[0]	D[2]	A[3]	VDDIO	A[6]	MOSCOUT	VDDOSC	VSSIO	A
B	nCS[5]	VDDIO	nCS[3]	nMOE	VDDIO	N/C	DD[2]	CL[1]	VDDCORE	D[1]	A[2]	A[4]	A[5]	WAKEUP	VDDIO	nURESET	B
C	VDDIO	EXPCLK	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	nPOR	nEXTPWR	C
D	WRITE	EXPRDY	VSSIO	VDDIO	nCS[2]	nMWE	N/C	CL[2]	VSSRTC	D[4]	nPWRFL	MOSCIN	VDDIO	VSSIO	D[7]	D[8]	D
E	RXD[2]	PB[7]	TDI	WORD	VSSIO	nCS[0]	N/C	FRM	A[0]	D[5]	VSSOSC	VSSIO	nMEDCHG/ nBROM	VDDIO	D[9]	D[10]	E
F	PB[5]	PB[3]	VSSIO	TXD[2]	RUN/ CLKEN	VSSIO	N/C	DD[3]	A[1]	D[6]	VSSRTC	BATOK	nBATCHG	VSSIO	D[11]	VDDIO	F
G	PB[1]	VDDIO	TDO	PB[4]	PB[6]	VSSRTC	VSSRTC	DD[0]	D[3]	VSSRTC	A[7]	A[8]	A[9]	VSSIO	D[12]	D[13]	G
H	PA[7]	PA[5]	VSSIO	PA[4]	PA[6]	PB[0]	PB[2]	VSSRTC	VSSRTC	A[10]	A[11]	A[12]	A[13]	VSSIO	D[14]	D[15]	H
J	PA[3]	PA[1]	VSSIO	PA[2]	PA[0]	TXD[1]	CTS	VSSRTC	VSSRTC	A[17]	A[16]	A[15]	A[14]	nTRST	D[16]	D[17]	J
K	LEDDRV	PHDIN	VSSIO	DCD	nTEST[1]	EINT[3]	VSSRTC	ADCIN	COL[4]	TCLK	D[20]	D[19]	D[18]	VSSIO	VDDIO	VDDIO	K
L	RXD[1]	DSR	VDDIO	nEINT[1]	PE[2]/ CLKSEL	VSSRTC	PD[0]/ LEDFLSH	VSSRTC	COL[6]	D[31]	VSSRTC	A[22]	A[21]	VSSIO	A[18]	A[19]	L
M	nTEST[0]	nEINT[2]	VDDIO	PE[0]/ BOOTSEL[0]	TMS	VDDIO	SSITXFR	DRIVE[1]	FB[0]	COL[0]	D[27]	VSSIO	A[23]	VDDIO	A[20]	D[21]	M
N	nEXTFIQ	PE[1]/ BOOTSEL[1]	VSSIO	VDDIO	PD[5]	PD[2]	SSIRXDA	ADCCLK	SMPCLK	COL[2]	D[29]	D[26]	HALFWORD	VSSIO	D[22]	D[23]	N
P	VSSRTC	RTCOUT	VSSIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	VDDIO	VSSIO	VSSIO	VDDIO	VSSIO	D[24]	VDDIO	P
R	RTCIN	VDDIO	PD[4]	PD[1]	SSITXDA	nADCCS	VDDIO	ADCOUT	COL[7]	COL[3]	COL[1]	D[30]	A[27]	A[25]	VDDIO	A[24]	R
T	VDDRTC	PD[7]	PD[6]	PD[3]	SSICLK	SSIRXFR	VDDCORE	DRIVE[0]	FB[1]	COL[5]	VDDIO	BUZ	D[28]	A[26]	D[25]	VSSIO	T

256-Ball PBGA Ball Listing

The list is ordered by ball location.

Table 21. 256-Ball PBGA Ball Listing

Ball Location	Name	Type	Description
A1	VDDIO	Pad power	Digital I/O power, 3.3V
A2	nCS[4]	O	Chip select out
A3	nCS[1]	O	Chip select out
A4	N/C	O	
A5	N/C	O	
A6	DD[1]	O	LCD serial display data
A7	M	O	LCD AC bias drive
A8	VDDIO	Pad power	Digital I/O power, 3.3V
A9	D[0]	I/O	Data I/O
A10	D[2]	I/O	Data I/O
A11	A[3]	O	System byte address

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
A12	VDDIO	Pad power	Digital I/O power, 3.3V
A13	A[6]	O	System byte address
A14	MOSCOUT	O	Main oscillator out
A15	VDDOSC	Oscillator power	Oscillator power in, 2.5V
A16	VSSIO	Pad ground	I/O ground
B1	nCS[5]	O	Chip select out
B2	VDDIO	Pad power	I/O ground
B3	nCS[3]	O	Chip select out
B4	nMOE	O	ROM, expansion OP enable
B5	VDDIO	Pad power	Digital I/O power, 3.3V
B6	N/C	O	

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
P6	VSSIO	Pad ground	I/O ground
P7	VSSIO	Pad ground	I/O ground
P8	VDDIO	Pad power	Digital I/O power, 3.3V
P9	VSSIO	Pad ground	I/O ground
P10	VDDIO	Pad power	Digital I/O power, 3.3V
P11	VSSIO	Pad ground	I/O ground
P12	VSSIO	Pad ground	I/O ground
P13	VDDIO	Pad power	Digital I/O power
P14	VSSIO	Pad ground	I/O ground
P15	D[24]	I/O	Data I/O
P16	VDDIO	Pad power	Digital I/O power, 3.3V
R1	RTCIN	I/O	Real time clock oscillator input
R2	VDDIO	Pad power	Digital I/O power, 3.3V
R3	PD[4]	I/O	GPIO port D
R4	PD[1]	I/O	GPIO port D
R5	SSITXDA	O	DAI/CODEC/SSI2 serial data output
R6	nADCCS	O	SSI1 ADC chip select
R7	VDDIO	Pad power	Digital I/O power, 3.3V
R8	ADCOUT	O	SSI1 ADC serial data output
R9	COL[7]	O	Keyboard scanner column drive
R10	COL[3]	O	Keyboard scanner column drive
R11	COL[1]	O	Keyboard scanner column drive
R12	D[30]	I/O	Data I/O
R13	A[27]	O	System byte address
R14	A[25]	O	System byte address
R15	VDDIO	Pad power	Digital I/O power, 3.3V
R16	A[24]	O	System byte address
T1	VDDRTC	RTC power	Real time clock power, 2.5V
T2	PD[7]	I/O	GPIO port D
T3	PD[6]	I/O	GPIO port D
T4	PD[3]	I/O	GPIO port D
T5	SSICLK	I/O	DAI/CODEC/SSI2 serial clock
T6	SSIRXFR	–	DAI/CODEC/SSI2 frame sync
T7	VDDCORE	Core power	Core power, 2.5V
T8	DRIVE[0]	I/O	PWM drive output
T9	FB[1]	I	PWM feedback input
T10	COL[5]	O	Keyboard scanner column drive
T11	VDDIO	Pad power	Digital I/O power, 3.3V
T12	BUZ	O	Buzzer drive output
T13	D[28]	I/O	Data I/O
T14	A[26]	O	System byte address
T15	D[25]	I/O	Data I/O
T16	VSSIO	Pad ground	I/O ground

Table 22. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
201	A7	D6	nMWE	O	358
202	B7	B4	nMOE	O	360
204	C7	E6	nCS[0]	O	362
205	A6	A3	nCS[1]	O	364
206	B6	D5	nCS[2]	O	366
207	C6	B3	nCS[3]	O	368
208	A5	A2	nCS[4]	O	370

1) See EP7309 Users' Manual for pin naming / functionality.

2) For each pad, the JTAG connection ordering is input, output, then enable as applicable.

Revision History

Revision	Date	Changes
PP1	NOV 2003	First preliminary release.
F1	AUG 2005	Updated SDRAM timing. Added MSL data.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find the one nearest to you go to www.cirrus.com