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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7309-cv

FEATURES *(cont)*

- Dynamically programmable clock speeds of 18, 36, 49, and 74 MHz
- 48 KB of on-chip SRAM
- MaverickKey™ IDs
  - — 32-bit unique ID can be used for SDMI compliance
  - — 128-bit random ID
- LCD controller
  - — Interfaces directly to a single-scan panel monochrome STN LCD
  - — Interfaces to a single-scan panel color STN LCD with minimal external glue logic
- Full JTAG boundary scan and Embedded ICE® support
- Integrated Peripheral Interfaces
  - — 8/32/16-bit SRAM/FLASH/ROM Interface
  - — Digital Audio Interface providing glueless interface to low-power DACs, ADCs and CODECs
  - — Two Synchronous Serial Interfaces (SSI1, SSI2)
  - — CODEC Sound Interface
  - — 8×8 Keypad Scanner
  - — 27 General Purpose Input/Output pins
  - — Dedicated LED flasher pin from the RTC
- Internal Peripherals
  - — Two 16550 compatible UARTs
  - — IrDA Interface
  - — Two PWM Interfaces
  - — Real-time Clock
  - — Two general purpose 16-bit timers
  - — Interrupt Controller
  - — Boot ROM
- Package
  - — 208-Pin LQFP
  - — 256-Ball PBGA
  - — 204-Ball TFBGA
- The fully static EP7309 is optimized for low power dissipation and is fabricated on a 0.25 micron CMOS process

OVERVIEW *(cont.)*

The EP7309 is designed for ultra-low-power operation. Its core operates at only 2.5 V, while its I/O has an operation range of 2.5 V–3.3 V. The device has three basic power states: operating, idle and standby.

MaverickKey unique hardware programmed IDs are a solution to the growing concern over secure web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs such as those assigned for SDMI (Secure Digital Music Initiative) or any other authentication mechanism.

The EP7309 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal, CS43L41/42/43 low-power audio DACs and the Crystal, CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Simply by adding desired memory and peripherals to the highly integrated EP7309 completes a low-power system solution. All necessary interface logic is integrated on-chip.

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rates up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the RX/TX signals to/from UART 1 to enable these signals to drive an infrared communication interface directly.

Pin Mnemonic	I/O	Pin Description
TXD[1]	O	UART 1 transmit
RXD[1]	I	UART 1 receive
CTS	I	UART 1 clear to send
DCD	I	UART 1 data carrier detect
DSR	I	UART 1 data set ready
TXD[2]	O	UART 2 transmit
RXD[2]	I	UART 2 receive
LEDDRV	O	Infrared LED drive output
PHDIN	I	Photo diode input

Table 3. Universal Asynchronous Receiver/Transmitters Pin Assignments

Digital Audio Interface (DAI)

The EP7309 integrates an interface to enable a direct connection to many low cost, low power, high quality audio converters. In particular, the DAI can directly interface with the Crystal® CS43L41/42/43 low-power audio DACs and the Crystal® CS53L32 low-power ADC. Some of these devices feature digital bass and treble boost, digital volume control and compressor-limiter functions.

Pin Mnemonic	I/O	Pin Description
SCLK	O	Serial bit clock
SDOUT	O	Serial data out
SDIN	I	Serial data in
LRCK	O	Sample clock
MCLKIN	I	Master clock input
MCLKOUT	O	Master clock output

Table 4. DAI Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

CODEC Interface

The EP7309 includes an interface to telephony-type CODECs for easy integration into voice-over-IP and other voice communications systems. The CODEC interface is multiplexed to the same pins as the DAI and SSI2.

Pin Mnemonic	I/O	Pin Description
PCMCLK	O	Serial bit clock
PCMOUT	O	Serial data out
PCMIN	I	Serial data in
PCMSYNC	O	Frame sync

Table 5. CODEC Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

SSI2 Interface

An additional SPI/Microwire1-compatible interface is available for both master and slave mode communications. The SSI2 unit shares the same pins as the DAI and CODEC interfaces through a multiplexer.

- Synchronous clock speeds of up to 512 kHz
- Separate 16 entry TX and RX half-word wide FIFOs
- Half empty/full interrupts for FIFOs
- Separate RX and TX frame sync signals for asymmetric traffic

Pin Mnemonic	I/O	Pin Description
SSICLK	I/O	Serial bit clock
SSITXDA	O	Serial data out
SSIRXDA	I	Serial data in
SSITXFR	I/O	Transmit frame sync
SSIRXFR	I/O	Receive frame sync

Table 6. SSI2 Interface Pin Assignments

Note: See Table 17 on page 10 for information on pin multiplexes.

Pin Mnemonic	Pin Description
RTCIN	Real-Time Clock Oscillator Input
RTCOUT	Real-Time Clock Oscillator Output
VDDRTC	Real-Time Clock Oscillator Power
VSSRTC	Real-Time Clock Oscillator Ground

Table 11. Real-Time Clock Pin Assignments

PLL and Clocking

- Processor and Peripheral Clocks operate from a single 3.6864 MHz crystal or external 13 MHz clock
- Programmable clock speeds allow the peripheral bus to run at 18 MHz when the processor is set to 18 MHz and at 36 MHz when the processor is set to 36, 49 or 74 MHz

Pin Mnemonic	Pin Description
MOSCIN	Main Oscillator Input
MOSCOUT	Main Oscillator Output
VDDOSC	Main Oscillator Power
VSSOSC	Main Oscillator Ground

Table 12. PLL and Clocking Pin Assignments

DC-to-DC converter interface (PWM)

- Provides two 96 kHz clock outputs with programmable duty ratio (from 1-in-16 to 15-in-16) that can be used to drive a positive or negative DC to DC converter

Pin Mnemonic	I/O	Pin Description
DRIVE[1:0]	I/O	PWM drive output
FB[1:0]	I	PWM feedback input

Table 13. DC-to-DC Converter Interface Pin Assignments

Timers

- Internal (RTC) timer
- Two internal 16-bit programmable hardware count-down timers

General Purpose Input/Output (GPIO)

- Three 8-bit and one 3-bit GPIO ports
- Supports scanning keyboard matrix

Pin Mnemonic	I/O	Pin Description
PA[7:0]	I/O	GPIO port A
PB[7:0]	I/O	GPIO port B
PD[0]/LEDFLSH (Note)	I/O	GPIO port D
PD[5:1]	I/O	GPIO port D
PD[7:6]/SDQM[1:0] (Note)	I/O	GPIO port D
PE[1:0]/BOOTSEL[1:0] (Note)	I/O	GPIO port E
PE[2]/CLKSEL (Note)	I/O	GPIO port E

Table 14. General Purpose Input/Output Pin Assignments

Note: Pins are multiplexed. See Table 18 on page 10 for more information.

Hardware debug Interface

- Full JTAG boundary scan and Embedded ICE® support

Pin Mnemonic	I/O	Pin Description
TCLK	I	JTAG clock
TDI	I	JTAG data input
TDO	O	JTAG data output
nTRST	I	JTAG async reset input
TMS	I	JTAG mode select

Table 15. Hardware Debug Interface Pin Assignments

LED Flasher

A dedicated LED flasher module can be used to generate a low frequency signal on Port D pin 0 for the purpose of blinking an LED without CPU intervention. The LED flasher feature is ideal as a visual annunciator in battery powered applications, such as a voice mail indicator on a portable phone or an appointment reminder on a PDA.

- Software adjustable flash period and duty cycle
- Operates from 32 kHz RTC clock
- Will continue to flash in IDLE and STANDBY states
- 4 mA drive current

Pin Mnemonic	I/O	Pin Description
PD[0]/LEDFLSH (Note)	O	LED flasher driver

Table 16. LED Flasher Pin Assignments

Note: Pins are multiplexed. See Table 18 on page 10 for more information.

Internal Boot ROM

The internal 128 byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7309 is available in a 208-pin LQFP package, 256-ball PBGA package or a 204-ball TFBGA package.

Pin Multiplexing

The following table shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the EP7309 User's Manual for more information).

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN

Table 17. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 17. DAI/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7309.

Signal	Block	Signal	Block
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table 18. Pin Multiplexing

System Design

As shown in system block diagram, simply adding desired memory and peripherals to the highly integrated EP7309 completes a low-power system solution. All necessary interface logic is integrated on-chip.

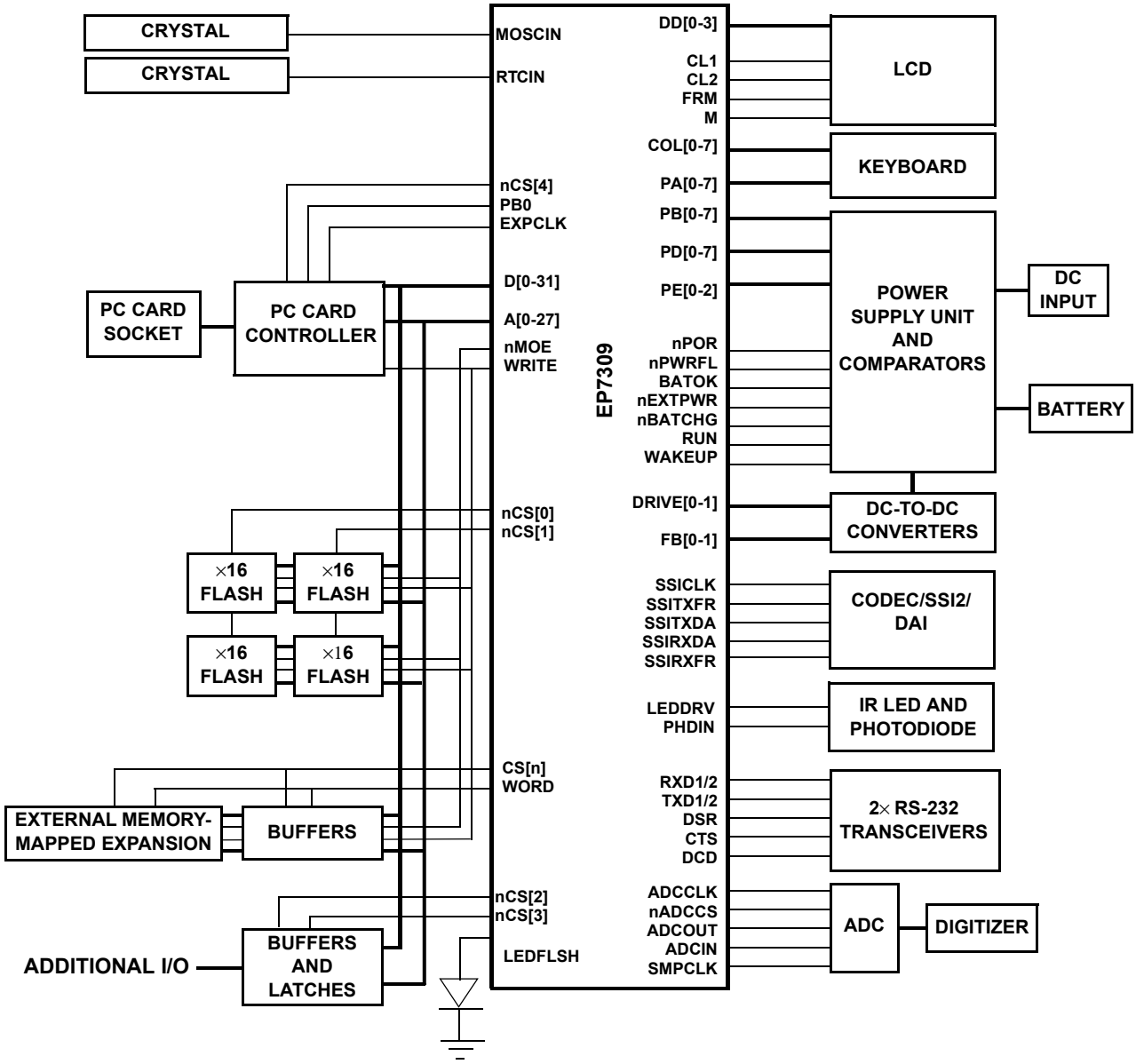

Figure 1. A Maximum EP7309 Based System

Note: A system can only use one of the following peripheral interfaces at any given time: SSI2,CODEC or DAI.

Static Memory Burst Read Cycle

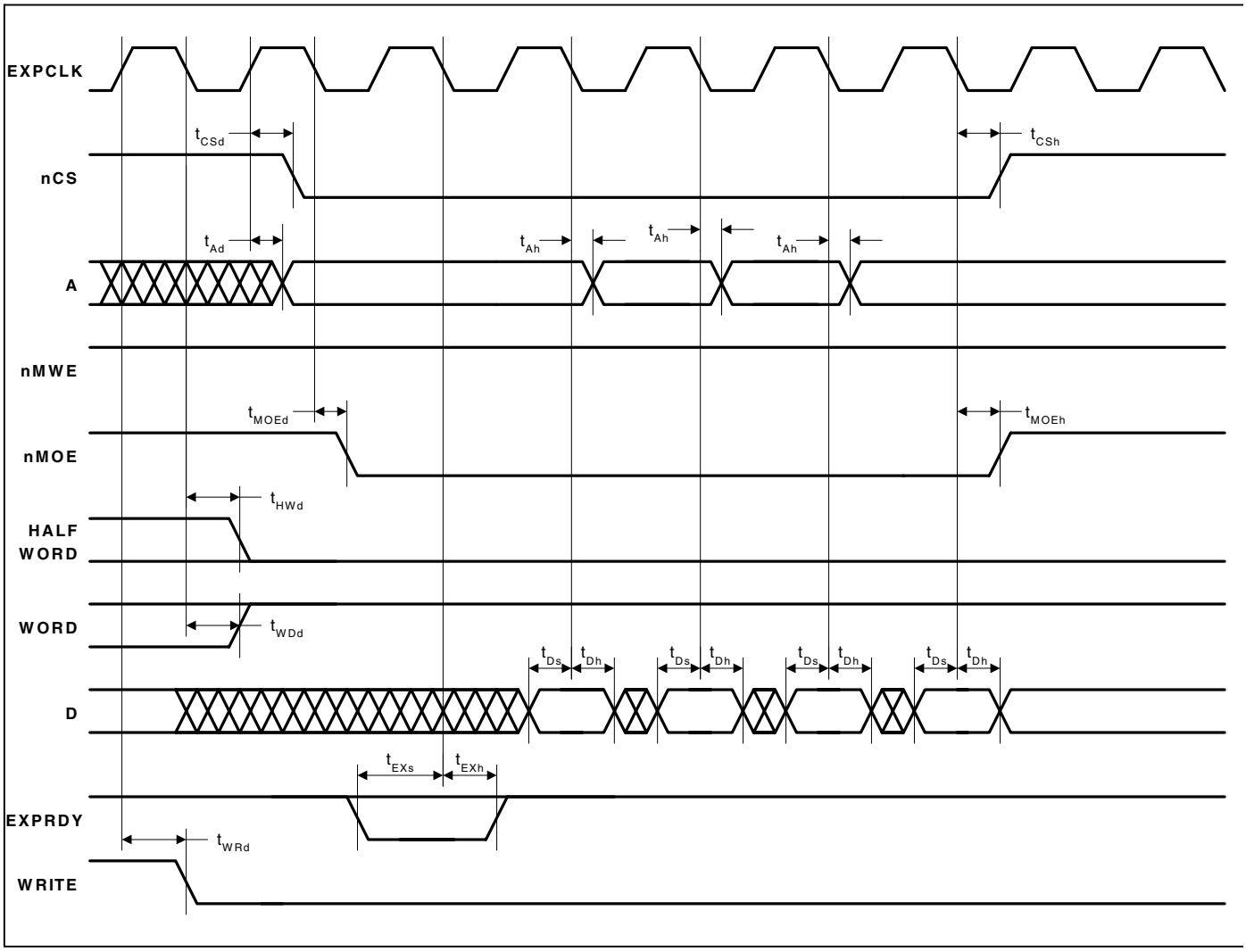

Figure 5. Static Memory Burst Read Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-0-0-0). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Consecutive reads with sequential access enabled are identical except that the sequential access wait state field is used to determine the number of wait states, and no idle cycles are inserted between successive non-sequential ROM/expansion cycles. This improves performance so the SQAEN bit should always be set where possible.
4. Address, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

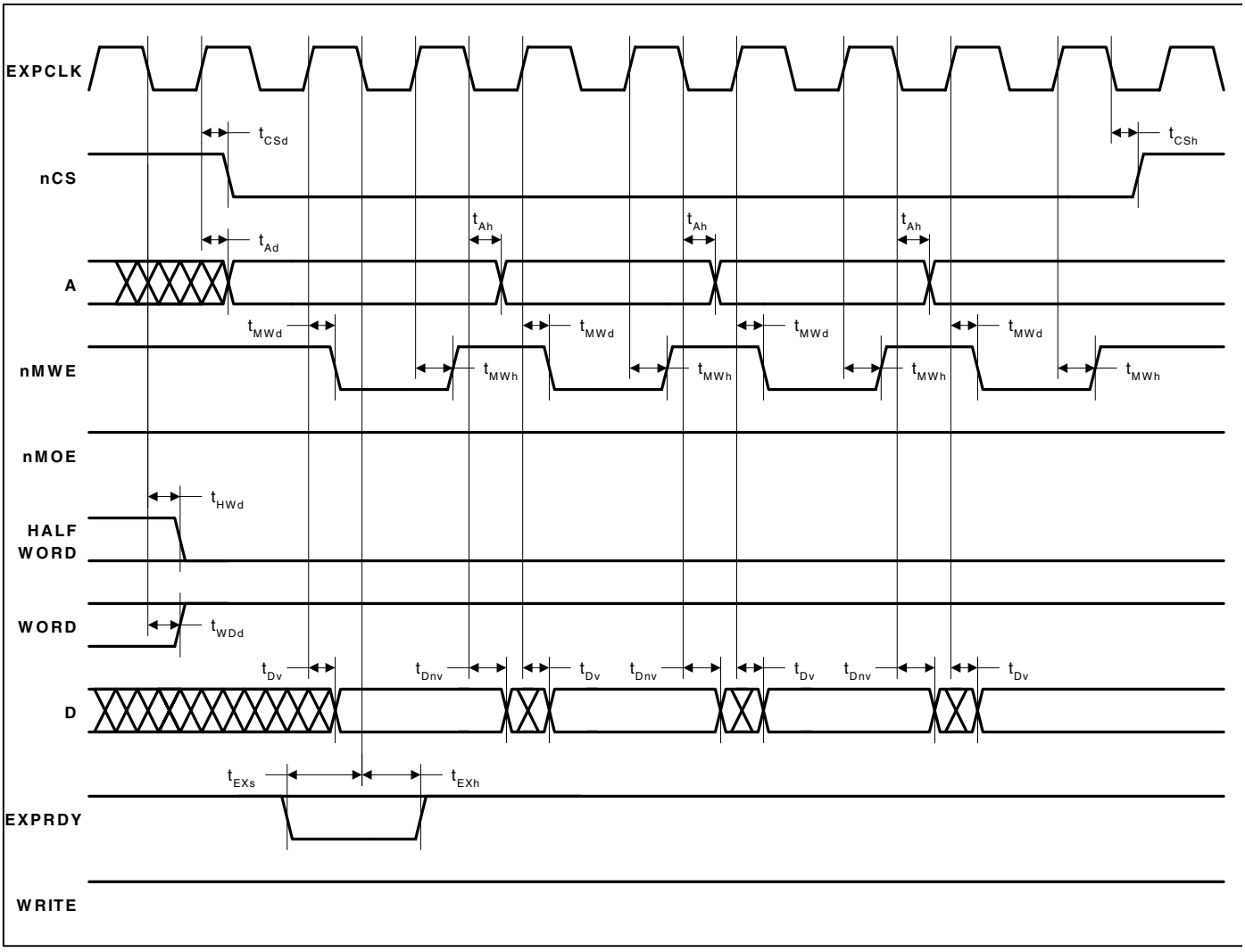

Figure 6. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

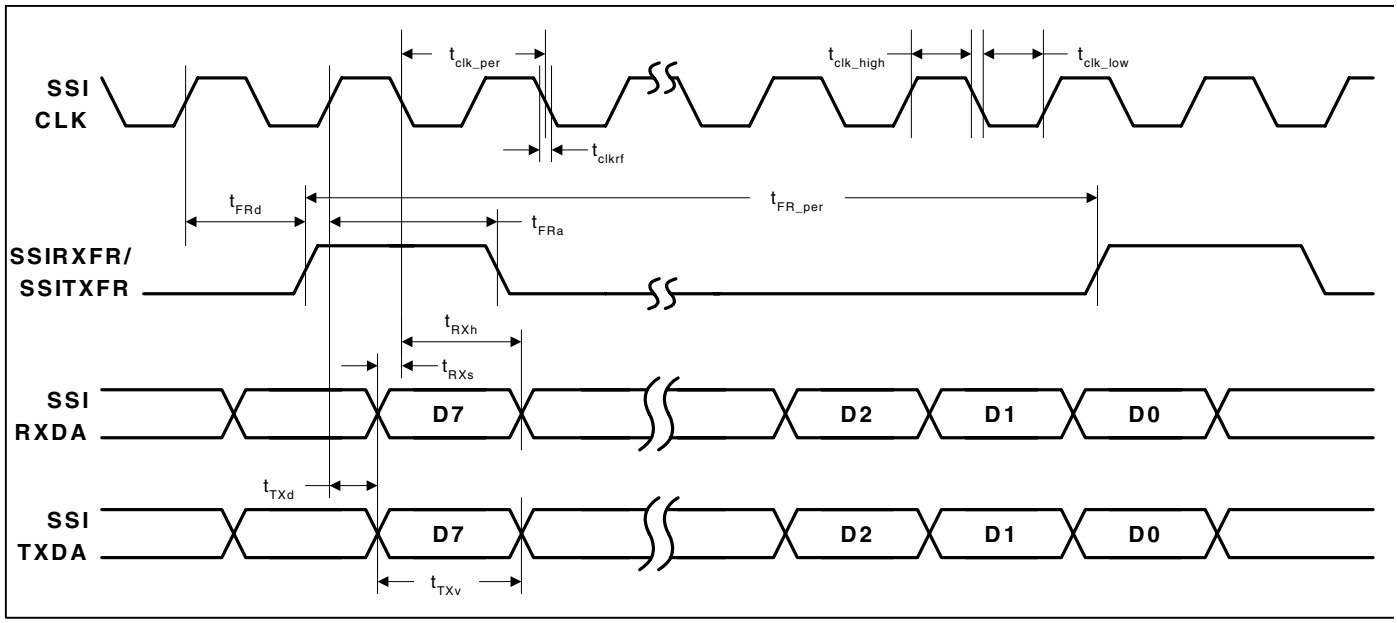

Figure 8. SSI2 Interface Timing Measurement

LCD Interface

Parameter	Symbol	Min	Max	Unit
CL[2] falling to CL[1] rising delay time	t_{CL1d}	– 10	25	ns
CL[1] falling to CL[2] rising delay time	t_{CL2d}	80	3,475	ns
CL[1] falling to FRM transition time	t_{FRMd}	300	10,425	ns
CL[1] falling to M transition time	t_{Md}	– 10	20	ns
CL[2] rising to DD (display data) transition time	t_{DDd}	– 10	20	ns

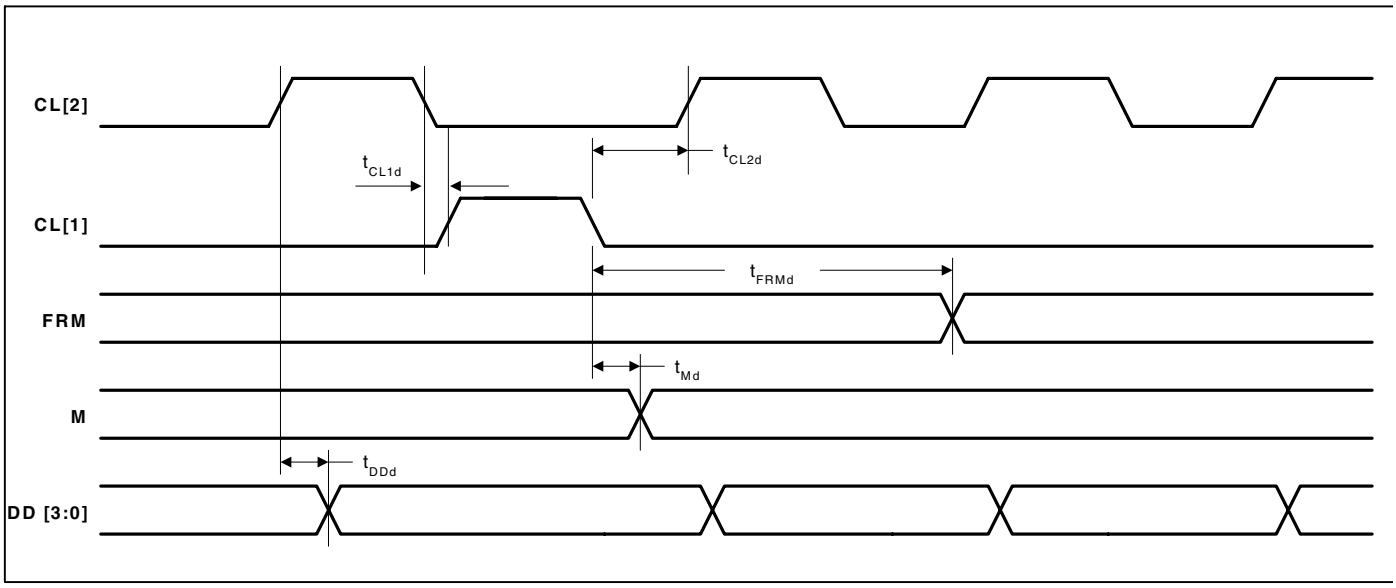

Figure 9. LCD Controller Timing Measurement

208-Pin LQFP Numeric Pin Listing

Table 19. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Type	Strength	Reset State
1	nCS[5]	O	1	High
2	VDDIO	Pad Pwr		
3	VSSIO	Pad Gnd		
4	EXPCLK	I/O	1	
5	WORD	Out	1	Low
6	WRITE	Out	1	Low
7	RUN/CLKEN	O	1	Low
8	EXPRDY	I	1	
9	TXD[2]	O	1	High
10	RXD[2]	I		
11	TDI	I	with p/u*	
12	VSSIO	Pad Gnd		
13	PB[7]	I/O	1	Input
14	PB[6]	I/O	1	Input
15	PB[5]	I/O	1	Input
16	PB[4]	I/O	1	Input
17	PB[3]	I/O	1	Input
18	PB[2]	I/O	1	Input
19	PB[1]/PRDY2	I/O	1	Input
20	PB[0]/PRDY1	I/O	1	Input
21	VDDIO	Pad Pwr		
22	TDO	O	1	Three state
23	PA[7]	I/O	1	Input
24	PA[6]	I/O	1	Input
25	PA[5]	I/O	1	Input
26	PA[4]	I/O	1	Input
27	PA[3]	I/O	1	Input
28	PA[2]	I/O	1	Input
29	PA[1]	I/O	1	Input
30	PA[0]	I/O	1	Input
31	LEDDRV	O	1	Low
32	TXD[1]	O	1	High
33	VSSIO	Pad Gnd	1	High
34	PHDIN	I		
35	CTS	I		
36	RXD[1]	I		

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
37	DCD	I		
38	DSR	I		
39	nTEST[1]	I	With p/u*	
40	nTEST[0]	I	With p/u*	
41	EINT[3]	I		
42	nEINT[2]	I		
43	nEINT[1]	I		
44	nEXTFIQ	I		
45	PE[2]/CLKSEL	I/O	1	Input
46	PE[1]/ BOOTSEL[1]	I/O	1	Input
47	PE[0]/ BOOTSEL[0]	I/O	1	Input
48	VSSRTC	RTC Gnd		
49	RTCOUT	O		
50	RTCIN	I		
51	VDDRTC	RTC power		
52	N/C			
53	PD[7]	I/O	1	Low
54	PD[6]	I/O	1	Low
55	PD[5]	I/O	1	Low
56	PD[4]	I/O	1	Low
57	VDDIO	Pad Pwr		
58	TMS	I	with p/u*	
59	PD[3]	I/O	1	Low
60	PD[2]	I/O	1	Low
61	PD[1]	I/O	1	Low
62	PD[0]/LEDFLSH	I/O	1	Low
63	SSICLK	I/O	1	Input
64	VSSIO	Pad Gnd		
65	SSITXFR	I/O	1	Low
66	SSITXDA	O	1	Low
67	SSIRXDA	I		
68	SSIRXFR	I/O		Input
69	ADCIN	I		
70	nADCCS	O	1	High
71	VSSCORE	Core Gnd		
72	VDDCORE	Core Pwr		

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
73	VSSIO	Pad Gnd		
74	VDDIO	Pad Pwr		
75	DRIVE[1]	I/O	2	High / Low
76	DRIVE[0]	I/O	2	High / Low
77	ADCCLK	O	1	Low
78	ADCOUT	O	1	Low
79	SMPCLK	O	1	Low
80	FB[1]	I		
81	VSSIO	Pad Gnd		
82	FB[0]	I		
83	COL[7]	O	1	High
84	COL[6]	O	1	High
85	COL[5]	O	1	High
86	COL[4]	O	1	High
87	COL[3]	O	1	High
88	COL[2]	O	1	High
89	VDDIO	Pad Pwr		
90	TCLK	I		
91	COL[1]	O	1	High
92	COL[0]	O	1	High
93	BUZ	O	1	Low
94	D[31]	I/O	1	Low
95	D[30]	I/O	1	Low
96	D[29]	I/O	1	Low
97	D[28]	I/O	1	Low
98	VSSIO	Pad Gnd		
99	A[27]	O	2	Low
100	D[27]	I/O	1	Low
101	A[26]	O	2	Low
102	D[26]	I/O	1	Low
103	A[25]	O	2	Low
104	D[25]	I/O	1	Low
105	HALFWORD	O	1	Low
106	A[24]	O	1	Low
107	VDDIO	Pad Pwr		—
108	VSSIO	Pad Gnd		—
109	D[24]	I/O	1	Low

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
110	A[23]	O	1	Low
111	D[23]	I/O	1	Low
112	A[22]	O	1	Low
113	D[22]	I/O	1	Low
114	A[21]	O	1	Low
115	D[21]	I/O	1	Low
116	VSSIO	Pad Gnd		
117	A[20]	O	1	Low
118	D[20]	I/O	1	Low
119	A[19]	O	1	Low
120	D[19]	I/O	1	Low
121	A[18]	O	1	Low
122	D[18]	I/O	1	Low
123	VDDIO	Pad Pwr		
124	VSSIO	Pad Gnd		
125	nTRST	I		
126	A[17]	O	1	Low
127	D[17]	I/O	1	Low
128	A[16]	O	1	Low
129	D[16]	I/O	1	Low
130	A[15]	O	1	Low
131	D[15]	I/O	1	Low
132	A[14]	O	1	Low
133	D[14]	I/O	1	Low
134	A[13]	O	1	Low
135	D[13]	I/O	1	Low
136	A[12]	O	1	Low
137	D[12]	I/O	1	Low
138	A[11]	O	1	Low
139	VDDIO	Pad Pwr		
140	VSSIO	Pad Gnd		
141	D[11]	I/O	1	Low
142	A[10]	O	1	Low
143	D[10]	I/O	1	Low
144	A[9]	O	1	Low
145	D[9]	I/O	1	Low
146	A[8]	O	1	Low
147	D[8]	I/O	1	Low

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	N/C				
C7	N/C				
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
J2	PA[5]	1	Input‡	I/O	GPIO port A
J3	PA[6]	1	Input‡	I/O	GPIO port A
J18	A[11]	1	Low	O	System byte address
J19	D[13]	1	Low	I/O	Data I/O
J20	A[13]/DRA[14]	1	Low	O	System byte address / SDRAM address
K1	PA[1]	1	Input‡	I/O	GPIO port A
K2	PA[2]	1	Input‡	I/O	GPIO port A
K3	VDDIO			Pad power	Digital I/O power, 3.3V
K18	D[14]	1	Low	I/O	Data I/O
K19	A[14]/DRA[13]	1	Low	O	System byte address / SDRAM address
K20	D[15]	1	Low	I/O	Data I/O
L1	TXD[1]	1	High	O	UART 1 transmit data out
L2	LEDDRV	1	Low	O	IR LED drive
L3	PA[3]	1	Input‡	I/O	GPIO port A
L18	VDDIO			Pad power	Digital I/O power, 3.3V
L19	D[16]	1	Low	I/O	Data I/O
L20	A[16]/DRA[11]	1	Low	O	System byte address / SDRAM address
M1	RXD[1]			I	UART 1 receive data input
M2	CTS			I	UART 1 clear to send input
M3	PA[0]	1	Input‡	I/O	GPIO port A
M18	A[15]/DRA[12]	1	Low	O	System byte address / SDRAM address
M19	A[17]/DRA[10]	1	Low	O	System byte address / SDRAM address
M20	nTRST			I	JTAG async reset input
N1	DSR			I	UART 1 data set ready input
N2	nTEST[1]	With p/u*		I	Test mode select input
N3	PHDIN			I	Photodiode input
N18	D[17]	1	Low	I/O	Data I/O
N19	D[19]	1	Low	I/O	Data I/O
N20	A[18]/DRA[9]	1	Low	O	System byte address / SDRAM address
P1	EINT[3]			I	External interrupt
P2	nEINT[2]			I	External interrupt input
P3	DCD			I	UART 1 data carrier detect
P18	D[18]	1	Low	I/O	Data I/O
P19	A[20]/DRA[7]	1	Low	O	System byte address / SDRAM address

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
P20	D[20]	1	Low	I/O	Data I/O
R1	nEXTFIQ			I	External fast interrupt input
R2	PE[2]/CLKSEL	1	Input‡	I/O	GPIO port E / clock input mode select
R3	nTEST[0]	With p/u*		I	Test mode select input
R18	A[19]/DRA[8]	1	Low	O	System byte address / SDRAM address
R19	D[22]	1	Low	I/O	Data I/O
R20	A[21]/DRA[6]	1	Low	O	System byte address / SDRAM address
T1	PE[1]/BOOTSEL[1]	1	Input‡	I/O	GPIO port E / boot mode select
T2	PE[0]/BOOTSEL[0]	1	Input‡	I/O	GPIO port E / boot mode select
T3	nEINT[1]			I	External interrupt input
T18	D[21]	1	Low	I/O	Data I/O
T19	D[23]	1	Low	I/O	Data I/O
T20	A[22]/DRA[5]	1	Low	O	System byte address / SDRAM address
U1	VSSRTC			RTC ground	Real time clock ground
U2	RTCOUT			O	Real time clock oscillator output
U3	RTCIN			I/O	Real time clock oscillator input
U18	HALFWORD	1	Low	O	Halfword access select output
U19	D[24]	1	Low	I/O	Data I/O
U20	A[23]/DRA[4]	1	Low	O	System byte address / SDRAM address
V1	VDDRTC			RTC power	Real time clock power, 2.5V
V2	VSSIO			Pad ground	I/O ground
V3	VSSIO			Pad ground	I/O ground
V4	PD[7]/SDQM[1]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
V5	PD[4]	1	Low	I/O	GPIO port D
V6	PD[2]	1	Low	I/O	GPIO port D
V7	SSICLK	1	Input‡	I/O	DAI/CODEC/SSI2 serial clock
V8	SSIRXDA			I/O	DAI/CODEC/SSI2 serial data input
V9	nADCCS	1	High	O	SSI1 ADC chip select
V10	VDDIO			Pad power	Digital I/O power, 3.3V
V11	ADCCLK	1	Low	O	SSI1 ADC serial clock
V12	COL[7]	1	High	O	Keyboard scanner column drive
V13	COL[4]	1	High	O	Keyboard scanner column drive
V14	TCLK			I	JTAG clock
V15	BUZ	1	Low	O	Buzzer drive output
V16	D[29]	1	Low	I/O	Data I/O

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
V17	A[26]/DRA[1]	2	Low	O	System byte address / SDRAM address
V18	VDDIO			Pad power	Digital I/O power, 3.3 V
V19	VDDIO			Pad power	Digital I/O power, 3.3 V
V20	A[24]/DRA[3]	‘	Low	O	System byte address / SDRAM address
W1	VSSIO			Pad ground	I/O ground
W2	VSSIO			Pad ground	I/O ground
W3	VSSIO			Pad ground	I/O ground
W4	PD[6]/SDQM[0]	1	Low	I/O	GPIO port D / SDRAM byte lane mask
W5	TMS	with p/u*		I	JTAG mode select
W6	PD[1]	1	Low	I/O	GPIO port D
W7	SSITXFR	1	Low	I/O	DAI/CODEC/SSI2 frame sync
W8	SSIRXFR	1	Input‡	I/O	DAI/CODEC/SSI2 frame sync
W9	VSSCORE			Core Ground	Core Ground
W10	DRIVE[1]	2	High / Low	I/O	PWM drive output
W11	ADCOUT	1	Low	O	SSI1 ADC serial data output
W12	FB[0]			I	PWM feedback input
W13	COL[5]	1	High	O	Keyboard scanner column drive
W14	COL[2]	1	High	O	Keyboard scanner column drive
W15	COL[0]	1	High	O	Keyboard scanner column drive
W16	D[30]	1	Low	I/O	Data I/O
W17	A[27]/DRA[0]	2	Low	O	System byte address / SDRAM address
W18	D[26]	1	Low	I/O	Data I/O
W19	VDDIO			Pad power	Digital I/O power, 3.3V
W20	D[25]	1	Low	I/O	Data I/O
Y1	VSSIO			Pad ground	I/O ground
Y2	VSSIO			Pad ground	I/O ground
Y3	VSSIO			Pad ground	I/O ground
Y4	PD[5]	1	Low	I/O	GPIO port D
Y5	PD[3]	1	Low	I/O	GPIO port D
Y6	PD[0]/LEDFLSH	1	Low	I/O	GPIO port D / LED blinker output
Y7	SSITXDA	1	Low	O	DAI/CODEC/SSI2 serial data output
Y8	ADCIN			I	SSI1 ADC serial input
Y9	VDDCORE			Core power	Digital core power, 2.5V
Y10	DRIVE[0]	2	Input‡	I/O	PWM drive output

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
H6	PB[0]/PRDY[1]	I	GPIO port B / CL-PS6700 interface signal
H7	PB[2]	I	GPIO port B
H8	VSSRTC	RTC ground	Real time clock ground
H9	VSSRTC	RTC ground	Real time clock ground
H10	A[10]	O	System byte address
H11	A[11]	O	System byte address
H12	A[12]	O	System byte address
H13	A[13]	O	System byte address
H14	VSSIO	Pad ground	I/O ground
H15	D[14]	I/O	Data I/O
H16	D[15]	I/O	Data I/O
J1	PA[3]	I	GPIO port A
J2	PA[1]	I	GPIO port A
J3	VSSIO	Pad ground	I/O ground
J4	PA[2]	I	GPIO port A
J5	PA[0]	I	GPIO port A
J6	TXD[1]	O	UART 1 transmit data out
J7	CTS	I	UART 1 clear to send input
J8	VSSRTC	RTC ground	Real time clock ground
J9	VSSRTC	RTC ground	Real time clock ground
J10	A[17]	O	System byte address
J11	A[16]	O	System byte address
J12	A[15]	O	System byte address
J13	A[14]	O	System byte address
J14	nTRST	I	JTAG async reset input
J15	D[16]	I/O	Data I/O
J16	D[17]	I/O	Data I/O
K1	LEDDRV	O	IR LED drivet
K2	PHDIN	I	Photodiode input
K3	VSSIO	Pad ground	I/O ground
K4	DCD	I	UART 1 data carrier detect
K5	nTEST[1]	I	Test mode select input
K6	EINT[3]	I	External interrupt
K7	VSSRTC	RTC ground	Real time clock ground
K8	ADCIN	I	SSI1 ADC serial input
K9	COL[4]	O	Keyboard scanner column drive
K10	TCLK	I	JTAG clock
K11	D[20]	I/O	Data I/O
K12	D[19]	I/O	Data I/O
K13	D[18]	I/O	Data I/O
K14	VSSIO	Pad ground	I/O ground
K15	VDDIO	Pad power	Digital I/O power, 3.3V
K16	VDDIO	Pad power	Digital I/O power, 3.3V
L1	RXD[1]	I	UART 1 receive data input
L2	DSR	I	UART 1 data set ready input
L3	VDDIO	Pad power	Digital I/O power, 3.3V
L4	nEINT[1]	I	External interrupt input
L5	PE[2]/CLKSEL	I	GPIO port E / clock input mode select

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
L6	VSSRTC	RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	I/O	GPIO port D / LED blinker output
L8	VSSRTC	Core ground	Real time clock ground
L9	COL[6]	O	Keyboard scanner column drive
L10	D[31]	I/O	Data I/O
L11	VSSRTC	RTC ground	Real time clock ground
L12	A[22]	O	System byte address
L13	A[21]	O	System byte address
L14	VSSIO	Pad ground	I/O ground
L15	A[18]	O	System byte address
L16	A[19]	O	System byte address
M1	nTEST[0]	I	Test mode select input
M2	nEINT[2]	I	External interrupt input
M3	VDDIO	Pad power	Digital I/O power, 3.3V
M4	PE[0]/BOOTSEL[0]	I	GPIO port E / Boot mode select
M5	TMS	I	JTAG mode select
M6	VDDIO	Pad power	Digital I/O power, 3.3V
M7	SSITXFR	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	I/O	PWM drive output
M9	FB[0]	I	PWM feedback input
M10	COL[0]	O	Keyboard scanner column drive
M11	D[27]	I/O	Data I/O
M12	VSSIO	Pad ground	I/O ground
M13	A[23]	O	System byte address
M14	VDDIO	Pad power	Digital I/O power, 3.3V
M15	A[20]	O	System byte address
M16	D[21]	I/O	Data I/O
N1	nEXTFIQ	I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	I	GPIO port E / boot mode select
N3	VSSIO	Pad ground	I/O ground
N4	VDDIO	Pad power	Digital I/O power, 3.3V
N5	PD[5]	I/O	GPIO port D
N6	PD[2]	I/O	GPIO port D
N7	SSIRXDA	I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	O	SSI1 ADC serial clock
N9	SMPCLK	O	SSI1 ADC sample clock
N10	COL[2]	O	Keyboard scanner column drive
N11	D[29]	I/O	Data I/O
N12	D[26]	I/O	Data I/O
N13	HALFWORD	O	Halfword access select output
N14	VSSIO	Pad ground	I/O ground
N15	D[22]	I/O	Data I/O
N16	D[23]	I/O	Data I/O
P1	VSSRTC	RTC ground	Real time clock ground
P2	RTCOUT	O	Real time clock oscillator output
P3	VSSIO	Pad ground	I/O ground
P4	VSSIO	Pad ground	I/O ground
P5	VDDIO	Pad power	Digital I/O power, 3.3V

Table 22. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
148	H18	G11	A[7]	O	274
150	F20	D15	D[7]	I/O	276
151	G19	F13	nBATCHG	I	279
152	E20	C16	nEXTPWR	I	280
153	F19	F12	BATOK	I	281
154	G18	C15	nPOR	I	282
155	D20	E13	nMEDCHG/nBROM	I	283
156	F18	B16	nURESET	I	284
161	D19	B14	WAKEUP	I	285
162	E19	D11	nPWRFL	I	286
163	C19	A13	A[6]	O	287
164	C20	F10	D[6]	I/O	289
165	E18	B13	A[5]	O	292
166	B20	E10	D[5]	I/O	294
169	B16	B12	A[4]	O	297
170	A16	D10	D[4]	I/O	299
171	C15	A11	A[3]	O	302
172	B15	G9	D[3]	I/O	304
173	A15	B11	A[2]	O	307
175	C14	A10	D[2]	I/O	309
176	B14	F9	A[1]	O	312
177	A14	B10	D[1]	I/O	314
178	C13	E9	A[0]	O	317
179	B13	A9	D[0]	I/O	319
184	A13	D8	CL2	O	322
185	C12	B8	CL1	O	324
186	B12	E8	FRM	O	326
187	A12	A7	M	O	328
188	C11	F8	DD[3]	I/O	330
189	B11	B7	DD[2]	I/O	333
191	B10	A6	DD[1]	I/O	336
192	A10	G8	DD[0]	I/O	339
193	A9	B6	N/C	O	342
194	B9	D7	N/C	O	344
195	C9	A5	N/C	I/O	346
196	A8	E7	N/C	I/O	349
199	B8	F7	N/C	I/O	352
200	C8	A4	N/C	I/O	355

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table 23 lists abbreviations and acronyms used in this data sheet.

Table 23. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table 23. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table 24. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt