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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM7TDMI
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	74MHz
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	-
SATA	-
USB	-
Voltage - I/O	2.5V, 2.7V, 3.0V, 3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	Hardware ID
Package / Case	208-LQFP
Supplier Device Package	208-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/cirrus-logic/ep7309-cvz

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Internal Boot ROM

The internal 128 byte Boot ROM facilitates download of saved code to the on-board SRAM/FLASH.

Packaging

The EP7309 is available in a 208-pin LQFP package, 256-ball PBGA package or a 204-ball TFBGA package.

Pin Multiplexing

The following table shows the pin multiplexing of the DAI, SSI2 and the CODEC. The selection between SSI2 and the CODEC is controlled by the state of the SERSEL bit in SYSCON2. The choice between the SSI2, CODEC, and the DAI is controlled by the DAISEL bit in SYSCON3 (see the EP7309 User's Manual for more information).

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSICLK	I/O	SCLK	SSICLK	PCMCLK
SSITXDA	O	SDOUT	SSITXDA	PCMOUT
SSIRXDA	I	SDIN	SSIRXDA	PCMIN

Table 17. DAI/SSI2/CODEC Pin Multiplexing

Pin Mnemonic	I/O	DAI	SSI2	CODEC
SSITXFR	I/O	LRCK	SSITXFR	PCMSYNC
SSIRXFR	I	MCLKIN	SSIRXFR	p/u
BUZ	O	MCLKOUT		

Table 17. DAI/SSI2/CODEC Pin Multiplexing

The following table shows the pins that have been multiplexed in the EP7309.

Signal	Block	Signal	Block
RUN	System Configuration	CLKEN	System Configuration
nMEDCHG	Interrupt Controller	nBROM	Boot ROM select
PD[0]	GPIO	LEDFLSH	LED Flasher
PE[1:0]	GPIO	BOOTSEL[1:0]	System Configuration
PE[2]	GPIO	CLKSEL	System Configuration

Table 18. Pin Multiplexing

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

DC Core, PLL, and RTC Supply Voltage	2.9 V
DC I/O Supply Voltage (Pad Ring)	3.6 V
DC Pad Input Current	±10 mA/pin; ±100 mA cumulative
Storage Temperature, No Power	–40°C to +125°C

Recommended Operating Conditions

DC core, PLL, and RTC Supply Voltage	2.5 V ± 0.2 V
DC I/O Supply Voltage (Pad Ring)	2.3 V - 3.5 V
DC Input / Output Voltage	O–I/O supply voltage
Operating Temperature	Extended -20°C to +70°C; Commercial 0°C to +70°C; Industrial -40°C to +85°C

DC Characteristics

All characteristics are specified at V_{DDCORE} = 2.5 V, V_{DDIO} = 3.3 V and V_{SS} = 0 V over an operating temperature of 0°C to +70°C for all frequencies of operation. The current consumption figures have test conditions specified per parameter."

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIH	CMOS input high voltage	$0.65 \times V_{DDIO}$	-	V_{DDIO} + 0.3	V	V_{DDIO} = 2.5 V
VIL	CMOS input low voltage	V_{SS} – 0.3	-	$0.25 \times V_{DDIO}$	V	V_{DDIO} = 2.5 V
VT+	Schmitt trigger positive going threshold	-	-	2.1	V	
VT-	Schmitt trigger negative going threshold	0.8	-	-	V	
Vhst	Schmitt trigger hysteresis	0.1	-	0.4	V	VIL to VIH
VOH	CMOS output high voltage[a] Output drive 1[a] Output drive 2[a]	V_{DD} – 0.2 2.5 2.5	- - -	- - -	V V V	IOH = 0.1 mA IOH = 4 mA IOH = 12 mA
VOL	CMOS output low voltage[a] Output drive 1[a] Output drive 2[a]	- - -	- - -	0.3 0.5 0.5	V V V	IOL = –0.1 mA IOL = –4 mA IOL = –12 mA
IIN	Input leakage current	-	-	1.0	µA	VIN = V_{DD} or GND
IOZ	Bidirectional 3-state leakage current[b c]	25	-	100	µA	VOUT = V_{DD} or GND
CIN	Input capacitance	8	-	10.0	pF	
COUT	Output capacitance	8	-	10.0	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CI/O	Transceiver capacitance	8	-	10.0	pF	
$IDD_{STANDBY}$ @ 25 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	77 41	- -	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 70 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	570 111	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$IDD_{STANDBY}$ @ 85 C	Standby current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	- -	1693 163	µA	Only nPOR, nPWRFAIL, nURESET, PE0, PE1, and RTS are driven, while all other float, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
IDD_{idle} at 74 MHz	Idle current consumption[1] Core, Osc, RTC @2.5 V I/O @ 3.3 V	- -	6 10	- -	mA	Both oscillators running, CPU static, Cache enabled, LCD disabled, VIH = V_{DD} ± 0.1 V, VIL = GND ± 0.1 V
$VDD_{STANDBY}$	Standby supply voltage	2.0	-	-	V	Minimum standby voltage for state retention, internal SRAM cache, and RTC operation only

a. Refer to the strength column in the pin assignment tables for all package types.

b. Assumes buffer has no pull-up or pull-down resistors.

c. The leakage value given assumes that the pin is configured as an input pin but is not currently being driven.

Note: 1) Total power consumption = IDD_{CORE} x 2.5 V + IDD_{IO} x 3.3 V

2) A typical design will provide 3.3 V to the I/O supply (i.e., V_{DDIO}), and 2.5 V to the remaining logic. This is to allow the I/O to be compatible with 3.3 V powered external logic (i.e., 3.3 V SDRAMs).

2) Pull-up current = 50 µA typical at V_{DD} = 3.3 V.

Static Memory

Figure 3 through Figure 6 define the timings associated with all phases of the Static Memory. The following table contains the values for the timings of each of the Static Memory modes.

Parameter	Symbol	Min	Typ	Max	Unit
EXPCLK rising edge to nCS assert delay time	t_{CSd}	2	8	20	ns
EXPCLK falling edge to nCS deassert hold time	t_{CSh}	2	7	20	ns
EXPCLK rising edge to A assert delay time	t_{Ad}	4	9	16	ns
EXPCLK falling edge to A deassert hold time	t_{Ah}	3	10	19	ns
EXPCLK rising edge to nMWE assert delay time	t_{MWd}	3	6	10	ns
EXPCLK rising edge to nMWE deassert hold time	t_{MWh}	3	6	10	ns
EXPCLK falling edge to nMOE assert delay time	t_{MOEd}	3	7	10	ns
EXPCLK falling edge to nMOE deassert hold time	t_{MOEh}	2	7	10	ns
EXPCLK falling edge to HALFWORD deassert delay time	t_{HWd}	2	8	20	ns
EXPCLK falling edge to WORD assert delay time	t_{WDd}	2	8	16	ns
EXPCLK rising edge to data valid delay time	t_{Dv}	8	13	21	ns
EXPCLK falling edge to data invalid delay time	t_{Dnv}	6	15	30	ns
Data setup to EXPCLK falling edge time	t_{Ds}	-	-	1	ns
EXPCLK falling edge to data hold time	t_{Dh}	-	-	3	ns
EXPCLK rising edge to WRITE assert delay time	t_{WRd}	5	11	23	ns
EXPREADY setup to EXPCLK falling edge time	t_{EXs}	-	-	0	ns
EXPCLK falling edge to EXPREADY hold time	t_{EXh}	-	-	0	ns

Static Memory Single Write Cycle

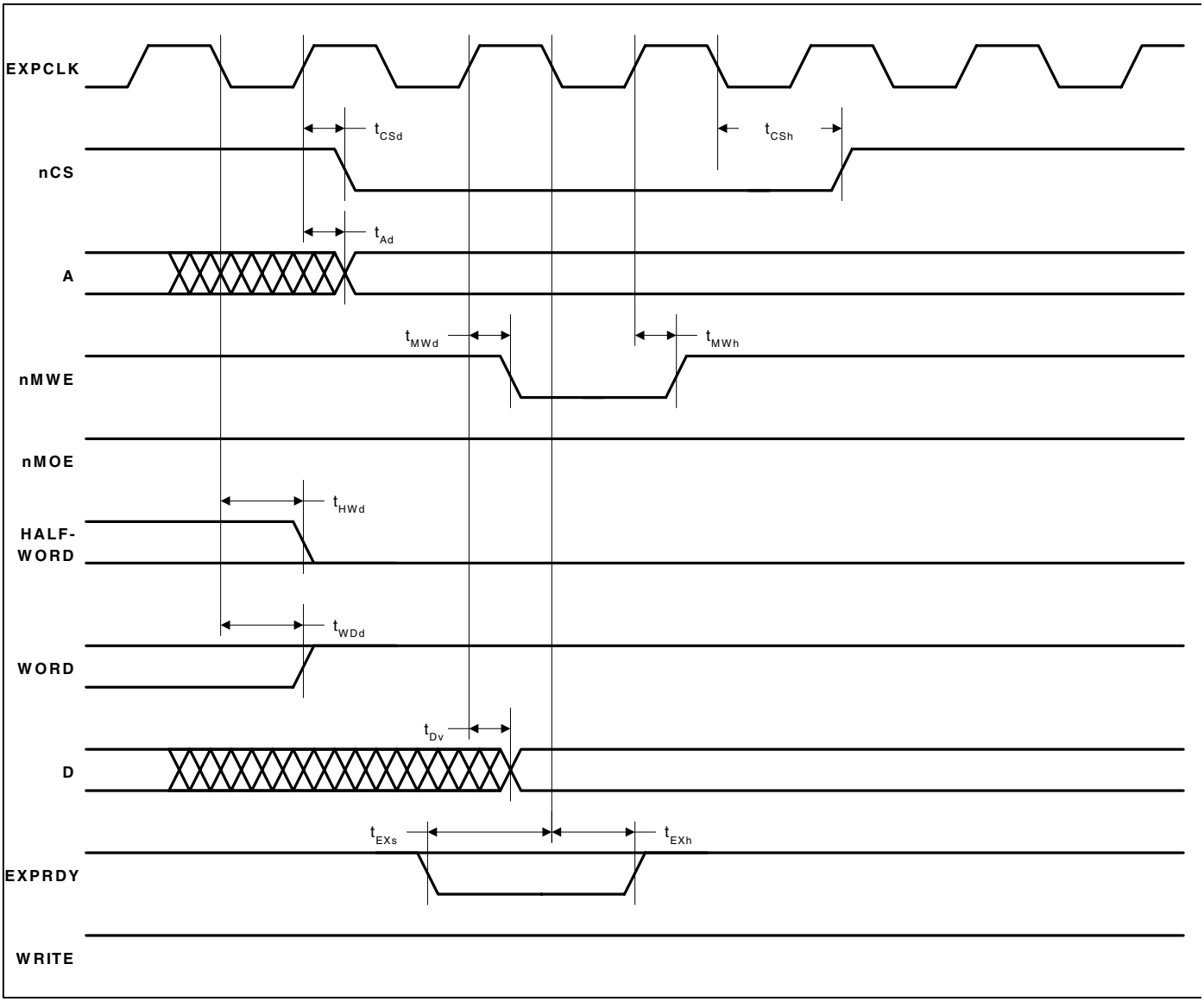

Figure 4. Static Memory Single Write Cycle Timing Measurement

Note: 1. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.

2. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.

3. Address, Data, Halfword, Word, and Write hold state until next cycle.

Static Memory Burst Write Cycle

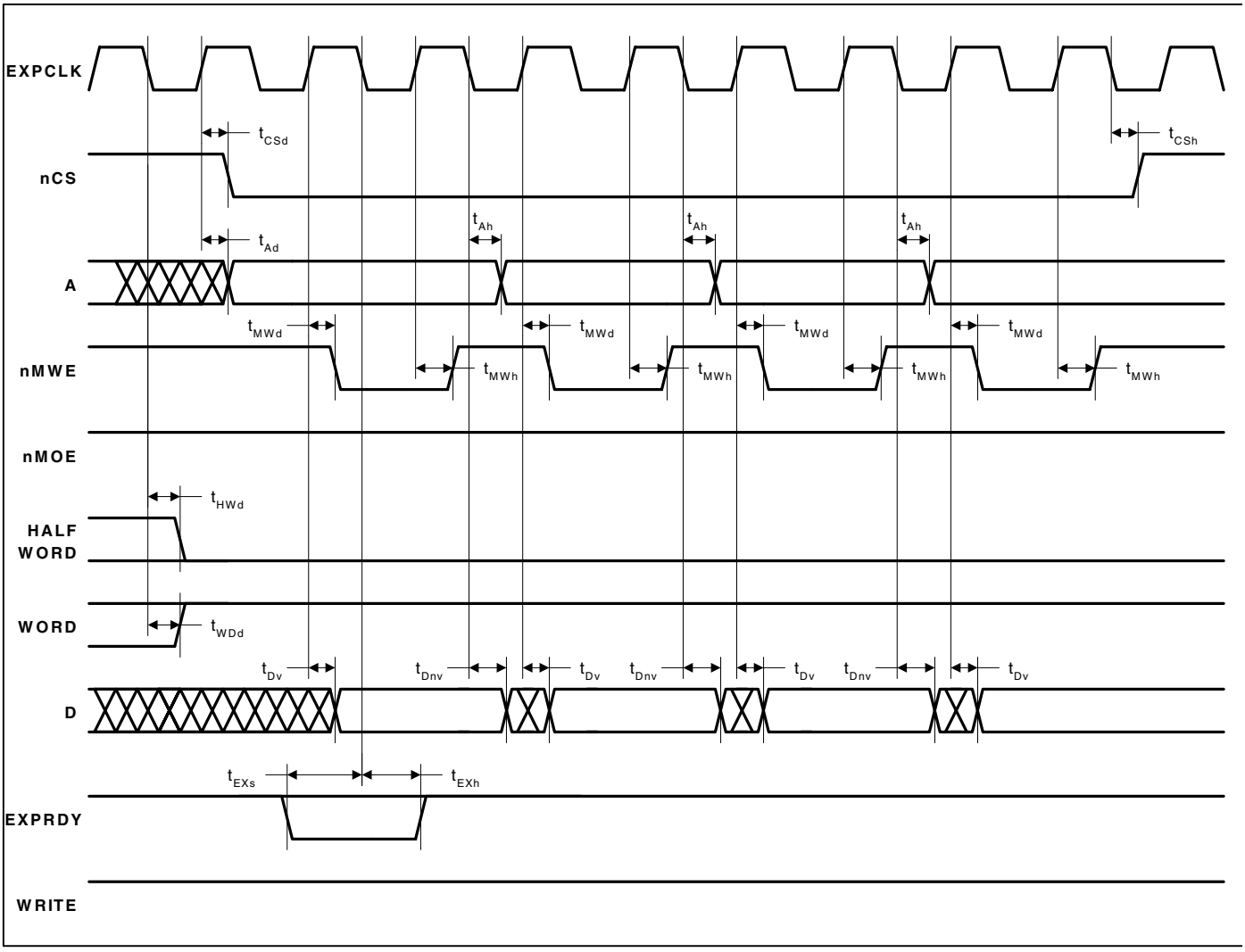

Figure 6. Static Memory Burst Write Cycle Timing Measurement

Note: 1. Four cycles are shown in the above diagram (minimum wait states, 1-1-1-1). This is the maximum number of consecutive cycles that can be driven. The number of consecutive cycles can be programmed from 2 to 4, inclusively.
2. The cycle time can be extended by integer multiples of the clock period (22 ns at 45 MHz, 27 ns at 36 MHz, 54 ns at 18.432 MHz, and 77 ns at 13 MHz), by either driving EXPRDY low and/or by programming a number of wait states. EXPRDY is sampled on the falling edge of EXPCLK before the data transfer. If low at this point, the transfer is delayed by one clock period where EXPRDY is sampled again. EXPCLK need not be referenced when driving EXPRDY, but is shown for clarity.
3. Zero wait states for sequential writes is not permitted for memory devices which use nMWE pin, as this cannot be driven with valid timing under zero wait state conditions.
4. Address, Data, Halfword, Word, and Write hold state until next cycle.

SSI2 Interface

Parameter	Symbol	Min	Max	Unit
SSICLK period (slave mode)	t_{clk_per}	185	2050	ns
SSICLK high time	t_{clk_high}	925	1025	ns
SSICLK low time	t_{clk_low}	925	1025	ns
SSICLK rise/fall time	t_{clkrf}	3	18	ns
SSICLK rising edge to RX and/or TX frame sync high time	t_{FRd}	-	3	ns
SSICLK rising edge to RX and/or TX frame sync low time	t_{FRa}	-	8	ns
SSIRXFR and/or SSITXFR period	t_{FR_per}	960	990	ns
SSIRXDA setup to SSICLK falling edge time	t_{RXs}	3	7	ns
SSIRXDA hold from SSICLK falling edge time	t_{RXh}	3	7	ns
SSICLK rising edge to SSITXDA data valid delay time	t_{TXd}	-	2	ns
SSITXDA valid time	t_{TXv}	960	990	ns

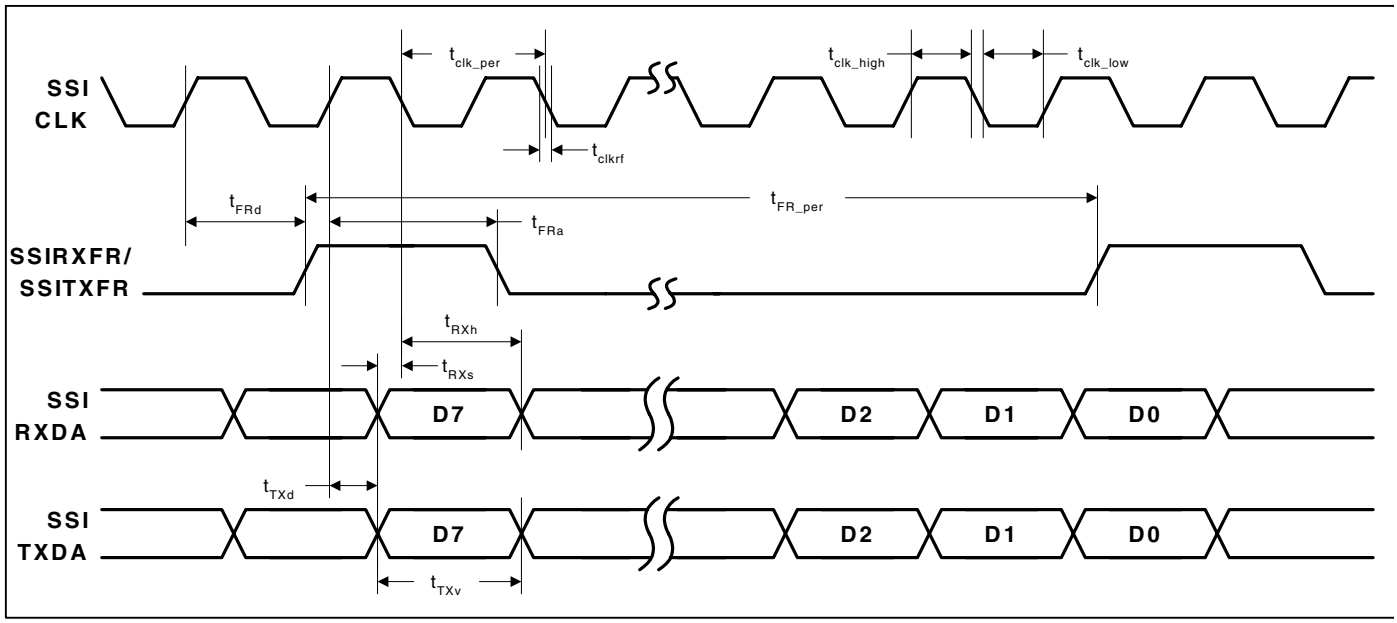

Figure 8. SSI2 Interface Timing Measurement

208-Pin LQFP Numeric Pin Listing

Table 19. 208-Pin LQFP Numeric Pin Listing

Pin No.	Signal	Type	Strength	Reset State
1	nCS[5]	O	1	High
2	VDDIO	Pad Pwr		
3	VSSIO	Pad Gnd		
4	EXPCLK	I/O	1	
5	WORD	Out	1	Low
6	WRITE	Out	1	Low
7	RUN/CLKEN	O	1	Low
8	EXPRDY	I	1	
9	TXD[2]	O	1	High
10	RXD[2]	I		
11	TDI	I	with p/u*	
12	VSSIO	Pad Gnd		
13	PB[7]	I/O	1	Input
14	PB[6]	I/O	1	Input
15	PB[5]	I/O	1	Input
16	PB[4]	I/O	1	Input
17	PB[3]	I/O	1	Input
18	PB[2]	I/O	1	Input
19	PB[1]/PRDY2	I/O	1	Input
20	PB[0]/PRDY1	I/O	1	Input
21	VDDIO	Pad Pwr		
22	TDO	O	1	Three state
23	PA[7]	I/O	1	Input
24	PA[6]	I/O	1	Input
25	PA[5]	I/O	1	Input
26	PA[4]	I/O	1	Input
27	PA[3]	I/O	1	Input
28	PA[2]	I/O	1	Input
29	PA[1]	I/O	1	Input
30	PA[0]	I/O	1	Input
31	LEDDRV	O	1	Low
32	TXD[1]	O	1	High
33	VSSIO	Pad Gnd	1	High
34	PHDIN	I		
35	CTS	I		
36	RXD[1]	I		

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
37	DCD	I		
38	DSR	I		
39	nTEST[1]	I	With p/u*	
40	nTEST[0]	I	With p/u*	
41	EINT[3]	I		
42	nEINT[2]	I		
43	nEINT[1]	I		
44	nEXTFIQ	I		
45	PE[2]/CLKSEL	I/O	1	Input
46	PE[1]/ BOOTSEL[1]	I/O	1	Input
47	PE[0]/ BOOTSEL[0]	I/O	1	Input
48	VSSRTC	RTC Gnd		
49	RTCOUT	O		
50	RTCIN	I		
51	VDDRTC	RTC power		
52	N/C			
53	PD[7]	I/O	1	Low
54	PD[6]	I/O	1	Low
55	PD[5]	I/O	1	Low
56	PD[4]	I/O	1	Low
57	VDDIO	Pad Pwr		
58	TMS	I	with p/u*	
59	PD[3]	I/O	1	Low
60	PD[2]	I/O	1	Low
61	PD[1]	I/O	1	Low
62	PD[0]/LEDFLSH	I/O	1	Low
63	SSICLK	I/O	1	Input
64	VSSIO	Pad Gnd		
65	SSITXFR	I/O	1	Low
66	SSITXDA	O	1	Low
67	SSIRXDA	I		
68	SSIRXFR	I/O		Input
69	ADCIN	I		
70	nADCCS	O	1	High
71	VSSCORE	Core Gnd		
72	VDDCORE	Core Pwr		

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
73	VSSIO	Pad Gnd		
74	VDDIO	Pad Pwr		
75	DRIVE[1]	I/O	2	High / Low
76	DRIVE[0]	I/O	2	High / Low
77	ADCCLK	O	1	Low
78	ADCOUT	O	1	Low
79	SMPCLK	O	1	Low
80	FB[1]	I		
81	VSSIO	Pad Gnd		
82	FB[0]	I		
83	COL[7]	O	1	High
84	COL[6]	O	1	High
85	COL[5]	O	1	High
86	COL[4]	O	1	High
87	COL[3]	O	1	High
88	COL[2]	O	1	High
89	VDDIO	Pad Pwr		
90	TCLK	I		
91	COL[1]	O	1	High
92	COL[0]	O	1	High
93	BUZ	O	1	Low
94	D[31]	I/O	1	Low
95	D[30]	I/O	1	Low
96	D[29]	I/O	1	Low
97	D[28]	I/O	1	Low
98	VSSIO	Pad Gnd		
99	A[27]	O	2	Low
100	D[27]	I/O	1	Low
101	A[26]	O	2	Low
102	D[26]	I/O	1	Low
103	A[25]	O	2	Low
104	D[25]	I/O	1	Low
105	HALFWORD	O	1	Low
106	A[24]	O	1	Low
107	VDDIO	Pad Pwr		—
108	VSSIO	Pad Gnd		—
109	D[24]	I/O	1	Low

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
110	A[23]	O	1	Low
111	D[23]	I/O	1	Low
112	A[22]	O	1	Low
113	D[22]	I/O	1	Low
114	A[21]	O	1	Low
115	D[21]	I/O	1	Low
116	VSSIO	Pad Gnd		
117	A[20]	O	1	Low
118	D[20]	I/O	1	Low
119	A[19]	O	1	Low
120	D[19]	I/O	1	Low
121	A[18]	O	1	Low
122	D[18]	I/O	1	Low
123	VDDIO	Pad Pwr		
124	VSSIO	Pad Gnd		
125	nTRST	I		
126	A[17]	O	1	Low
127	D[17]	I/O	1	Low
128	A[16]	O	1	Low
129	D[16]	I/O	1	Low
130	A[15]	O	1	Low
131	D[15]	I/O	1	Low
132	A[14]	O	1	Low
133	D[14]	I/O	1	Low
134	A[13]	O	1	Low
135	D[13]	I/O	1	Low
136	A[12]	O	1	Low
137	D[12]	I/O	1	Low
138	A[11]	O	1	Low
139	VDDIO	Pad Pwr		
140	VSSIO	Pad Gnd		
141	D[11]	I/O	1	Low
142	A[10]	O	1	Low
143	D[10]	I/O	1	Low
144	A[9]	O	1	Low
145	D[9]	I/O	1	Low
146	A[8]	O	1	Low
147	D[8]	I/O	1	Low

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
148	A[7]	O	1	Low
149	VSSIO	Pad Gnd		
150	D[7]	I/O	1	Low
151	nBATCHG	I		
152	nEXTPWR	I		
153	BATOK	I		
154	nPOR	I	Schmitt	
155	nMEDCHG/ nBROM	I		
156	nURESET	I	Schmitt	
157	VDDOSC	Osc Pwr		
158	MOSCIN	Osc		
159	MOSCOUT	Osc		
160	VSSOSC	Osc Gnd		
161	WAKEUP	I	Schmitt	
162	nPWRFL	I		
163	A[6]	O	1	Low
164	D[6]	I/O	1	Low
165	A[5]	Out	1	Low
166	D[5]	I/O	1	Low
167	VDDIO	Pad Pwr		
168	VSSIO	Pad Gnd		
169	A[4]	O	1	Low
170	D[4]	I/O	1	Low
171	A[3]	O	2	Low
172	D[3]	I/O	1	Low
173	A[2]	O	2	Low
174	VSSIO	Pad Gnd		
175	D[2]	I/O	1	Low
176	A[1]	O	2	Low
177	D[1]	I/O	1	Low
178	A[0]	O	2	Low
179	D[0]	I/O	1	Low
180	VSS CORE	Core Gnd		
181	VDD CORE	Core Pwr		
182	VSSIO	Pad Gnd		
183	VDDIO	Pad Pwr		
184	CL[2]	O	1	Low
185	CL[1]	O	1	Low

Table 19. 208-Pin LQFP Numeric Pin Listing (Continued)

Pin No.	Signal	Type	Strength	Reset State
186	FRM	O	1	Low
187	M	O	1	Low
188	DD[3]	I/O	1	Low
189	DD[2]	I/O	1	Low
190	VSSIO	Pad Gnd		
191	DD[1]	I/O	1	Low
192	DD[0]	I/O	1	Low
193	N/C	O	1	High
194	N/C	O	1	High
195	N/C	I/O	2	Low
196	N/C	I/O	2	Low
197	VDDIO	Pad Pwr		
198	VSSIO	Pad Gnd		
199	N/C	I/O	2	Low
200	N/C	I/O	2	Low
201	nMWE	O	1	High
202	nMOE	O	1	High
203	VSSIO	Pad Gnd		
204	nCS[0]	O	1	High
205	nCS[1]	O	1	High
206	nCS[2]	O	1	High
207	nCS[3]	O	1	High
208	nCS[4]	O	1	High

*With p/u' means with internal pull-up on the pin.

204-Ball TFBGA Ball Listing

The list is ordered by ball location.

Table 20. 204-Ball TFBGA Ball Listing

Ball Location	Name	Strength†	Reset State	Type	Description
A1	VDDIO			Pad power	Digital I/O power, 3.3 V
A2	EXPCLK	1		I	Expansion clock input
A3	nCS[3]	1	High	O	Chip select 3
A4	nCS[1]	1	High	O	Chip select 1
A5	nMWE/nSDWE	1	High	O	ROM, expansion write enable/ SDRAM write enable control signal
A6	N/C				
A7	N/C				
A8	DD[2]	1	Low	O	LCD serial display data
A9	FRM	1	Low	O	LCD frame synchronization pulse
A10	CL[1]	1	Low	O	LCD line clock
A11	VSSCORE			Core ground	Core ground
A12	D[1]	1	Low	I/O	Data I/O
A13	A[2]	2	Low	O	System byte address
A14	D[4]	1	Low	I/O	Data I/O
A15	A[5]	1	Low	O	System byte address
A16	nPWRFL			I	Power fail sense input
A17	MOSCOUT			O	Main oscillator out
A18	VSSIO			Pad ground	I/O ground
A19	VSSIO			Pad ground	I/O ground
A20	VSSIO			Pad ground	I/O ground
B1	WORD	1	Low	O	Word access select output
B2	VDDIO			Pad power	Digital I/O power, 3.3 V
B3	nCS[5]	1	Low	O	Chip select 5
B4	nCS[2]	1	High	O	Chip select 2
B5	nMOE/nSDCAS	1	High	O	ROM, expansion OP enable/SDRAM CAS control signal
B6	N/C				
B7	N/C				
B8	DD[1]	1	Low	O	LCD serial display data
B9	M	1	Low	O	LCD AC bias drive
B10	CL[2]	1	Low	0	LCD pixel clock out
B11	D[0]	1	Low	I/O	Data I/O
B12	A[1]	2	Low	O	System byte address
B13	D[3]	2	Low	I/O	Data I/O
B14	A[4]	1	Low	O	System byte address

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
B15	D[6]	1	Low	I/O	Data I/O
B16	WAKEUP	Schmitt		I	System wake up input
B17	MOSCIN			I	Main oscillator input
B18	VSSIO			Pad ground	I/O ground
B19	VSSIO			Pad ground	I/O ground
B20	nURESET	Schmitt		I	User reset input
C1	RUN/CLKEN	1	Low	0	Run output / clock enable output
C2	EXPRDY	1		I	Expansion port ready input
C3	VDDIO			Pad power	Digital I/O power, 3.3 V
C4	nCS[4]	1	High	O	Chip select 4
C5	nCS[0]	1	High	O	Chip select 0
C6	N/C				
C7	N/C				
C8	DD[0]	1	Low	O	LCD serial display data
C9	DD[3]	1	Low	O	LCD serial display data
C10	VDDCORE			Core power	Digital core power, 2.5 V
C11	A[0]	2	Low	O	System byte address
C12	D[2]	1	Low	I/O	Data I/O
C13	A[3]	2	Low	O	System byte address
C14	D[5]	1	Low	I/O	Data I/O
C15	A[6]	1	Low	O	System byte address
C16	VSSOSC			Oscillator ground	PLL ground
C17	VDDOSC			Oscillator power	Oscillator power in, 2.5V
C18	VSSIO			Pad ground	I/O ground
C19	BATOK			I	Battery ok input

Table 20. 204-Ball TFBGA Ball Listing (Continued)

Ball Location	Name	Strength†	Reset State	Type	Description
C20	nPOR	Schmitt		I	Power-on reset input
D1	PB[7]	1	Input‡	I	GPIO port B
D2	RXD[2]			I	UART 2 receive data input
D3	VDDIO			Pad power	Digital I/O power, 3.3V
D18	VSSIO			Pad ground	I/O ground
D19	nBATCHG			I	Battery changed sense input
D20	A[7]	1	Low	O	System byte address
E1	PB[4]	1	Input‡	I	GPIO port B
E2	TXD[2]	1	High	O	UART 2 transmit data output
E3	WRITE/nSDRAS	1	Low	O	Transfer direction / SDRAM RAS signal output
E18	nMEDCHG/nBROM			I	Media change interrupt input / internal ROM boot enable
E19	nEXTPWR			I	External power supply sense input
E20	D[9]	1	Low	I/O	Data I/O
F1	PB[3]	1	Input‡	I/O	GPIO port B
F2	PB[6]	1	Input‡	I/O	GPIO port B
F3	TDI	with p/u*		I	JTAG data input
F18	D[7]	1	Low	I/O	Data I/O
F19	A[8]	1	Low	O	System byte address
F20	D[10]	1	Low	I/O	Data I/O
G1	PB[1]	1	Input‡	I/O	
G2	PB[2]	1	Input‡	I/O	GPIO port B
G3	PB[5]	1	Input‡	I/O	GPIO port B
G18	D[8]	1	Input‡	I/O	Data I/O
G19	A[9]	1	Low	O	System byte address
G20	D[11]	1	Low	I/O	Data I/O
H1	PA[7]	1	Input‡	I/O	GPIO port A
H[2]	TDO	1	Input‡	O	JTAG data out
H[3]	PB[0]	1	Input‡	I/O	GPIO port B
H[18]	A[10]	1	Low	O	System byte address
H19	D[12]	1	Low	I/O	Data I/O
H20	A[12]	1	Low	O	System byte address
J1	PA[4]	1	Input‡	I/O	GPIO port A

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
H6	PB[0]/PRDY[1]	I	GPIO port B / CL-PS6700 interface signal
H7	PB[2]	I	GPIO port B
H8	VSSRTC	RTC ground	Real time clock ground
H9	VSSRTC	RTC ground	Real time clock ground
H10	A[10]	O	System byte address
H11	A[11]	O	System byte address
H12	A[12]	O	System byte address
H13	A[13]	O	System byte address
H14	VSSIO	Pad ground	I/O ground
H15	D[14]	I/O	Data I/O
H16	D[15]	I/O	Data I/O
J1	PA[3]	I	GPIO port A
J2	PA[1]	I	GPIO port A
J3	VSSIO	Pad ground	I/O ground
J4	PA[2]	I	GPIO port A
J5	PA[0]	I	GPIO port A
J6	TXD[1]	O	UART 1 transmit data out
J7	CTS	I	UART 1 clear to send input
J8	VSSRTC	RTC ground	Real time clock ground
J9	VSSRTC	RTC ground	Real time clock ground
J10	A[17]	O	System byte address
J11	A[16]	O	System byte address
J12	A[15]	O	System byte address
J13	A[14]	O	System byte address
J14	nTRST	I	JTAG async reset input
J15	D[16]	I/O	Data I/O
J16	D[17]	I/O	Data I/O
K1	LEDDRV	O	IR LED drivet
K2	PHDIN	I	Photodiode input
K3	VSSIO	Pad ground	I/O ground
K4	DCD	I	UART 1 data carrier detect
K5	nTEST[1]	I	Test mode select input
K6	EINT[3]	I	External interrupt
K7	VSSRTC	RTC ground	Real time clock ground
K8	ADCIN	I	SSI1 ADC serial input
K9	COL[4]	O	Keyboard scanner column drive
K10	TCLK	I	JTAG clock
K11	D[20]	I/O	Data I/O
K12	D[19]	I/O	Data I/O
K13	D[18]	I/O	Data I/O
K14	VSSIO	Pad ground	I/O ground
K15	VDDIO	Pad power	Digital I/O power, 3.3V
K16	VDDIO	Pad power	Digital I/O power, 3.3V
L1	RXD[1]	I	UART 1 receive data input
L2	DSR	I	UART 1 data set ready input
L3	VDDIO	Pad power	Digital I/O power, 3.3V
L4	nEINT[1]	I	External interrupt input
L5	PE[2]/CLKSEL	I	GPIO port E / clock input mode select

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
L6	VSSRTC	RTC ground	Real time clock ground
L7	PD[0]/LEDFLSH	I/O	GPIO port D / LED blinker output
L8	VSSRTC	Core ground	Real time clock ground
L9	COL[6]	O	Keyboard scanner column drive
L10	D[31]	I/O	Data I/O
L11	VSSRTC	RTC ground	Real time clock ground
L12	A[22]	O	System byte address
L13	A[21]	O	System byte address
L14	VSSIO	Pad ground	I/O ground
L15	A[18]	O	System byte address
L16	A[19]	O	System byte address
M1	nTEST[0]	I	Test mode select input
M2	nEINT[2]	I	External interrupt input
M3	VDDIO	Pad power	Digital I/O power, 3.3V
M4	PE[0]/BOOTSEL[0]	I	GPIO port E / Boot mode select
M5	TMS	I	JTAG mode select
M6	VDDIO	Pad power	Digital I/O power, 3.3V
M7	SSITXFR	I/O	DAI/CODEC/SSI2 frame sync
M8	DRIVE[1]	I/O	PWM drive output
M9	FB[0]	I	PWM feedback input
M10	COL[0]	O	Keyboard scanner column drive
M11	D[27]	I/O	Data I/O
M12	VSSIO	Pad ground	I/O ground
M13	A[23]	O	System byte address
M14	VDDIO	Pad power	Digital I/O power, 3.3V
M15	A[20]	O	System byte address
M16	D[21]	I/O	Data I/O
N1	nEXTFIQ	I	External fast interrupt input
N2	PE[1]/BOOTSEL[1]	I	GPIO port E / boot mode select
N3	VSSIO	Pad ground	I/O ground
N4	VDDIO	Pad power	Digital I/O power, 3.3V
N5	PD[5]	I/O	GPIO port D
N6	PD[2]	I/O	GPIO port D
N7	SSIRXDA	I/O	DAI/CODEC/SSI2 serial data input
N8	ADCCLK	O	SSI1 ADC serial clock
N9	SMPCLK	O	SSI1 ADC sample clock
N10	COL[2]	O	Keyboard scanner column drive
N11	D[29]	I/O	Data I/O
N12	D[26]	I/O	Data I/O
N13	HALFWORD	O	Halfword access select output
N14	VSSIO	Pad ground	I/O ground
N15	D[22]	I/O	Data I/O
N16	D[23]	I/O	Data I/O
P1	VSSRTC	RTC ground	Real time clock ground
P2	RTCOUT	O	Real time clock oscillator output
P3	VSSIO	Pad ground	I/O ground
P4	VSSIO	Pad ground	I/O ground
P5	VDDIO	Pad power	Digital I/O power, 3.3V

Table 21. 256-Ball PBGA Ball Listing (Continued)

Ball Location	Name	Type	Description
P6	VSSIO	Pad ground	I/O ground
P7	VSSIO	Pad ground	I/O ground
P8	VDDIO	Pad power	Digital I/O power, 3.3V
P9	VSSIO	Pad ground	I/O ground
P10	VDDIO	Pad power	Digital I/O power, 3.3V
P11	VSSIO	Pad ground	I/O ground
P12	VSSIO	Pad ground	I/O ground
P13	VDDIO	Pad power	Digital I/O power
P14	VSSIO	Pad ground	I/O ground
P15	D[24]	I/O	Data I/O
P16	VDDIO	Pad power	Digital I/O power, 3.3V
R1	RTCIN	I/O	Real time clock oscillator input
R2	VDDIO	Pad power	Digital I/O power, 3.3V
R3	PD[4]	I/O	GPIO port D
R4	PD[1]	I/O	GPIO port D
R5	SSITXDA	O	DAI/CODEC/SSI2 serial data output
R6	nADCCS	O	SSI1 ADC chip select
R7	VDDIO	Pad power	Digital I/O power, 3.3V
R8	ADCOUT	O	SSI1 ADC serial data output
R9	COL[7]	O	Keyboard scanner column drive
R10	COL[3]	O	Keyboard scanner column drive
R11	COL[1]	O	Keyboard scanner column drive
R12	D[30]	I/O	Data I/O
R13	A[27]	O	System byte address
R14	A[25]	O	System byte address
R15	VDDIO	Pad power	Digital I/O power, 3.3V
R16	A[24]	O	System byte address
T1	VDDRTC	RTC power	Real time clock power, 2.5V
T2	PD[7]	I/O	GPIO port D
T3	PD[6]	I/O	GPIO port D
T4	PD[3]	I/O	GPIO port D
T5	SSICLK	I/O	DAI/CODEC/SSI2 serial clock
T6	SSIRXFR	–	DAI/CODEC/SSI2 frame sync
T7	VDDCORE	Core power	Core power, 2.5V
T8	DRIVE[0]	I/O	PWM drive output
T9	FB[1]	I	PWM feedback input
T10	COL[5]	O	Keyboard scanner column drive
T11	VDDIO	Pad power	Digital I/O power, 3.3V
T12	BUZ	O	Buzzer drive output
T13	D[28]	I/O	Data I/O
T14	A[26]	O	System byte address
T15	D[25]	I/O	Data I/O
T16	VSSIO	Pad ground	I/O ground

JTAG Boundary Scan Signal Ordering

Table 22. JTAG Boundary Scan Signal Ordering

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
1	B3	B1	nCS[5]	O	1
4	A2	C2	EXPCLK	I/O	3
5	B1	E4	WORD	O	6
6	E3	D1	WRITE	O	8
7	C1	F5	RUN/CLKEN	O	10
8	C2	D2	EXPRDY	I	13
9	E2	F4	TXD2	O	14
10	D2	E1	RXD2	I	16
13	F3	E2	PB[7]	I/O	17
14	D1	G5	PB[6]	I/O	20
15	F2	F1	PB[5]	I/O	23
16	G3	G4	PB[4]	I/O	26
17	E1	F2	PB[3]	I/O	29
18	F1	H7	PB[2]	I/O	32
19	G2	G1	PB[1]/PRDY2	I/O	35
20	G1	H6	PB[0]/PRDY1	I/O	38
23	H3	H1	PA[7]	I/O	41
24	H1	H5	PA[6]	I/O	44
25	J3	H2	PA[5]	I/O	47
26	J2	H4	PA[4]	I/O	50
27	J1	J1	PA[3]	I/O	53
28	L3	J4	PA[2]	I/O	56
29	K2	J2	PA[1]	I/O	59
30	K1	J5	PA[0]	I/O	62
31	M3	K1	LEDDRV	O	65
32	L2	J6	TXD1	O	67
34	L1	K2	PHDIN	I	69
35	N3	J7	CTS	I	70
36	M2	L1	RXD1	I	71
37	M1	K4	DCD	I	72
38	P3	L2	DSR	I	73
39	N1	K5	nTEST1	I	74
40	N2	M1	nTEST0	I	75
41	R3	K6	EINT3	I	76
42	P1	M2	nEINT2	I	77
43	P2	L4	nEINT1	I	78

Table 22. JTAG Boundary Scan Signal Ordering (Continued)

LQFP Pin No.	TFBGA Ball	PBGA Ball	Signal	Type	Position
102	Y17	N12	D[26]	I/O	179
103	W17	R14	A[25]	O	182
104	Y18	T15	D[25]	I/O	184
105	V17	N13	HALFWORD	O	187
106	W18	R16	A[24]	O	189
109	Y19	P15	D[24]	I/O	191
110	W20	M13	A[23]	O	194
111	U18	N16	D[23]	I/O	196
112	V20	L12	A[22]	O	199
113	U19	N15	D[22]	I/O	201
114	U20	L13	A[21]	O	204
115	T19	M16	D[21]	I/O	206
117	T20	M15	A[20]	O	209
118	R19	K11	D[20]	I/O	211
119	R20	L16	A[19]	O	214
120	T18	K12	D[19]	I/O	216
121	P19	L15	A[18]	O	219
122	P20	K13	D[18]	I/O	221
126	R18	J10	A[17]	O	224
127	N19	J16	D[17]	I/O	226
128	N20	J11	A[16]	O	229
129	P18	J15	D[16]	I/O	231
130	M19	J12	A[15]	O	234
131	N18	H16	D[15]	I/O	236
132	L20	J13	A[14]	O	239
133	L19	H15	D[14]	I/O	241
134	M18	H13	A[13]	O	244
135	K20	G16	D[13]	I/O	246
136	K19	H12	A[12]	O	249
137	K18	G15	D[12]	I/O	251
138	J20	H11	A[11]	O	254
141	J19	F15	D[11]	I/O	256
142	H20	H10	A[10]	O	259
143	H19	E16	D[10]	I/O	261
144	J18	G13	A[9]	O	264
145	K3	E15	D[9]	I/O	266
146	Y3	G12	A[8]	O	269
147	G20	D16	D[8]	I/O	271

CONVENTIONS

This section presents acronyms, abbreviations, units of measurement, and conventions used in this data sheet.

Acronyms and Abbreviations

Table 23 lists abbreviations and acronyms used in this data sheet.

Table 23. Acronyms and Abbreviations

Acronym/ Abbreviation	Definition
A/D	analog-to-digital
ADC	analog-to-digital converter
CODEC	coder / decoder
D/A	digital-to-analog
DMA	direct-memory access
EPB	embedded peripheral bus
FCS	frame check sequence
FIFO	first in / first out
FIQ	fast interrupt request
GPIO	general purpose I/O
ICT	in circuit test
IR	infrared
IRQ	standard interrupt request
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	liquid crystal display
LED	light-emitting diode
LQFP	low profile quad flat pack
LSB	least significant bit
MIPS	millions of instructions per second
MMU	memory management unit
MSB	most significant bit
PBGA	plastic ball grid array
PCB	printed circuit board
PDA	personal digital assistant
PLL	phase locked loop
p/u	pull-up resistor
RISC	reduced instruction set computer
RTC	Real-Time Clock
SIR	slow (9600–115.2 kbps) infrared
SRAM	static random access memory
SSI	synchronous serial interface

Table 23. Acronyms and Abbreviations (Continued)

Acronym/ Abbreviation	Definition
TAP	test access port
TLB	translation lookaside buffer
UART	universal asynchronous receiver

Units of Measurement

Table 24. Unit of Measurement

Symbol	Unit of Measure
°C	degree Celsius
fs	sample frequency
Hz	hertz (cycle per second)
kbps	kilobits per second
KB	kilobyte (1,024 bytes)
kHz	kilohertz
kΩ	kilohm
Mbps	megabits (1,048,576 bits) per second
MB	megabyte (1,048,576 bytes)
MBps	megabytes per second
MHz	megahertz (1,000 kilohertz)
µA	microampere
µF	microfarad
µW	microwatt
µs	microsecond (1,000 nanoseconds)
mA	milliampere
mW	milliwatt
ms	millisecond (1,000 microseconds)
ns	nanosecond
V	volt
W	watt