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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1184agj-gae-ax

Table 2-4. Connection of Unused Pins (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P140/PCLBUZ0/INTP6	8-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P141/PCLBUZ1/INTP7			
P142/$\overline{\text{SCK20}}$/SCL20	5-AN		
P143/SI20/RxD2/SDA20			
P144/SO20/TxD2	5-AG		
P145/TI07/TO07	8-R		
P146, P147	5-AG		
P150/ANI8 to P157/ANI15[Note]	11-G		Input: Independently connect to AV_{REF0} or AV_{SS} via a resistor. Output: Leave open.
P160/TI10/TO10 to P163/TI13/TO13	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
AV_{REF0}	–	–	Make this pin the same potential as EV_{DD0}, EV_{DD1}, or V_{DD}. See **2.2.18 AV_{REF0}** when using P20 to P27 and P150 to P157.
AV_{REF1}	–	–	Make this pin the same potential as EV_{DD0}, EV_{DD1}, or V_{DD}. See **2.2.19 AV_{REF1}** when using P110 and P111.
AV_{SS}	–	–	Make this pin the same potential as the EV_{SS0}, EV_{SS1}, or V_{SS}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{\text{RESET}}$	2	Input	Connect directly or via a resistor to EV_{DD0} or EV_{DD1}.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF).

Notes P150/ANI8 to P157/ANI15 are set in the digital input port mode after release of reset.

5.8.3 Connection of asynchronous memory

Use the separate bus mode for connecting an asynchronous memory.

Figure 5-11. Example of Asynchronous Memory Connection

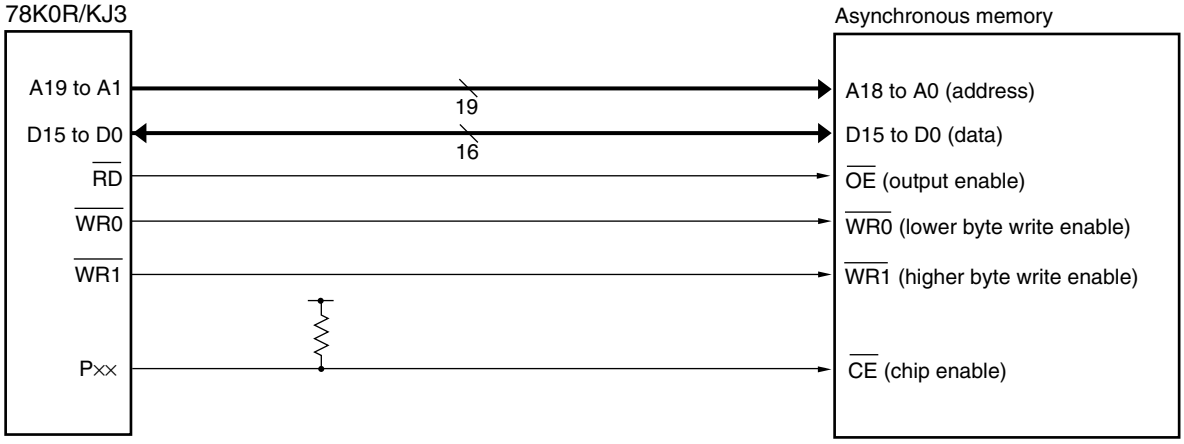


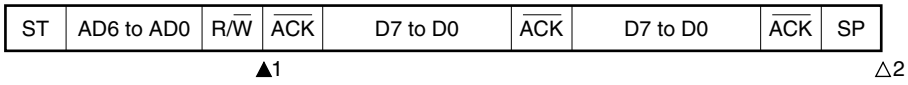
Figure 7-44. Operation Procedure When External Event Counter Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN bit, TAU1EN bit of the PER0 register to 1. →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets the TPSm register. Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets the TMRmn register (determines operation mode of channel). Sets number of counts to the TDRmn register. Clears the TOEmn bit of the TOEm register to 0.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and count operation starts. Value of TDRmn is loaded to TCRmn and detection of the TImn pin input edge is awaited.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	Counter (TCRmn) counts down each time input edge of the TImn pin has been detected. When count value reaches 0000H, the value of TDRmn is loaded to TCRmn again, and the count operation is continued. By detecting TCRmn = 0000H, the INTTMmn output is generated. After that, the above operation is repeated.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. TCRmn holds count value and stops.
TAU stop	The TAU0EN bit, TAU1EN bit of the PER0 register are cleared to 0. →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

(b) When arbitration loss occurs during transmission of extension code

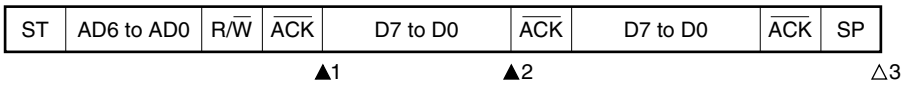


▲1: IICS0 = 0110×010B
Sets LREL0 = 1 by software
△2: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(c) When arbitration loss occurs during transmission of data

(i) When WTIM0 = 0



▲1: IICS0 = 10001110B
▲2: IICS0 = 01000000B
△3: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1

(9/13)

Edition	Description	Chapter
3rd Edition	Addition of **8.4.5 1 Hz output of real-time counter**	CHAPTER 8 REAL-TIME COUNTER (continuation)
	Addition of **8.4.6 32.768 kHz output of real-time counter**	
	Addition of **8.4.7 512 Hz, 16.384 kHz output of real-time counter**	
	Addition of **8.4.8 Example of watch error correction of real-time counter**	
	Change of **Caution 3** in **Table 9-4 Setting Window Open Period of Watchdog Timer**	CHAPTER 9 WATCHDOG TIMER
	Change of description in **11.2 (9) AV_{REF0} pin**	CHAPTER 11 A/D CONVERTER
	Change of **Table 11-3 A/D Conversion Time Selection**	
	Change of **Figure 11-6. A/D Converter Sampling and A/D Conversion Timing**	
	Addition of **Caution 3** to **Figure 11-10 Format of A/D Port Configuration Register (ADPC)**	
	Addition of **11.5 Temperature Sensor Function**	
	Addition of **11.7 (2) Reducing current when A/D converter is stopped**	
	Addition of **12.2 (1) AV_{REF1} pin**	CHAPTER 12 D/A CONVERTER
	Addition of **12.3 (4) Port mode register 11 (PM11)**	
	Change of description in **12.4.1 Operation in normal mode**	
	Change of description in **12.4.2 Operation in real-time output mode**	
	Addition of **Note** to **13.1.3 Simplified I^2C (IIC10, IIC11, IIC20 IIC21)**	CHAPTER 13 SERIAL ARRAY UNIT
	Change of **Note 2** in **Figure 13-5 Format of Serial Clock Select Register m (SPSm)**	
	Change of **Figure 13-7 Format of Serial Communication Operation Setting Register mn (SCRmn)**	
	Change of **Figure 13-26 Procedure for Stopping Master Transmission**	
	Change of **Figure 13-28 Timing Chart of Master Transmission (in Single-Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **Figure 13-30 Timing Chart of Master Transmission (in Continuous Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-36 Timing Chart of Master Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **Figure 13-40 Procedure for Stopping Master Transmission/Reception**	
	Change of **Figure 13-41 Procedure for Resuming Master Transmission/Reception**	
	Modification of **Figure 13-42 Timing Chart of Master Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-44 Timing Chart of Master Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of transfer rate in **13.5.4 Slave transmission**	
	Change of **Figure 13-48 Procedure for Stopping Slave Transmission**	
	Change of **Figure 13-49 Procedure for Resuming Slave Transmission**	
	Change of **Figure 13-50 Timing Chart of Slave Transmission (in Single-Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **Figure 13-52 Timing Chart of Slave Transmission (in Continuous Transmission Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	