Renesas Electronics America Inc - UPD78F1185AGJ-GAE-AX Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1185agj-gae-ax

3.4.8 Based indexed addressing

[Function]

Based indexed addressing uses the contents of a register pair specified with the instruction word as the base address, and the content of the B register or C register similarly specified with the instruction word as offset address. The sum of these values is used to specify the target address.

[Operand format]

Identifier	Description
–	[HL+B], [HL+C] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[HL+B], ES:[HL+C] (higher 4-bit addresses are specified by the ES register)

Figure 3-38. Example of [HL+B], [HL+C]

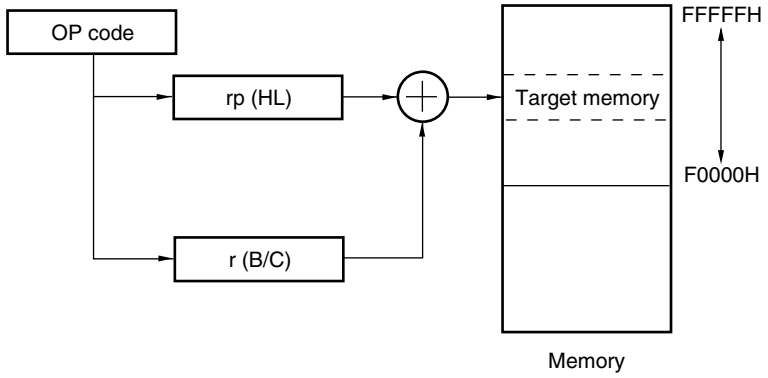


Figure 3-39. Example of ES:[HL+B], ES:[HL+C]

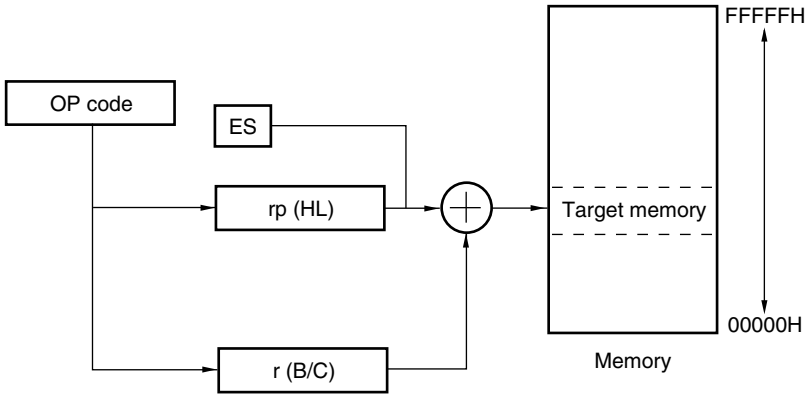
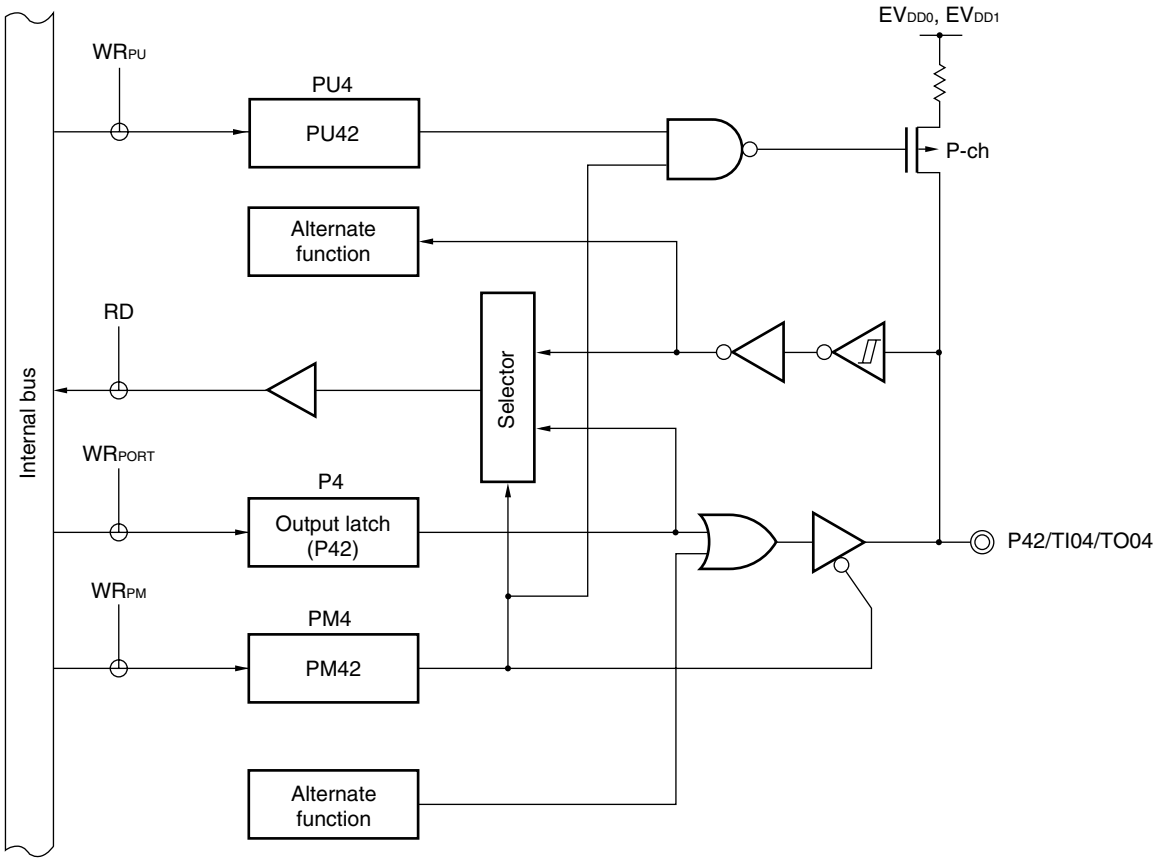


Figure 4-19. Block Diagram of P42



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

(4) Port input mode registers (PIM0, PIM4, PIM9, PIM12, PIM14)

These registers set the input buffer of P03, P04, P43, P44, P95, P96, P125, P126, P142, and P143 in 1-bit units.

TTL input buffer can be selected during serial communication with an external device of the different potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-56. Format of Port Input Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PIM0	0	0	0	PIM04	PIM03	0	0	0	F0040H	00H	R/W
PIM4	0	0	0	PIM44	PIM43	0	0	0	F0044H	00H	R/W
PIM9	0	PIM96	PIM95	0	0	0	0	0	F0049H	00H	R/W
PIM12	0	PIM126	PIM125	0	0	0	0	0	F004CH	00H	R/W
PIM14	0	0	0	0	PIM143	PIM142	0	0	F004EH	00H	R/W

PIMmn	Pmn pin input buffer selection (m = 0, 4, 9, 12, 14; n = 2 to 6)
0	Normal input buffer
1	TTL input buffer

4.4.4 Connecting to external device with different power potential (2.5 V, 3 V)

When parts of ports 0, 4, 9, 12 and 14 operate with V_{DD} = 4.0 V to 5.5 V, I/O connections with an external device that operates on 2.5 V or 3 V power supply voltage are possible.

Regarding inputs, CMOS/TTL switching is possible on a bit-by-bit basis by port input mode registers (PIM0, PIM4, PIM9, PIM12, PIM14).

Moreover, regarding outputs, different power potentials can be supported by switching the output buffer to the N-ch open drain (V_{DD} withstand voltage) by the port output mode registers (POM0, POM4, POM9, POM12, POM14).

(1) Setting procedure when using I/O pins of UART1, UART2, CSI01, CSI10, CSI11, CSI20 and CSI21 functions

(a) Use as 2.5 V or 3 V input port

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> If pull-up is needed, externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART1:	P03
In case of UART2:	P143
In case of CSI01:	P43, P44
In case of CSI10:	P03, P04
In case of CSI11:	P95, P96
In case of CSI20:	P142, P143
In case of CSI21:	P125, P126

<3> Set the corresponding bit of the PIMn register to 1 to switch to the TTL input buffer.

<4> V_{IH}/V_{IL} operates on 2.5 V or 3 V operating voltage.

(b) Use as 2.5 V or 3 V output port

<1> After reset release, the port mode changes to the input mode (Hi-Z).

<2> Pull up externally the pin to be used (on-chip pull-up resistor cannot be used).

In case of UART1:	P02
In case of UART2:	P144
In case of CSI01:	P43, P45
In case of CSI10:	P02, P04
In case of CSI11:	P95, P97
In case of CSI20:	P142, P144
In case of CSI21:	P125, P127

<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POMn register to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.

<5> Set the output mode by manipulating the PMn register.
At this time, the output data is high level, so the pin is in the Hi-Z state.

<6> Operation is done only in the low level according to the operating status of the serial array unit.

Remark n = 0, 4, 9, 12, 14

(1) Peripheral enable register 0 (PER0)

PER0 is used to enable or disable use of each peripheral hardware macro. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the timer array unit 0 is used, be sure to set bit 0 (TAU0EN) of this register to 1.

When the timer array unit 1 is used, be sure to set bit 1 (TAU1EN) of this register to 1.

PER0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-5. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN	DACEN	ADCEN	IIC0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN

TAUmEN	Control of timer array unit m input clock
0	Stops supply of input clock. • SFR used by the timer array unit m cannot be written. • The timer array unit m is in the reset status.
1	Supplies input clock. • SFR used by the timer array unit m can be read/written.

Caution When setting the timer array unit, be sure to set TAUmEN to 1 first. If TAUmEN = 0, writing to a control register of the timer array unit is ignored, and all read values are default values (except for timer input select register m (TISm), input switch control register (ISC), noise filter enable registers 1, 2 (NFEN1, 2), port mode registers 0, 1, 3, 4, 13, 14, 16 (PM0, PM1, PM3, PM4, PM13, PM14, PM16), and port registers 0, 1, 3, 4, 13, 14, 16 (P0, P1, P3, P4, P13, P14, P16)).

Remark m = 0, 1

(2) Timer clock select register m (TPSm)

TPSm is a 16-bit register that is used to select two types of operation clocks (CKm0, CKm1) that are commonly supplied to each channel. CKm1 is selected by bits 7 to 4 of TPSm, and CKm0 is selected by bits 3 to 0.

Rewriting of TPSm during timer operation is possible only in the following cases.

Rewriting of PRSm00 to PRSm03 bits: Possible only when all the channels set to CKSmn = 0 are in the operation stopped state (TEmn = 0)

Rewriting of PRSm10 to PRSm13 bits: Possible only when all the channels set to CKSmn = 1 are in the operation stopped state (TEmn = 0)

TPSm can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of TPSm can be set with an 8-bit memory manipulation instruction with TPSmL.

Reset signal generation clears this register to 0000H.

(9) Timer output enable register m (TOEm)

TOEm is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of the timer output register (TOm) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOmn).

TOEm can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of TOEm can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

Figure 7-18. Format of Timer Output Enable Register m (TOEm)

Address: F01BAH, F01BBH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00

Address: F01E2H, F01E3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE1	0	0	0	0	0	0	0	0	0	0	0	0	TOE13	TOE12	TOE11	TOE10

TOEmn	Timer output enable/disable of channel n
0	The TOmn operation stopped by count operation (timer channel output bit). Writing to the TOmn bit is enabled. The TOmn pin functions as data output, and it outputs the level set to the TOmn bit. The output level of the TOmn pin can be manipulated by software.
1	The TOmn operation enabled by count operation (timer channel output bit). Writing to the TOmn bit is disabled (writing is ignored). The TOmn pin functions as timer output, and the TOEmn is set or reset depending on the timer operation. The TOmn pin outputs the square-wave or PWM depending on the timer operation.

Caution Be sure to clear bits 15 to 8 of TOE0 and bits 15 to 4 of TOE1 to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

7.7.4 Operation as input pulse interval measurement

The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured.

The pulse interval can be calculated by the following expression.

TImn input pulse interval = Period of count clock × ((10000H × TSRmn: OVF) + (Capture value of TDRmn + 1))

Caution The TImn pin input is sampled using the operating clock selected with the CKSmn bit of the TMRmn register, so an error equal to the number of operating clocks occurs.

TCRmn operates as an up counter in the capture mode.

When the channel start trigger (TSmn) is set to 1, TCRmn counts up from 0000H in synchronization with the count clock.

When the TImn pin input valid edge is detected, the count value is transferred (captured) to TDRmn and, at the same time, the counter (TCRmn) is cleared to 0000H, and the INTTMmn is output. If the counter overflows at this time, the OVF bit of the TSRmn register is set to 1. If the counter does not overflow, the OVF bit is cleared. After that, the above operation is repeated.

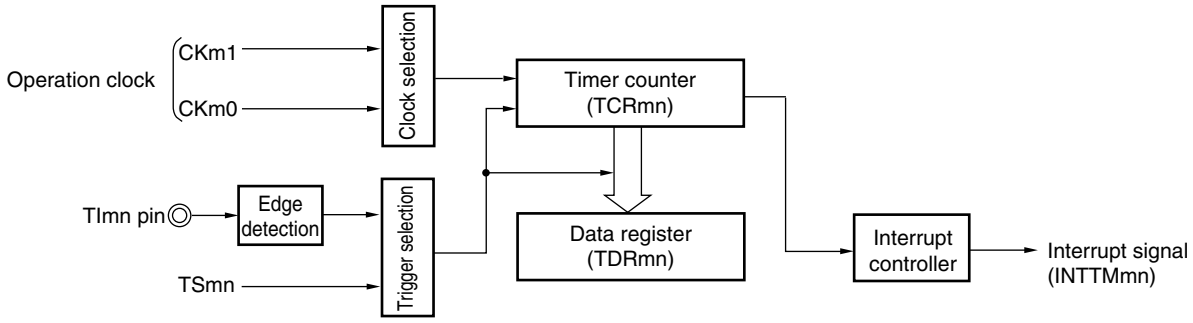
As soon as the count value has been captured to the TDRmn register, the OVF bit of the TSRmn register is updated depending on whether the counter overflows during the measurement period. Therefore, the overflow status of the captured value can be checked.

If the counter reaches a full count for two or more periods, it is judged to be an overflow occurrence, and the OVF bit of the TSRmn register is set to 1. However, the OVF bit is configured as a cumulative flag, the correct interval value cannot be measured if an overflow occurs more than once.

Set STSmn2 to STSmn0 of the TMRmn register to 001B to use the valid edges of TImn as a start trigger and a capture trigger.

When TEmn = 1, instead of the TImn pin input, a software operation (TSmn = 1) can be used as a capture trigger.

Figure 7-49. Block Diagram of Operation as Input Pulse Interval Measurement



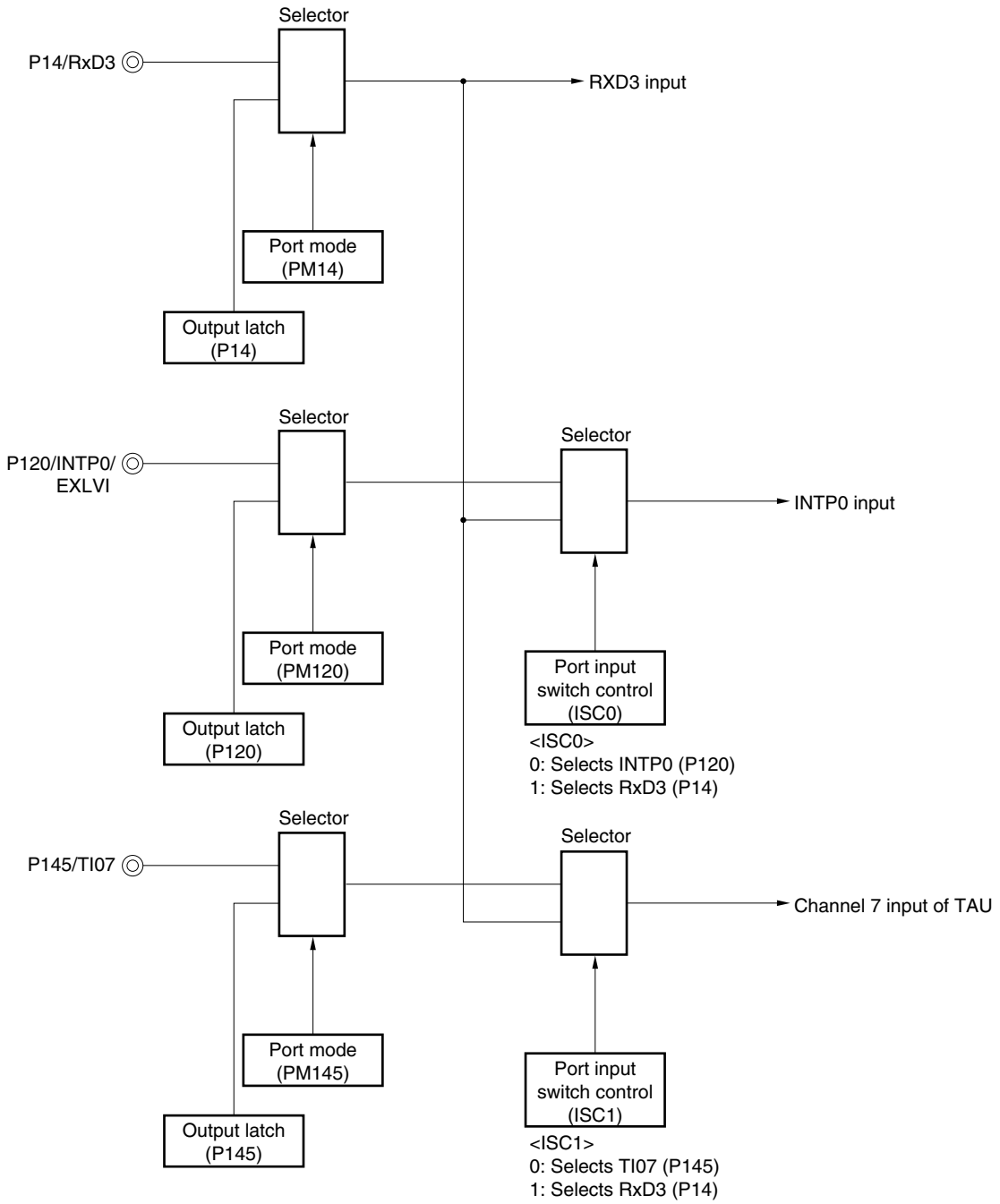
Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7),
mn = 00 to 07, 10 to 13

Figure 13-88 shows the configuration of a port that manipulates reception of LIN.

The wakeup signal transmitted from the master of LIN is received by detecting an edge of an external interrupt (INTP0). The length of the sync field transmitted from the master can be measured by using the external event capture operation of the timer array unit (TAU) to calculate a baud-rate error.

By controlling switch of port input (ISC0/ISC1), the input source of port input (RxD3) for reception can be input to the external interrupt pin (INTP0) and timer array unit (TAU).

Figure 13-88. Port Configuration for Manipulating Reception of LIN



Remark ISC0, ISC1: Bits 0 and 1 of the input switch control register (ISC) (See **Figure 13-17**.)

16.4 Operation of DMA Controller

16.4.1 Operation procedure

<1> The DMA controller is enabled to operate when DENn = 1. Before writing the other registers, be sure to set DENn to 1. Use 80H to write with an 8-bit manipulation instruction.

<2> Set an SFR address, a RAM address, the number of times of transfer, and a transfer mode of DMA transfer to the DSAn, DRAn, CBCn, and DMCn registers.

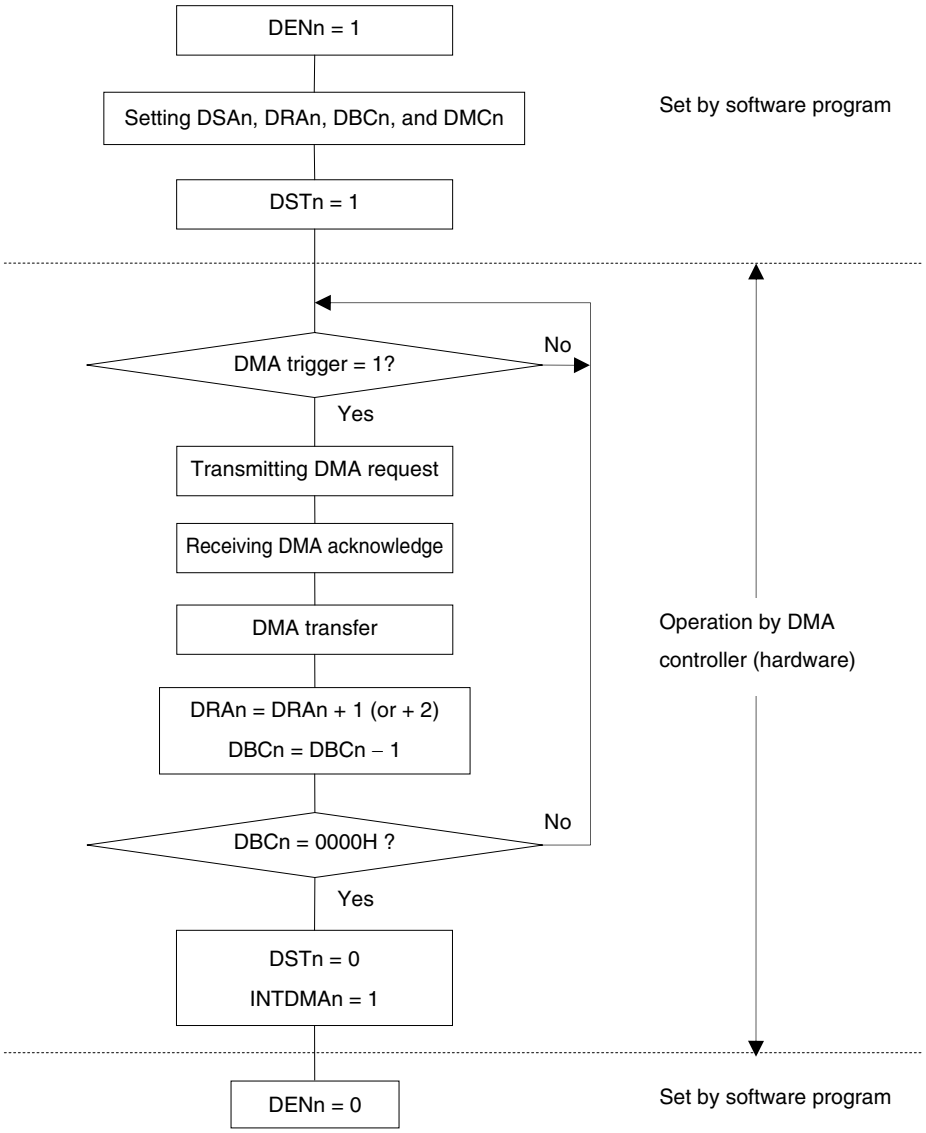
<3> The DMA controller waits for a DMA trigger when DSTn = 1. Use 81H to write with an 8-bit manipulation instruction.

<4> When a software trigger (STGn) or a start source trigger specified by IFCn3 to IFCn0 is input, a DMA transfer is started.

<5> Transfer is completed when the number of times of transfer set by the DBCn register reaches 0, and transfer is automatically terminated by occurrence of an interrupt (INTDMAn).

<6> Stop the operation of the DMA controller by clearing DENn to 0 when the DMA controller is not used.

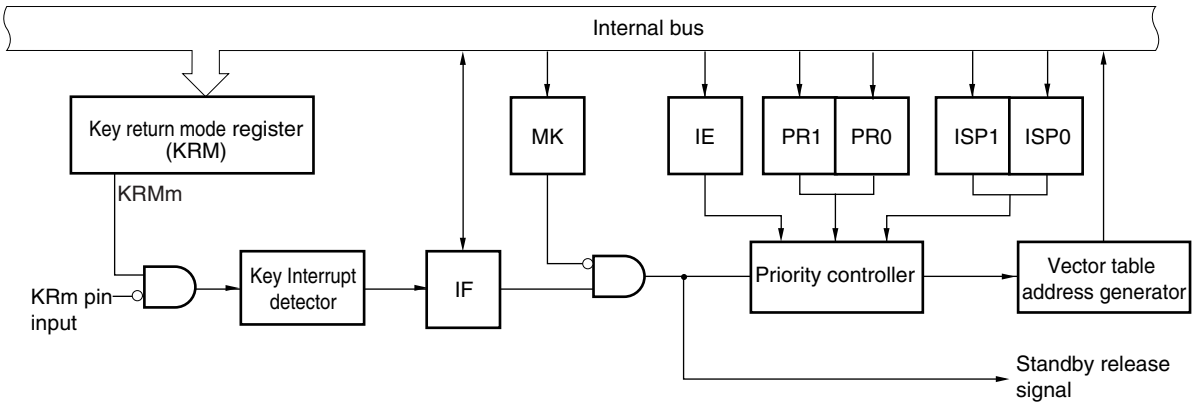
Figure 16-6. Operation Procedure



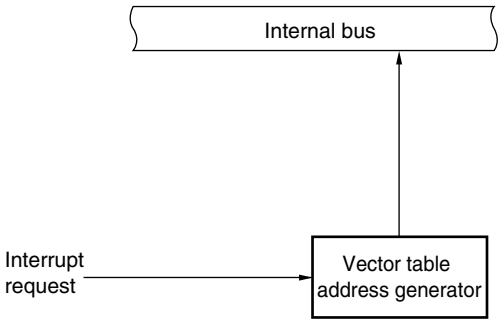
Remark n: DMA channel number (n = 0, 1)

Figure 17-1. Basic Configuration of Interrupt Function (2/2)

<R> **(C) External maskable interrupt (INTKR)**



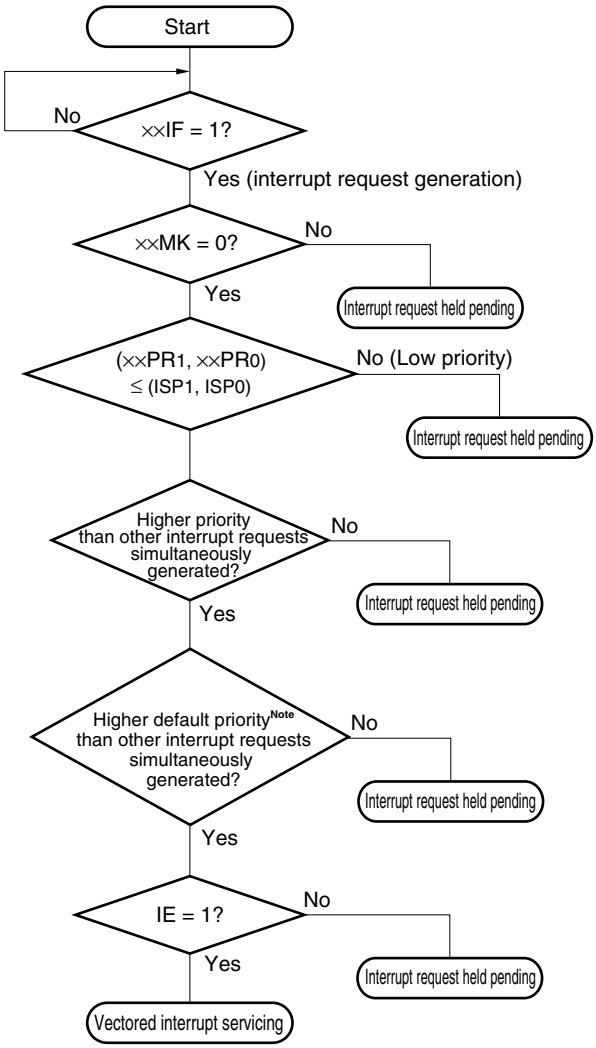
(D) Software interrupt



Remarks 1. IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

2. m = 0 to 7

Figure 17-7. Interrupt Request Acknowledgment Processing Algorithm



××IF: Interrupt request flag
××MK: Interrupt mask flag
××PR0: Priority specification flag 0
××PR1: Priority specification flag 1
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP0, ISP1: Flag that indicates the priority level of the interrupt currently being serviced (see **Figure 17-6**)

Note For the default priority, refer to **Table 17-1 Interrupt Source List**.

Table 28-5. Operation List (4/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	XCH	A, ES:!addr16	5	3	–	A ←→ (ES, addr16)			
		A, ES:[DE]	3	3	–	A ←→ (ES, DE)			
		A, ES:[DE + byte]	4	3	–	A ←→ ((ES, DE) + byte)			
		A, ES:[HL]	3	3	–	A ←→ (ES, HL)			
		A, ES:[HL + byte]	4	3	–	A ←→ ((ES, HL) + byte)			
		A, ES:[HL + B]	3	3	–	A ←→ ((ES, HL) + B)			
		A, ES:[HL + C]	3	3	–	A ←→ ((ES, HL) + C)			
	ONEB	A	1	1	–	A ← 01H			
		X	1	1	–	X ← 01H			
		B	1	1	–	B ← 01H			
		C	1	1	–	C ← 01H			
		saddr	2	1	–	(saddr) ← 01H			
		!addr16	3	1	–	(addr16) ← 01H			
		ES:!addr16	4	2	–	(ES, addr16) ← 01H			
	CLRB	A	1	1	–	A ← 00H			
		X	1	1	–	X ← 00H			
		B	1	1	–	B ← 00H			
		C	1	1	–	C ← 00H			
		saddr	2	1	–	(saddr) ← 00H			
		!addr16	3	1	–	(addr16) ← 00H			
		ES:!addr16	4	2	–	(ES,addr16) ← 00H			
	MOVS	[HL + byte], X	3	1	–	(HL + byte) ← X	×		×
		ES:[HL + byte], X	4	2	–	(ES, HL + byte) ← X	×		×
16-bit data transfer	MOVW	rp, #word	3	1	–	rp ← word			
		saddrp, #word	4	1	–	(saddrp) ← word			
		sfrp, #word	4	1	–	sfrp ← word			
		AX, saddrp	2	1	–	AX ← (saddrp)			
		saddrp, AX	2	1	–	(saddrp) ← AX			
		AX, sfrp	2	1	–	AX ← sfrp			
		sfrp, AX	2	1	–	sfrp ← AX			
		AX, rp Note 3	1	1	–	AX ← rp			
		rp, AX Note 3	1	1	–	rp ← AX			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except rp = AX

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum (except when branching to the external memory area).

3. In products where the external memory area is adjacent to the internal flash area, the number of waits is added to the number of instruction execution clocks placed in the last address (16-byte max.) in the flash memory, in order to use the external bus interface function. This should be done because, during pre-reading of the instruction code, an external memory wait being inserted due to an external memory area exceeding the flash space is accessed. For the number of waits, refer to **5.4 Number of Instruction Wait Clocks for Data Access**.

(3) X1 oscillation: Ceramic resonator (AMPH = 1, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd.	CSTCE12M0G55-R0	SMD	12.0	Internal (33)	Internal (33)	1.8	5.5
	CSTCE16M0V53-R0	SMD	16.0	Internal (15)	Internal (15)	1.8	
	CSTLS16M0X51-B0	Lead		Internal (5)	Internal (5)	1.8	
	CSTCE20M0V53-R0	SMD	20.0	Internal (15)	Internal (15)	1.9	
	CSTCG20M0V53-R0	Small SMD		Internal (15)	Internal (15)	2.0	
	CSTLS20M0X51-B0	Lead		Internal (5)	Internal (5)	1.9	
TOKO, Inc.	DCRHYC(P)12.00A	Lead	12.0	Internal (22)	Internal (22)	1.8	5.5
	DCRHZ(P)16.00A-15	Lead	16.0	Internal (15)	Internal (15)		
	DCRHZ(P)20.00A-15	Lead	20.0	Internal (15)	Internal (15)	2.0	
	DECRHZ20.00	SMD		Internal (10)	Internal (10)	1.8	

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

<R> **When doing so, check the conditions for using the AMPH bit, RMC register, and whether to enter or exit the STOP mode.**

The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KJ3 so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(4) Serial interface: IIC0

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

(a) IIC0

Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency	f_{SCL}	6.7 MHz ≤ f_{CLK}	0	100	0	400	kHz
		4.0 MHz ≤ f_{CLK} < 6.7 MHz	0	100	0	340	kHz
		3.2 MHz ≤ f_{CLK} < 4.0 MHz	0	100	–	–	kHz
		2.0 MHz ≤ f_{CLK} < 3.2 MHz	0	85	–	–	kHz
Setup time of restart condition[Note 1]	$t_{SU:STA}$		4.7		0.6		μs
Hold time	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCL0 = "L"	t_{LOW}		4.7		1.3		μs
Hold time when SCL0 = "H"	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	CL00 = 1 and CL01 = 1	0	3.45[Note 3]	0	0.9[Note 4]	μs
				5.50[Note 5]		1.5[Note 6]	μs
		CL00 = 0 and CL01 = 0, or CL00 = 1 and CL01 = 0	0	3.45	0	0.9[Note 7]	μs
						0.95[Note 8]	μs
		CL00 = 0 and CL01 = 1	0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

3. When 3.2 MHz ≤ f_{CLK} ≤ 4.19 MHz.

4. When 6.7 MHz ≤ f_{CLK} ≤ 8.38 MHz.

5. When 2.0 MHz ≤ f_{CLK} < 3.2 MHz. At this time, use the SCL0 clock within 85 kHz.

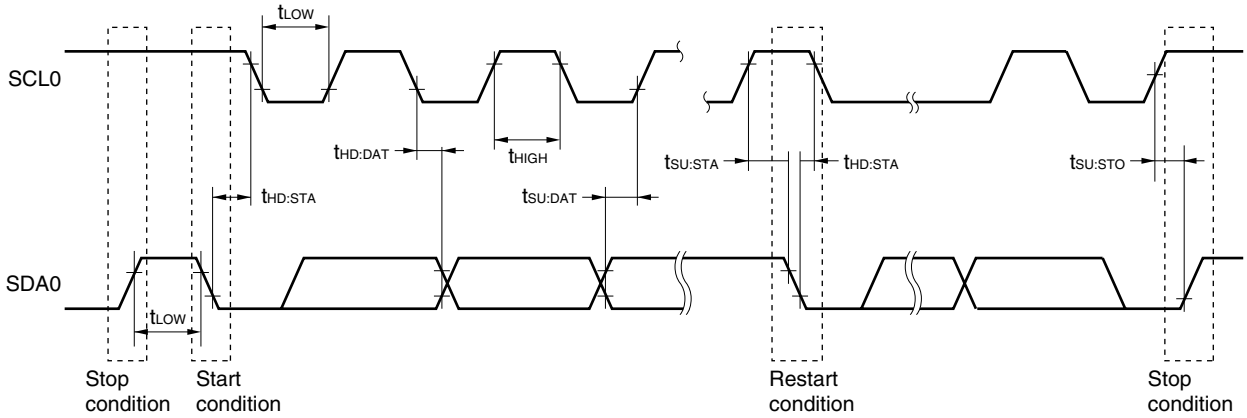
6. When 4.0 MHz ≤ f_{CLK} < 6.7 MHz. At this time, use the SCL0 clock within 340 kHz.

7. When 8.0 MHz ≤ f_{CLK} ≤ 16.76 MHz.

8. When 7.6 MHz ≤ f_{CLK} < 8.0 MHz.

Remark CL00, CL01, DFC0: Bits 0, 1, and 2 of the IIC clock select register 0 (IICCL0)

IIC0 serial transfer timing



DC Characteristics (6/12)

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, P112 to P117, P120, P125 to P127, P131 to P137, P140 to P147, P160 to P163, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P20 to P27, P150 to P157	$V_I = AV_{REF0}$, 2.7 V ≤ AV_{REF0} ≤ V_{DD}				1	μA
			$V_I = AV_{REF0}$, AV_{REF0} = V_{DD} < 2.7 V					
	I_{LIH3}	P110, P111	$V_I = AV_{REF1}$, 2.7 V ≤ AV_{REF1} ≤ V_{DD}				1	μA
			$V_I = AV_{REF1}$, AV_{REF1} = V_{DD} < 2.7 V					
	I_{LIH4}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{DD}$	In Input port			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P107, P112 to P117, P120, P125 to P127, P131 to P137, P140 to P147, P160 to P163, FLMD0, $\overline{\text{RESET}}$	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P20 to P27, P150 to P157	$V_I = V_{SS}$, 2.7 V ≤ AV_{REF0} ≤ V_{DD}				−1	μA
			$V_I = V_{SS}$, AV_{REF0} = V_{DD} < 2.7 V					
	I_{LIL3}	P110, P111	$V_I = V_{SS}$, 2.7 V ≤ AV_{REF1} ≤ V_{DD}				−1	μA
			$V_I = V_{SS}$, AV_{REF1} = V_{DD} < 2.7 V					
	I_{LIL4}	P121 to P124 (X1, X2, XT1, XT2)	$V_I = V_{SS}$	In Input port			−1	μA
				In resonator connection			−10	μA

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (11/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70 °C	V_{DD} = 5.0 V		2.2	26.0	μA
				V_{DD} = 3.0 V		2.2	26.0	μA
				V_{DD} = 2.0 V		2.1	25.8	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85 °C	V_{DD} = 5.0 V		2.2	41.0	μA
				V_{DD} = 3.0 V		2.2	41.0	μA
				V_{DD} = 2.0 V		2.1	40.8	μA
	I_{DD3} Note 3	STOP mode	T_A = –40 to +70 °C			1.1	21.0	μA
			T_A = –40 to +85 °C			1.1	36.0	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When internal high-speed oscillator and high-speed system clock are stopped. When watchdog timer is stopped.

3. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. When subsystem clock is stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

<R> **2.** Temperature condition of the TYP. value is T_A = 25°C

LVI Circuit Characteristics (T_A = –40 to +85°C, $V_{POC} \le V_{DD} = EV_{DD1} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1}$ =0 V)

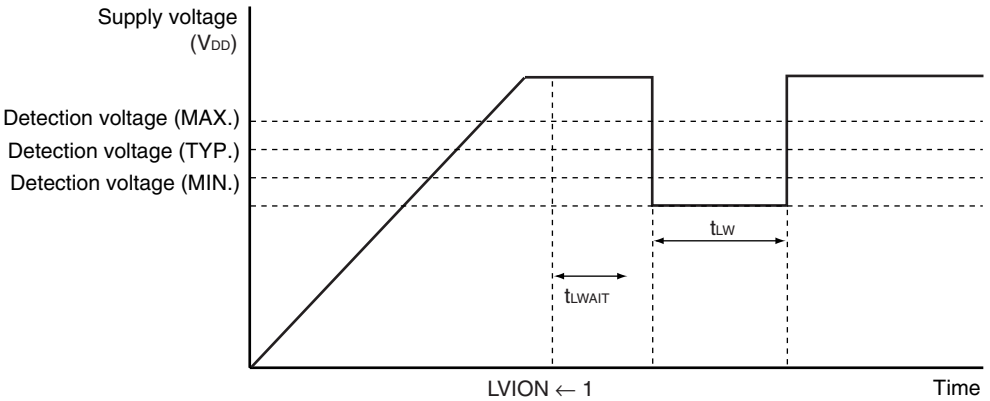
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		1.97	2.07	2.17	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	V_{EXLVI}	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Supply voltage when power supply voltage is turned on	V_{PUPLVI}	When LVI default start function enabled is set	1.87	2.07	2.27	V
Minimum pulse width		t_{LW}		2.00			μs
Detection delay time						200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

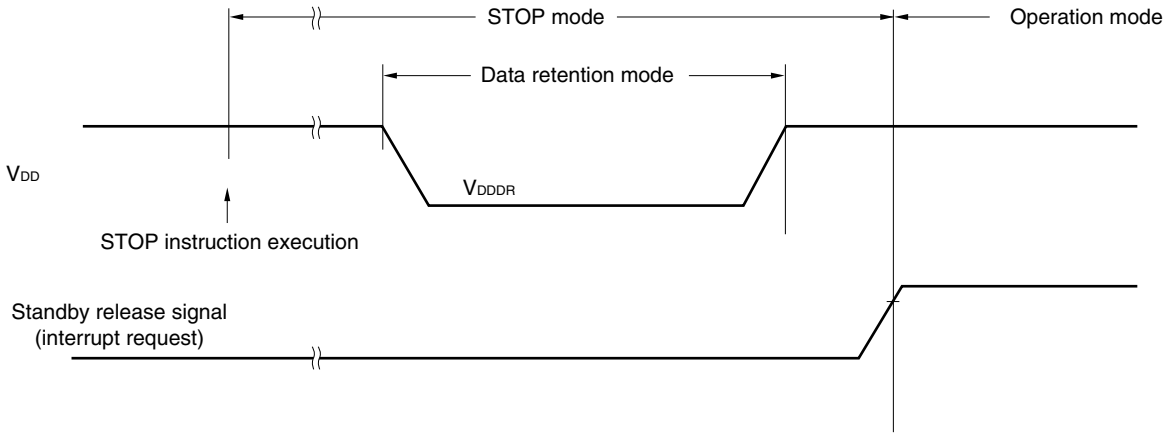
LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.5[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
V_{DD} supply current	I_{DD}	TYP. = 10 MHz, MAX. = 20 MHz			4.5	15	mA
CPU/peripheral hardware clock frequency	f_{CLK}			2		20	MHz
Number of rewrites (number of deletes per block)	C_{WRT}	Used for updating programs When using flash memory programmer and NEC Electronics self programming library	Retained for 15 years	100			Times
		Used for updating data When using NEC Electronics EEPROM emulation library (usable ROM size: 6 KB of 3 consecutive blocks)	Retained for 5 years	10,000			Times

Remark When updating data multiple times, use the flash memory as one for updating data.

(3/35)

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 4	Soft	Port functions	P16/TI01/TO01/ INTP5/EX30, P17/TI02/TO02/ EX31	To use P16/TI01/TO01/INTP5/EX30 or P17/TI02/TO02/EX31 as a general-purpose port, set bits 1 and 2 (TO01, TO02) of timer output register 0 (TO0) and bits 1 and 2 (TOE01, TOE02) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.	p.115 ☐
			P15/RTCDIV/ RTCCL/EX29	To use P15/RTCDIV/RTCCL/EX29 as a general-purpose port, set bit 4 (RCLOE0) of real-time counter control register 0 (RTCC0) and bit 6 (RCLOE2) of real-time counter control register 2 (RTCC2) to “0”, which is the same as their default status settings.	p.115 ☐
			Port 1	Do not enable outputting other alternate functions when the external expansion output (address bus) function is used.	p.115 ☐
	Hard		Port 2	See 2.2.18 AV_{REF0} for the voltage to be applied to the AV_{REF0} pin when using port 2 as a digital I/O.	p.121 ☐
	Soft		P31/TI03/TO03/ INTP4	To use P31/TI03/TO03/INTP4 as a general-purpose port, set bit 3 (TO03) of timer output register 0 (TO0) and bit 3 (TOE03) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.	p.123 ☐
			P30/RTC1HZ/ INTP3	To use P30/RTC1HZ/INTP3 as a general-purpose port, set bit 5 (RCLOE1) of real-time counter control register 0 (RTCC0) to “0”, which is the same as its default status setting.	p.123 ☐
			P40/TOOL0, P41/TOOL1	When a tool is connected, the P40 pin cannot be used as a port pin. When the on-chip debug function is used, P41 pin can be used as follows by the mode setting on the debugger. 1-line mode: can be used as a port (P41). 2-line mode: used as a TOOL1 pin and cannot be used as a port (P41).	p.125 ☐
			P43/$\overline{\text{SCK01}}$, P44/SI01, P45/SO01	To use P43/$\overline{\text{SCK01}}$, P44/SI01, or P45/SO01 as a general-purpose port, note the serial array unit 0 setting. For details, refer to Table 13-6 Relationship Between Register Settings and Pins (Channel 1 of Unit 0: CSI01, UART0 reception).	p.125 ☐
			P42/TI04/TO04, P46/INTP1/TI05/ TO05	To use P42/TI04/TO04 or P46/INTP1/TI05/TO05 as a general-purpose port, set bits 4 and 5 (TO04, TO05) of timer output register 0 (TO0) and bits 4 and 5 (TOE04, TOE05) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.	p.125 ☐
			P60/SCL0, P61/SDA0	When using P60/SCL0 or P61/SDA0 as a general-purpose port, stop the operation of serial interface IIC0.	p.136 ☐
			P95/$\overline{\text{SCK11}}$/SCL 11, P96/SI11/SDA11 , P97/SO11	To use P95/$\overline{\text{SCK11}}$/SCL11, P96/SI11/SDA11, or P97/SO11 as a general-purpose port, note the serial array unit setting. For details, refer to Table 13-8 Relationship Between Register Settings and Pins (Channel 3 of Unit 0: CSI11, UART1 Reception, IIC11).	p.141 ☐
	Hard		Port 11	See 2.2.19 AV_{REF1} for the voltage to be applied to the AV_{REF1} pin when using Port 11 as digital I/O.	p.146 ☐
	Soft		P121 to P124	The function setting on P121 to P124 is available only once after the reset release. The port once set for connection to an oscillator cannot be used as an input port unless the reset is performed.	p.148 ☐
			P125/$\overline{\text{SCK21}}$/SC L21, P126/SI21/SDA2 1, or P127/SO21	To use P125/$\overline{\text{SCK21}}$/SCL21, P126/SI21/SDA21, or P127/SO21 as a general-purpose port, note the serial array unit 1 setting. For details, refer to Table 13-10 Relationship Between Register Settings and Pins (Channel 1 of Unit 1: CSI21, UART2 reception, IIC21).	p.148 ☐
			P131/TI06/TO06	To use P131/TI06/TO06 as a general-purpose port, set bit 6 (TO06) of timer output register 0 (TO0) and bit 6 (TOE06) of timer output enable register 0 (TOE0) to “0”, which is the same as their default status setting.	p.153 ☐