Renesas Electronics America Inc - UPD78F1186AGJ-GAE-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, EBI/EMI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	127
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1186agj-gae-ax

Pin Identification

ANI0 to ANI15: Analog input

ANO0, ANO1: Analog output

ASTB: Address strobe

AV_{REF0}, AV_{REF1}: Analog reference voltage

AV_{SS} : Analog ground

CLKOUT: Clock output

EV_{DD0}, EV_{DD1}: Power supply for port

EV_{SS0}, EV_{SS1}: Ground for port

EX0 to EX35: External extension bus

EXCLK: External clock input (Main system clock)

EXLVI: External potential input for low-voltage detector

FLMD0: Flash programming mode

INTP0 to INTP11: External interrupt input

KR0 to KR7: Key return

P00 to P07: Port 0

P10 to P17: Port 1

P20 to P27: Port 2

P30 to P37: Port 3

P40 to P47: Port 4

P50 to P57: Port 5

P60 to P67: Port 6

P70 to P77: Port 7

P80 to P87: Port 8

P90 to P97: Port 9

P100 to P107: Port 10

P110 to P117: Port 11

P120 to P127: Port 12

P130 to P137: Port 13

P140 to P147: Port 14

P150 to P157: Port 15

P160 to P163: Port 16

PCLBUZ0, PCLBUZ1: Programmable clock output/ buzzer output

$\overline{RD}$: Read strobe

REGC: Regulator capacitance

$\overline{RESET}$: Reset

RTC1HZ: Real-time counter correction clock (1 Hz) output

RTCCL: Real-time counter clock (32 kHz original oscillation) output

RTCDIV: Real-time counter clock (32 kHz divided frequency) output

RxD0 to RxD3: Receive data

$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK11}$, $\overline{SCK20}$, $\overline{SCK21}$: Serial clock input/output

SCL0, SCL10, SCL11, SCL20, SCL21: Serial clock input/output

SDA0, SDA10, SDA11, SDA20, SDA21: Serial data input/output

SI00, SI01, SI10, SI11, SI20, SI21: Serial data input

SO00, SO01, SO10, SO11, SO20, SO21: Serial data output

TI00 to TI07, TI10 to TI13: Timer input

TO00 to TO07, TO10 to TO13: Timer output

TOOL0: Data input/output for tool

TOOL1: Clock output for tool

TxD0 to TxD3: Transmit data

V_{DD}: Power supply

V_{SS}: Ground

$\overline{WAIT}$: Wait

$\overline{WR0}$: Lower byte write strobe

$\overline{WR1}$: Upper byte write strobe

X1, X2: Crystal oscillator (main system clock)

XT1, XT2: Crystal oscillator (subsystem clock)

3.1.2 Mirror area

The 78K0R/KJ3 mirrors the data flash area of 00000H to 0FFFFH or 10000H to 1FFFFH, to F0000H to FFFFFH (the data flash area to be mirrored is set by the processor mode control register (PMC)).

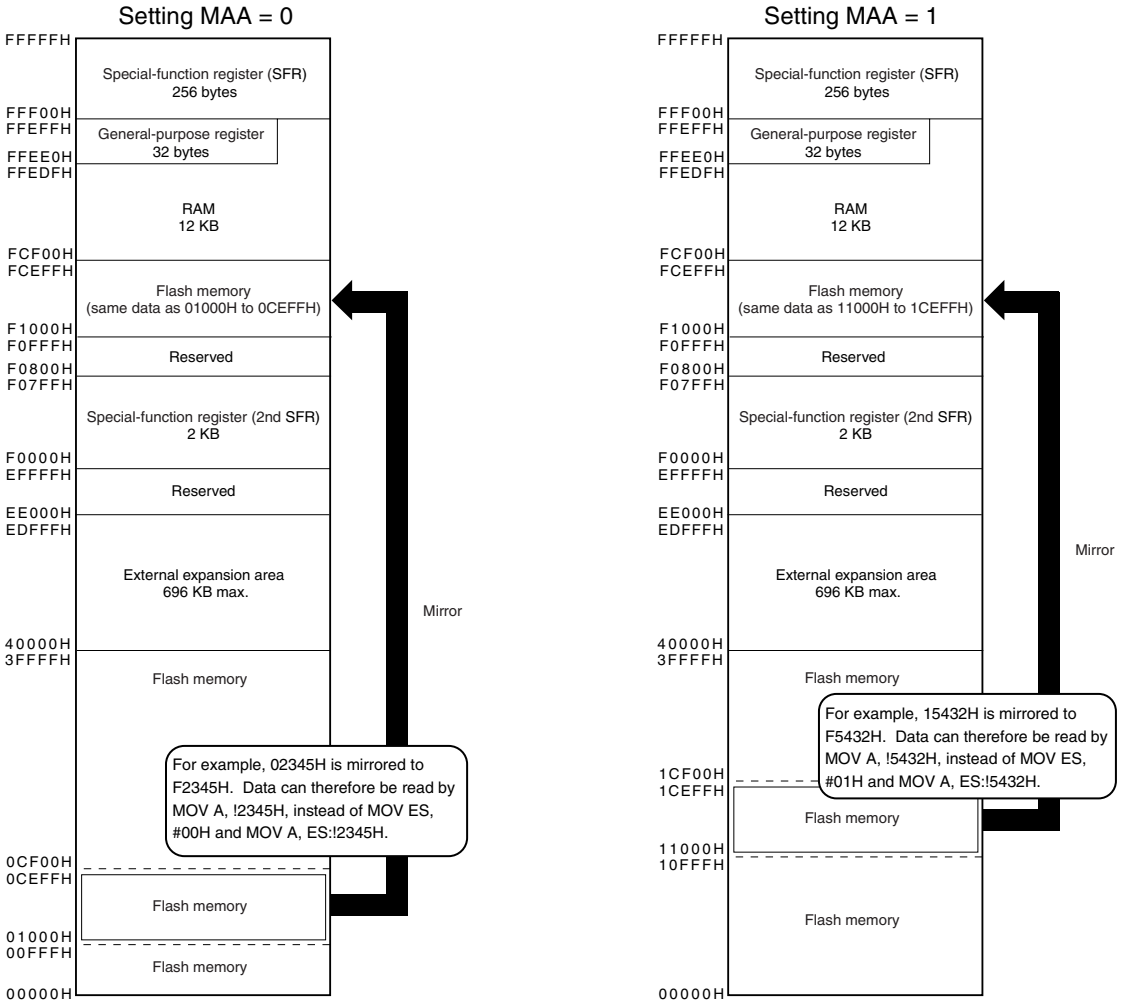
By reading data from F0000H to FFFFFH, an instruction that does not have the ES registers as an operand can be used, and thus the contents of the data flash can be read with the shorter code. However, the data flash area is not mirrored to the SFR, extended SFR, RAM, and use prohibited areas.

See **3.1 Memory Space** for the mirror area of each product.

The mirror area can only be read and no instruction can be fetched from this area.

The following show examples.

Example μPD78F1186A (Flash memory: 256 KB, RAM: 12 KB)



Remark MAA: Bit 0 of the processor mode control register (PMC).

PMC register is described below.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 by a priority specification flag register (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **17.3 (3)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 3-14. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves data as shown in Figure 3-15.

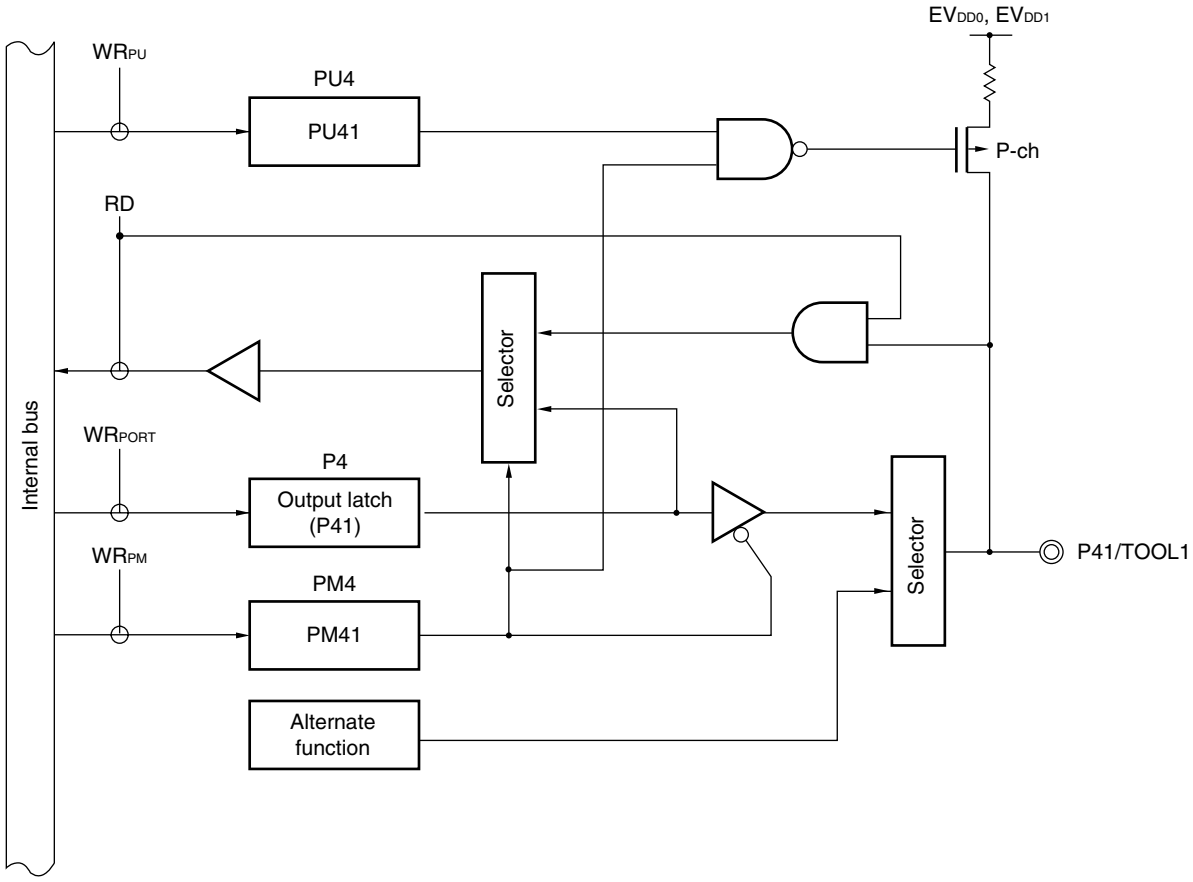
Caution 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

<R> **2. The values of the stack pointer must be set to even numbers. If odd numbers are specified, the least significant bit is automatically cleared to 0.**

3. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.

4. While using the self-programming function, the area of FFE20H to FFEFFH cannot be used as a stack memory. Furthermore, the areas of F8700H to F8EFFH cannot be used with the μPD78F1188A, respectively.

Figure 4-18. Block Diagram of P41



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

4.2.15 Port 14

Port 14 is an 8-bit I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 to P147 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14).

Input to the P142 and P143 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 14 (PIM14).

Output from the P142 to P144 pins can be specified as N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 14 (POM14).

This port can also be used for timer I/O, external interrupt request input, clock/buzzer output, serial interface data I/O, and clock I/O.

Reset signal generation sets port 14 to input mode.

Figures 4-47 to 4-50 show block diagrams of port 14.

Cautions 1. To use P142/$\overline{\text{SCK20}}$/SCL20, P143/SI20/RxD2/SDA20 or P144/SO20/TxD2 as a general-purpose port, note the serial array unit 1 setting. For details, refer to the following tables.

- **Table 13-9 Relationship Between Register Settings and Pins (Channel 0 of Unit 1: CSI20, UART2 Transmission, IIC20)**
- **Table 13-10 Relationship Between Register Settings and Pins (Channel 1 of Unit 1: CSI21, UART2 reception, IIC21).**

2. To use P145/TI07/TO07 as a general-purpose port, set bit 7 (TO07) of timer output register 0 (TO0) and bit 7 (TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

3. To use P140/PCLBUZ0/INTP6 or P141/PCLBUZ1/INTP7 as a general-purpose port, set bit 7 of clock output select register 0 and 1 (CKS0, CKS1) to "0", which is the same as their default status setting.

Table 6-4. CPU Clock Transition and SFR Register Setting Examples (4/4)

<R> **(9) CPU clock changing from subsystem clock (D) to high-speed system clock (C)**

(Setting sequence of SFR registers) ⟶

Setting Flag of SFR Register / Status Transition	OSTS Register	CSC Register	OSMC Register	OSTC Register	CKC Register	
		MSTOP	FSEL		MCM0	CSS
(D) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	**Note 1**	0	0	Must be checked	1	0
(D) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	**Note 1**	0	1 Note 2	Must be checked	1	0
(D) → (C) (external main clock)	**Note 1**	0	0/1	Must not be checked	1	0

Unnecessary if the CPU is operating with the high-speed system clock

Unnecessary if these registers are already set

Notes 1. Set the oscillation stabilization time as follows.
- Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS

2. FSEL = 1 when f_{CLK} > 10 MHz
If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) and CHAPTER 30 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)).

(10) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
• HALT mode (F) set while CPU is operating with high-speed system clock (C)
• HALT mode (G) set while CPU is operating with subsystem clock (D)

Status Transition	Setting
(B) → (E) (C) → (F) (D) → (G)	Executing HALT instruction

<R> **(11) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)**
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) ⟶

Status Transition		Setting		
(B) → (H)		Stopping peripheral functions that cannot operate in STOP mode	–	Executing STOP instruction
(C) → (I)	In X1 oscillation		Sets the OSTS register	
	External clock		–	

Remark (A) to (I) in Table 6-4 correspond to (A) to (I) in Figure 6-15.

Correction example <2>

Example of correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register is set to its initial value (00H).

Note See **8.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **8.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 0.9999817 Hz)

Oscillation frequency = 32768 × 0.9999817 ≈ 32767.4 Hz

Assume the target frequency to be 32768 Hz (32767.4 Hz + 18.3 ppm) and DEV to be 1.

The expression for calculating the correction value when DEV is 1 is applied.

Correction value = Number of correction counts in 1 minute
= (Oscillation frequency ÷ Target frequency − 1) × 32768 × 60
= (32767.4 ÷ 32768 − 1) × 32768 × 60
= −36

[Calculating the values to be set to (F6 to F0)]

(When the correction value is −36)

If the correction value is 0 or less (when speeding up), assume F6 to be 1.

Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

− {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2	= −36
(/F5, /F4, /F3, /F2, /F1, /F0)	= 17
(/F5, /F4, /F3, /F2, /F1, /F0)	= (0, 1, 0, 0, 0, 1)
(F5, F4, F3, F2, F1, F0)	= (1, 0, 1, 1, 1, 0)

Consequently, when correcting from 32767.4 Hz to 32768 Hz (32767.4 Hz + 18.3 ppm), setting the correction register such that DEV is 1 and the correction value is −36 (bits 6 to 0 of SUBCUD: 1101110) results in 32768 Hz (0 ppm).

Figure 8-28 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (1, 1, 1, 0, 1, 1, 1, 0).

Cautions 4. The operation of the watchdog timer in the HALT and STOP modes differs as follows depending on the set value of bit 0 (WDSTBYON) of the option byte (000C0H).

	WDSTBYON = 0	WDSTBYON = 1
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		

If WDSTBYON = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is cleared to 0 and counting starts.
When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

5. The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

9.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (000C0H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to WDTE during the window open period before the overflow time.

The following overflow time is set.

Table 9-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer
0	0	0	$2^{10}/f_{IL}$ (3.88 ms)
0	0	1	$2^{11}/f_{IL}$ (7.76 ms)
0	1	0	$2^{12}/f_{IL}$ (15.52 ms)
0	1	1	$2^{13}/f_{IL}$ (31.03 ms)
1	0	0	$2^{15}/f_{IL}$ (124.12 ms)
1	0	1	$2^{17}/f_{IL}$ (496.48 ms)
1	1	0	$2^{18}/f_{IL}$ (992.97 ms)
1	1	1	$2^{20}/f_{IL}$ (3971.88 ms)

Caution The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. ( ): f_{IL} = 264 kHz (MAX.)

10.2 Configuration of Clock Output/Buzzer Output Controller

The clock output/buzzer output controller includes the following hardware.

Table 10-1. Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output select registers 0, 1 (CKS0, CKS1) Port mode register 14 (PM14) Port register 14 (P14)

10.3 Registers Controlling Clock Output/Buzzer Output Controller

The following two registers are used to control the clock output/buzzer output controller.

- Clock output select registers 0, 1 (CKS0, CSK1)
- Port mode register 14 (PM14)

(1) Clock output select registers 0, 1 (CKS0, CKS1)

These registers set output enable/disable for clock output or for the buzzer frequency output pin (PCLBUZ0/PCLBUZ1), and set the output clock.

Select the clock to be output from PCLBUZ0 by using CKS0.

Select the clock to be output from PCLBUZ1 by using CKS1.

CKS0 and CKS1 are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

13.6.4 LIN reception

Of UART reception, UART3 supports LIN communication.

For LIN reception, channel 3 of unit 1 (SAU1) is used.

UART	UART0	UART1	UART2	UART3
Support of LIN communication	Not supported	Not supported	Not supported	Supported
Target channel	–	–	–	Channel 0 of SAU1
Pins used	–	–	–	RxD3
Interrupt	–	–	–	INTSR3
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)			
Error interrupt	–	–	–	INTSRE3
Error detection flag	• Framing error detection flag (FEF13) • Parity error detection flag (PEF13) • Overrun error detection flag (OVF13)			
Transfer data length	8 bits			
Transfer rate	Max. $f_{MCK}/6$ [bps] (SDR13 [15:9] = 2 or more), Min. $f_{CLK}/(2 \times 2^{11} \times 128)$ [bps] Note			
Data phase	Forward output (default: high level) Reverse output (default: low level)			
Parity bit	The following selectable • No parity bit (no parity check) • Appending 0 parity (no parity check) • Appending even parity • Appending odd parity			
Stop bit	The following selectable • Appending 1 bit • Appending 2 bits			
Data direction	MSB or LSB first			

Note Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 29 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS) and CHAPTER 30 ELECTRICAL SPECIFICATIONS ((A) GRADE PRODUCTS)**).

Remark f_{MCK}: Operation clock (MCK) frequency of target channel
f_{CLK}: System clock frequency

Figure 13-87 outlines a reception operation of LIN.

Notes 1. The SE0 register is a read-only status register which is set using the SS0 and ST0 registers.

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin. In this case, set channel 2 of unit 0 to operation stop mode or UART1 transmission (refer to **Table 13-7**).
When channel 2 of unit 0 is set to CSI10 or IIC10, this pin cannot be used as an RxD1 function pin. In this case, set channel 3 of unit 0 to operation stop mode or CSI11 or IIC11.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **13.3 (12) Serial output register m (SOm)**.

5. When using UART1 transmission and reception in a pair, set channel 2 of unit 0 to UART1 transmission (refer to **Table 13-7**).

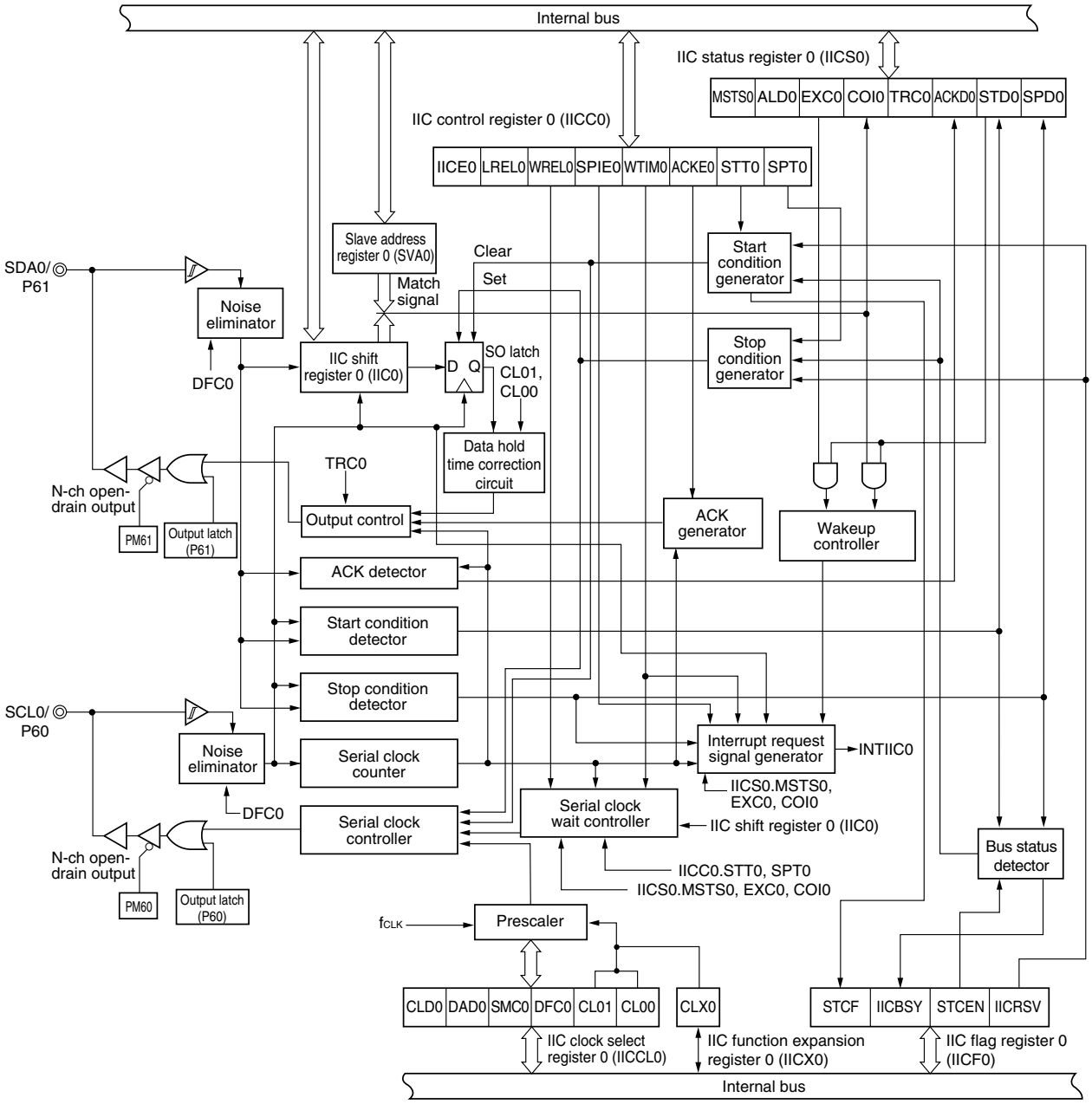
6. The SMR02 register of channel 2 of unit 0 must also be set during UART1 reception. For details, refer to **13.6.2 (1) Register setting**.

7. Set the CKO03 bit to 1 before a start condition is generated. Clear the SO03 bit from 1 to 0 when the start condition is generated.

8. Set the CKO03 bit to 1 before a stop condition is generated. Clear the SO03 bit from 0 to 1 when the stop condition is generated.

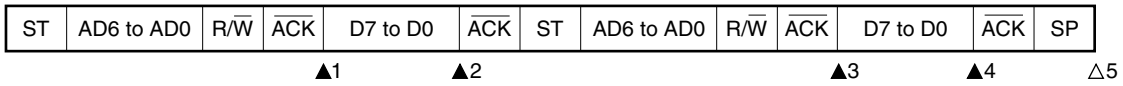
Remark X: Don't care

Figure 14-1. Block Diagram of Serial Interface IIC0



(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

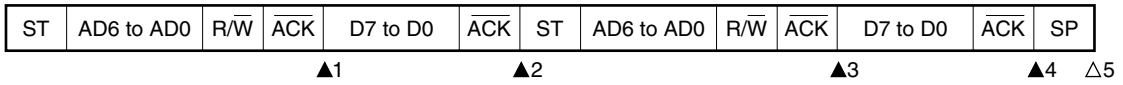
(i) When WTIM0 = 0 (after restart, matches with SVA0)



▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001×000B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001×000B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

(ii) When WTIM0 = 1 (after restart, matches with SVA0)

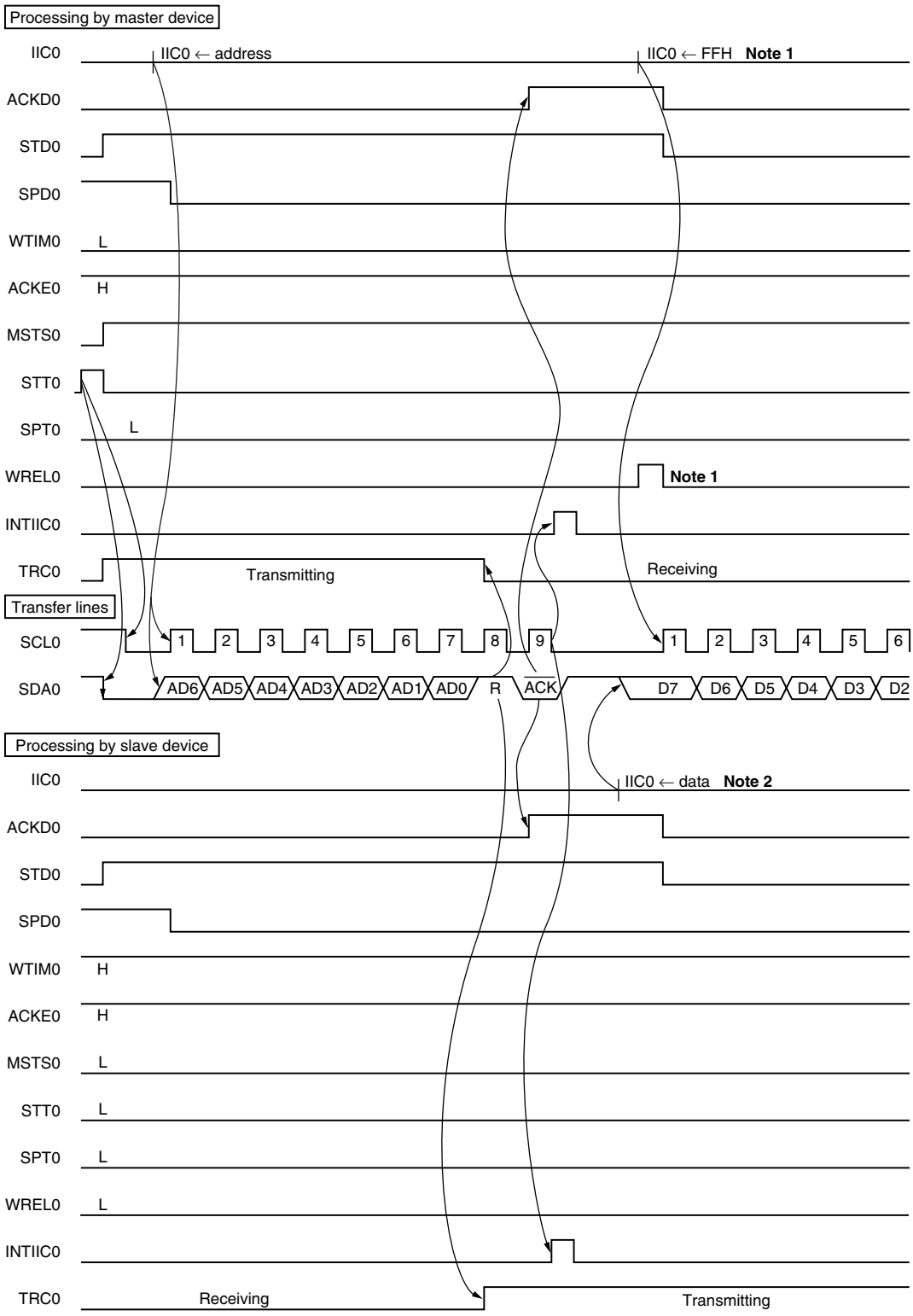


▲1: IICS0 = 0001×110B
▲2: IICS0 = 0001××00B
▲3: IICS0 = 0001×110B
▲4: IICS0 = 0001××00B
△5: IICS0 = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE0 = 1
×: Don't care

Figure 14-29. Example of Slave to Master Communication
(When 8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/3)

(1) Start condition ~ address



Notes 1. To cancel a master wait state, write “FFH” to IIC0 or set WREL0.

2. Write data to IIC0, not setting WREL0, in order to cancel a wait state during slave transmission.

(2) DMA RAM address register n (DRAn)

This is a 16-bit register that is used to set a RAM address that is the transfer source or destination of DMA channel n.

Addresses of the internal RAM area other than the general-purpose registers (FDF00H to FFEDFH in the case of the μPD78F1184A) can be set to this register.

Set the lower 16 bits of the RAM address.

This register is automatically incremented when DMA transfer has been started. It is incremented by +1 in the 8-bit transfer mode and by +2 in the 16-bit transfer mode. DMA transfer is started from the address set to this DRAn register. When the data of the last address has been transferred, DRAn stops with the value of the last address +1 in the 8-bit transfer mode, and the last address +2 in the 16-bit transfer mode.

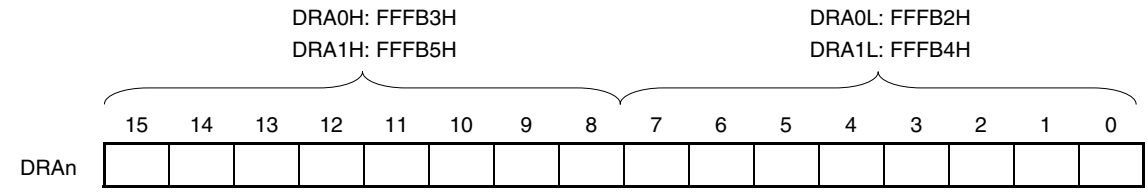
In the 16-bit transfer mode, the least significant bit is ignored and is treated as an even address.

DRAn can be read or written in 8-bit or 16-bit units. However, it cannot be written during DMA transfer.

Reset signal generation clears this register to 0000H.

Figure 16-2. Format of DMA RAM Address Register n (DRAn)

Address: FFFB2H, FFFB3H (DRA0), FFFB4H, FFFB5H (DRA1) After reset: 0000H R/W



(n = 0, 1)

Remark n: DMA channel number (n = 0, 1)

Table 25-1. Wiring Between 78K0R/KJ3 and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer			Pin Name	Pin No.
Signal Name	I/O	Pin Function		
SI/RxD[Notes 1, 2]	Input	Receive signal	TOOL0/P40	21
SO/TxD[Note 2]	Output	Transmit signal		
SCK	Output	Transfer clock	–	–
CLK	Output	Clock output	–	–
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	25
FLMD0	Output	Mode signal	FLMD0	28
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	34
			EV_{DD0}	35
			EV_{DD1}	64
			AV_{REF0}	107
			AV_{REF1}	104
GND	–	Ground	V_{SS}	32
			EV_{SS0}	33
			EV_{SS1}	63
			AV_{SS}	108

Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

DC Characteristics (8/12)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF0} ≤ V_{DD}, 1.8 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		7.0	12.2	mA
				Resonator connection		7.3	12.5	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		7.0	12.2	mA
				Resonator connection		7.3	12.5	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		3.8	6.2	mA
				Resonator connection		3.9	6.3	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		3.8	6.2	mA
				Resonator connection		3.9	6.3	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Normal current mode, Square wave input		2.1	3.0	mA
				Normal current mode, Resonator connection		2.2	3.1	mA
				Low consumption current mode Note 4, Square wave input		1.5	2.1	mA
				Low consumption current mode Note 4, Resonator connection		1.5	2.1	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Normal current mode, Square wave input		1.4	2.1	mA
				Normal current mode, Resonator connection		1.4	2.1	mA
				Low consumption current mode Note 4, Square wave input		1.4	2.0	mA
				Low consumption current mode Note 4, Resonator connection		1.4	2.0	mA
			f_{IH} = 8 MHz Note 5	V_{DD} = 5.0 V		3.1	5.0	mA
				V_{DD} = 3.0 V		3.1	5.0	mA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF0}, and AV_{REF1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When internal high-speed oscillator and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0 and FSEL (bit 0 of operation speed mode control register (OSMC)) = 0.

4. When the RMC register is set to 5AH.

5. When high-speed system clock and subsystem clock are stopped. When FSEL (bit 0 of operation speed mode control register (OSMC)) = 0 is set.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

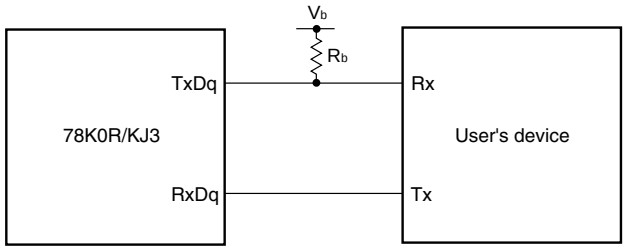
f_{IH}: Internal high-speed oscillation clock frequency

2. For details on the normal current mode and low consumption current mode according to the regulator output voltage, refer to **CHAPTER 23 REGULATOR**.

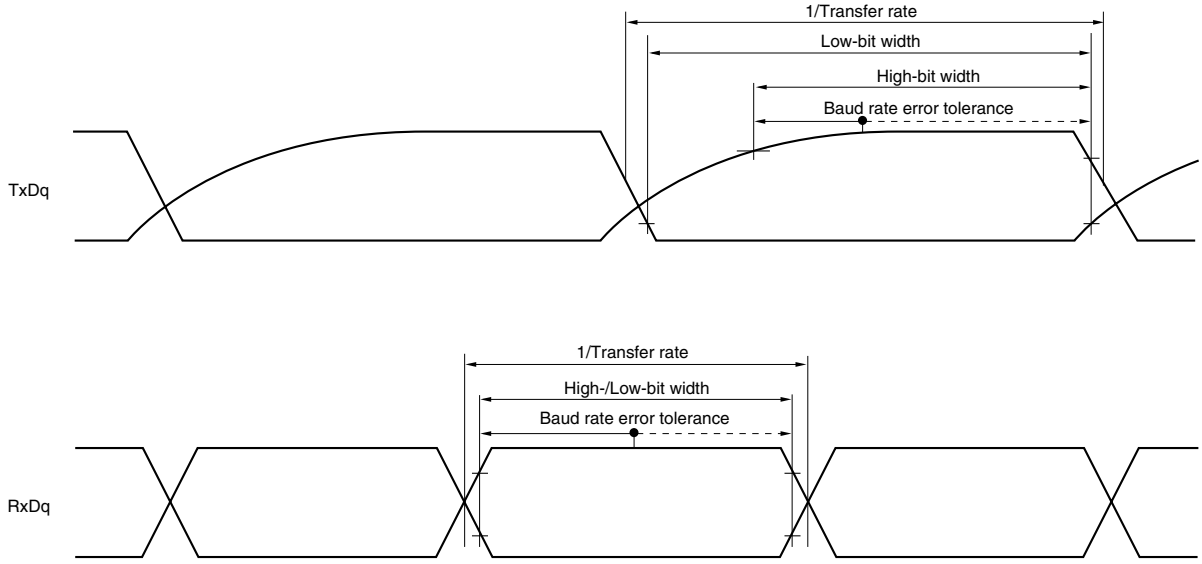
<R> **3.** Temperature condition of the TYP. value is T_A = 25°C

(3) Serial interface: Serial array unit (10/18)

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential)



Caution Select the TTL input buffer for RxDq and the N-ch open drain output (V_{DD} tolerance) mode for TxDq by using the PIMg and POMg registers.

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 1, 2), g: PIM and POM number (g = 0, 14)

3. UART0 and UART3 cannot communicate at different potential. Use UART1 and UART2 for communication at different potential.

Chapter	Classification	Function	Details of Function	Cautions	Page
Chapter 11	Soft	A/D converter	ADCR: 10-bit A/D conversion result register	When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCR may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.	p.376 □
			ADCRH: 8-bit A/D conversion result register	When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.	p.376 □
			ADS: Analog input channel specification register	Be sure to clear bits 4 to 6 to “0”.	p.377 □
				Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 15 (PM2, PM15).	p.377 □
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.377 □
			ADPC: A/D port configuration register	Set a channel to be used for A/D conversion in the input mode by using port mode registers 2 and 15 (PM2, PM15).	p.378 □
				Do not set the pin that is set by ADPC as digital I/O by ADS.	p.378 □
				P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 are set as analog inputs in the order of P157/ANI15, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 as analog inputs, start designing from P157/ANI15.	p.378 □
			PM2, PM15: Port mode registers 2 and 15	If a pin is set as an analog input port, not the pin level but “0” is always read.	p.379 □
			Basic operations of A/D converter	Make sure the period of <2> to <6> is 1 μs or more.	p.380 □
			A/D conversion operation	Make sure the period of <2> to <6> is 1 μs or more.	p.384 □
				<2> may be done between <3> and <5>.	p.384 □
				The period from <7> to <10> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <9> to <10> is the conversion time set using FR2 to FR0, LV1, and LV0.	p.384 □
			Temperature sensor function	The temperature sensor cannot be used when low current consumption mode is set (RMC = 5AH) or when the internal high-speed oscillator has been stopped (HIOSTOP = 1 (bit 0 of CSC register)). The temperature sensor can operate as long as the internal high-speed oscillator operates (HIOSTOP = 0), even if it is not selected as the CPU/peripheral hardware clock source.	p.385 □
			Registers used by temperature sensors	Setting of the A/D port configuration register (ADPC), port mode register 2 (PM2) and port register 2 (P2) is not required when using the temperature sensor. There is no problem if the pin function is set as digital I/O.	p.386 □
				Set the conversion times so as to satisfy the following condition. f_{AD} = 0.6 to 1.8 MHz	p.386 □
				When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion (ADCS = 0) beforehand.	p.386 □
				The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.	p.386 □

(10/13)

Edition	Description	Chapter
3rd Edition	Change of **Figure 13-53 Flowchart of Slave Transmission (in Continuous Transmission Mode)**	CHAPTER 13 SERIAL ARRAY UNIT (continuation)
	Change of transfer rate in **13.5.5 Slave reception**	
	Change of **(b) Serial output enable register m (SOEm) in Figure 13-54. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21)**	
	Modification of **Figure 13-58 Timing Chart of Slave Reception (in Single-Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of transfer rate in **13.5.6 Slave transmission/reception**	
	Change of **Figure 13-62 Procedure for Stopping Slave Transmission/Reception**	
	Change of **Figure 13-63 Procedure for Resuming Slave Transmission/Reception**	
	Modification of **Figure 13-64 Timing Chart of Slave Transmission/Reception (in Single-Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Modification of **Figure 13-66 Timing Chart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode) (Type 1: DAPmn = 0, CKPmn = 0)**	
	Change of **13.5.7 Calculating transfer clock frequency**	
	Change of **Note 2** in **Table 13-2 Selection of Operation Clock**	
	Addition of **Caution** to **13.6 Operation of UART (UART0, UART1, UART2, UART3) Communication**	
	Change of **Figure 13-70 Procedure for Stopping UART Transmission**	
	Change of **Figure 13-72 Timing Chart of UART Transmission (in Single-Transmission Mode)**	
	Change of **Figure 13-74 Timing Chart of UART Transmission (in Continuous Transmission Mode)**	
	Change of **13.6.2 UART reception**	
	Change of **(b) Serial output enable register m (SOEm)** in **Figure 13-76 Example of Contents of Registers for UART Reception of UART (UART0, UART1, UART2, UART3)**	
	Modification of **Figure 13-80 Timing Chart of UART Reception**	
	Modification of transfer data length in **13.6.3 LIN transmission**	
	Change of **Note 2** in **Figure 13-82 Transmission Operation of LIN**	
	Change of **Note 2** in **Table 13-3 Selection of Operation Clock**	
	Addition of **Note** to **13.7 Operation of Simplified I^2C (IIC10, IIC11, IIC20, IIC21) Communication**	
	Addition of **Note** to **13.7.1 Address field transmission**	
	Change of **Figure 13-89 Initial Setting Procedure for Address Field Transmission**	
	Change of **Figure 13-90 Timing Chart of Address Field Transmission**	
	Addition of **Note** to **13.7.2 Data transmission**	
	Change of **Figure 13-93 Timing Chart of Data Transmission**	
	Addition of **Note** to **13.7.3 Data reception**	
	Change of **Figure 13-96 Timing Chart of Data Reception**	
	Change of **Figure 13-97 Flowchart of Data Reception** and change of **Caution**	
	Change of **Figure 13-98 Timing Chart of Stop Condition Generation**	
	Change of **Note 2** in **Table 13-4 Selection of Operation Clock**	